



# A43L3616A Series

## 2M x 16 Bit x 4 Banks Synchronous DRAM

### Preliminary

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#### Document Title

2M x 16 Bit x 4 Banks Synchronous DRAM

#### Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	August 7, 2007	Preliminary
0.1	Change clock frequency from 133MHz to 143MHz at 7ns cycle time	November 14, 2007	
0.2	Add part numbering scheme	February 20, 2008	
0.3	Add A43L4608A part number Modify DC spec.	May 5, 2008	
0.4	Add Test Mode description	August 13, 2008	
0.5	Add automotive temperature grade	November 11, 2008	
0.6	Remove A43L4608A part number Modify DC current spec.	January 7, 2009	
0.7	Add 54 balls CSP (8mm x 8mm) package	August 28, 2009	
0.8	Modify $t_{RAS(max.)}$ from 100ns to 100 $\mu$ s	November 8, 2011	



# A43L3616A Series

## 2M x 16 Bit x 4 Banks Synchronous DRAM

### Preliminary

#### Features

- JEDEC standard 3.3V ± 0.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks / Pulse  $\overline{\text{RAS}}$
- MRS cycle with address key programs
  - CAS Latency (2,3)
  - Burst Length (1,2,4,8)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Industrial operating range: -40°C to +85°C for -U
- Automotive temperature operation: -40°C to +85°C for -A
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Available in 54 Balls CSP (8mm X 8mm) and 54-pin TSOP(II) packages
- Package is available to lead free (-F series)
- All Pb-free (Lead-free) products are RoHS compliant

#### General Description

The A43L3616A is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 X 2,097,152 words by 16 bits, fabricated with AMIC's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on

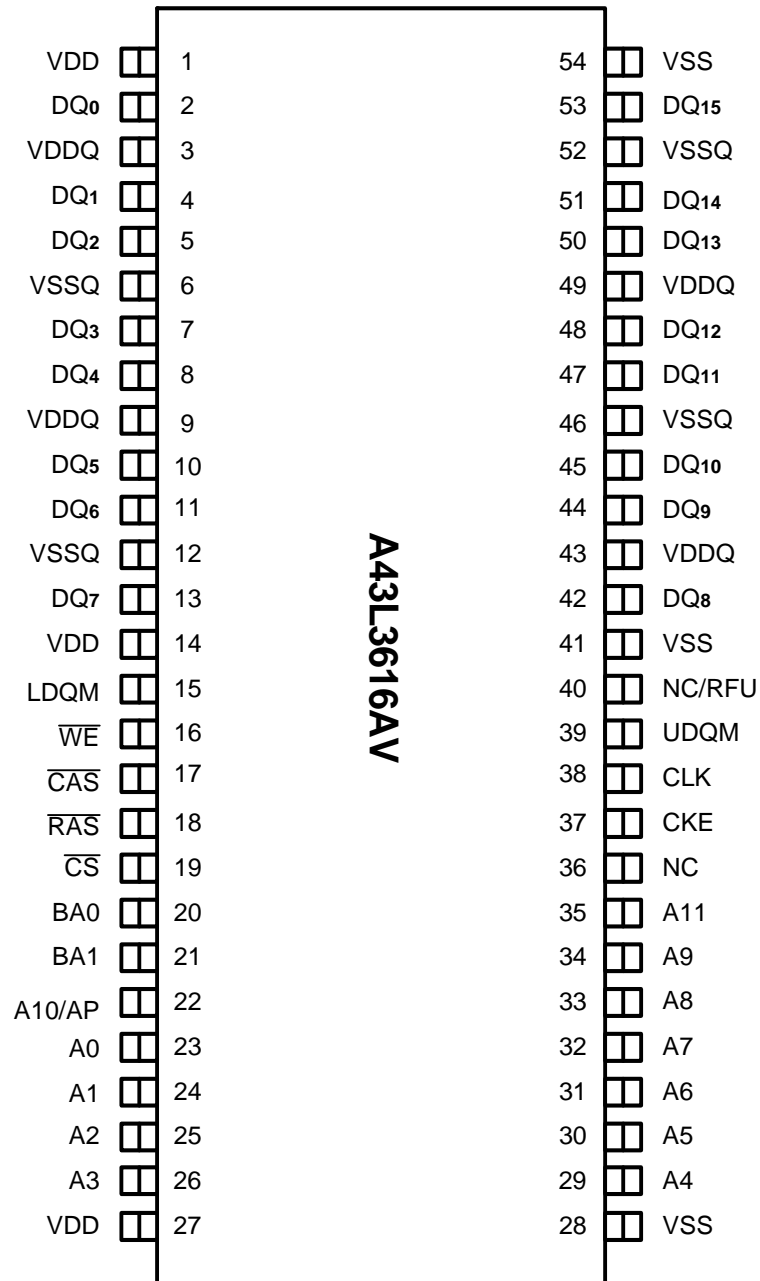
every clock cycle. Range of operating frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

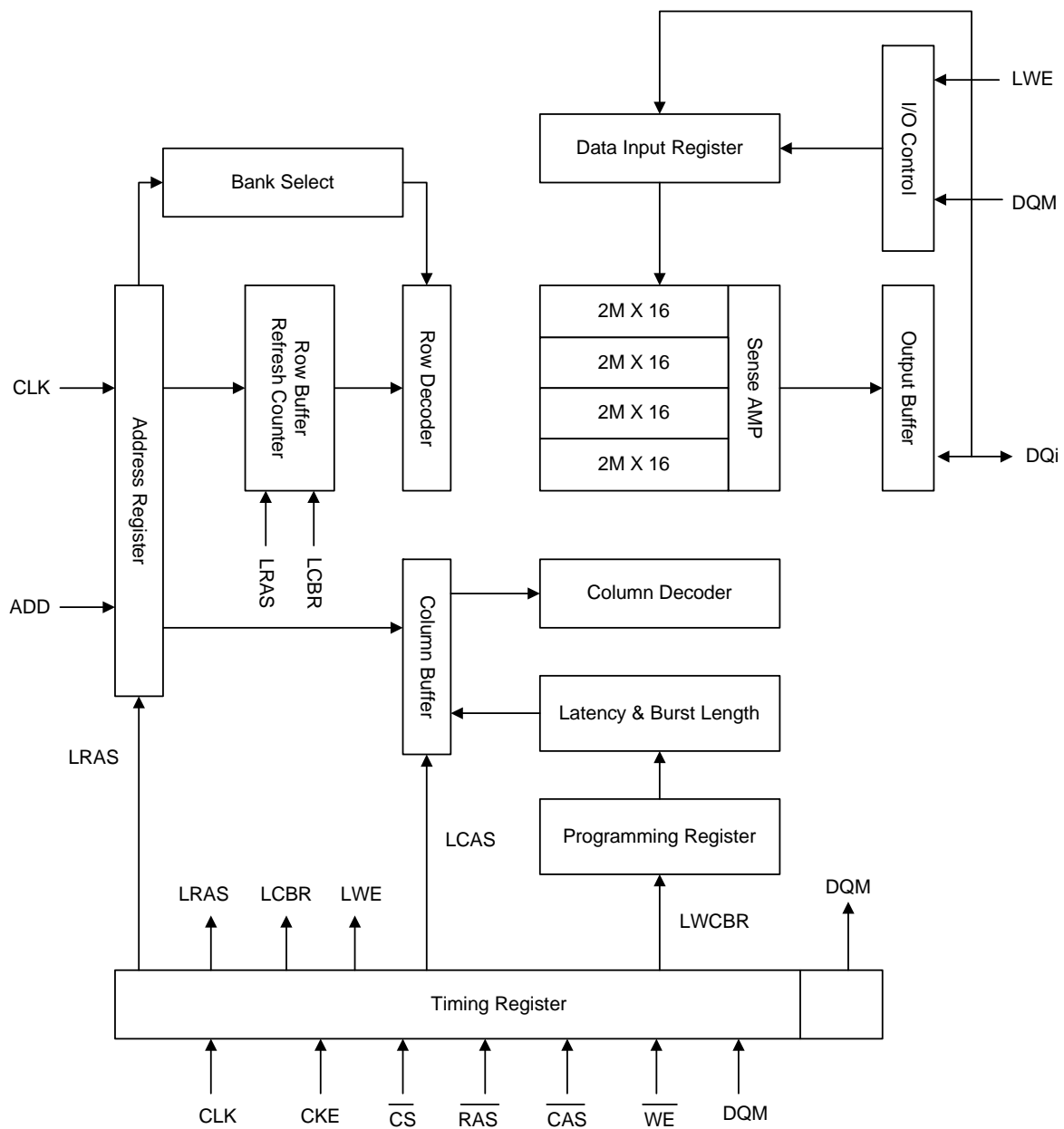
#### Pin Configuration

- 54 Balls CSP (8 mm x 8 mm)

Top View

54 Ball (6X9) CSP						
	1	2	3	7	8	9
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ	VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ	VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ	VSSQ	DQ6	DQ5
E	DQ8	NC	VSS	VDD	LDQM	DQ7
F	UDQM	CLK	CKE	$\overline{\text{CAS}}$	$\overline{\text{RAS}}$	$\overline{\text{WE}}$
G	NC	A11	A9	BA0	BA1	$\overline{\text{CS}}$
H	A8	A7	A6	A0	A1	A10
J	VSS	A5	A4	A3	A2	VDD

**Pin Configuration (continued)**
**■ TSOP (II)**


**Block Diagram**


Notes: This figure shows the A43L3616A.

**Pin Descriptions**

Symbol	Name	Description
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip Select	Disables or Enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + tss prior to new command. Disable input buffers for power down in standby.
A0~A11	Address	Row / Column addresses are multiplexed on the same pins. Row address : RA0~RA11, Column address: CA0~CA8 (x16).
BA0, BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects band for read/write during column address latch time.
$\overline{\text{RAS}}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write Enable	Enables write operation and Row precharge.
DQM, L(U)DQM	Data Input/Output Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active. LDQM corresponds to DQ <sub>0</sub> ~ DQ <sub>7</sub> , UDQM corresponds to DQ <sub>8</sub> ~ DQ <sub>15</sub> .
DQ <sub>0-15</sub>	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power Supply: +3.3V±0.3V/Ground.
VDDQ/VSSQ	Data Output Power/Ground	Provide isolated Power/Ground to DQs for improved noise immunity.
NC/RFU	No Connection	

**Absolute Maximum Ratings\***

Voltage on any pin relative to VSS (Vin, Vout) . . . . .	0.5V to +4.6V
Voltage on VDD supply relative to VSS (VDD, VDDQ) . . . . .	0.5V to +4.6V
Storage Temperature (T <sub>STG</sub> ) . . . . .	-55°C to +125°C
Soldering Temperature X Time (T <sub>SLD</sub> ) . . . . .	260°C X 10sec
Power Dissipation (P <sub>D</sub> ) . . . . .	.1W
Short Circuit Current (I <sub>OS</sub> ) . . . . .	50mA

**\*Comments**

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**Capacitance (TA=25°C, f=1MHz)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	CI1	A0 to A11, BA0, BA1	2.5		3.5	pF
	CI2	CLK, CKE, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , DQM	2.5		3.5	pF
Data Input/Output Capacitance	CI/O	DQ0 to DQ15	4		6.5	pF

**DC Electrical Characteristics**

Recommend operating conditions (Voltage referenced to VSS = 0V, TA = 0°C to +70°C, -40°C to +85°C for industrial temperature range or -40°C to +85°C for automotive temperature range)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD,VDDQ	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	VDD+0.3	V	Note 1
Input Low Voltage	V <sub>IL</sub>	-0.3	0	0.8	V	Note 2
Output High Voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output Low Voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input Leakage Current	I <sub>IL</sub>	-5	-	5	μA	Note 3
Output Leakage Current	I <sub>OL</sub>	-5	-	5	μA	Note 4
Output Loading Condition	See Figure 1					

**Note:**

- V<sub>IH</sub> (max) = 4.6V AC (pulse width ≤ 10ns).
- V<sub>IL</sub> (min) = -1.5V AC (pulse width ≤ 10ns).
- Any input 0V ≤ VIN ≤ VDD + 0.3V, all other pins are not under test = 0V
- Dout is disabled, 0V ≤ Vout ≤ VDD

**Decoupling Capacitance Guide Line**

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between VDD and VSS	C <sub>DC1</sub>	0.1 + 0.01	μF
Decoupling Capacitance between VDDQ and VSSQ	C <sub>DC2</sub>	0.1 + 0.01	μF

- Note:** 1. VDD and VDDQ pins are separated each other.  
 All VDD pins are connected in chip. All VDDQ pins are connected in chip.  
 2. VSS and VSSQ pins are separated each other  
 All VSS pins are connected in chip. All VSSQ pins are connected in chip.

**DC Electrical Characteristics**

 (Recommended operating condition unless otherwise noted, T<sub>A</sub> = 0 to 70°C, -40°C to +85°C for industrial temperature range or -40°C to +85°C for automotive temperature range)

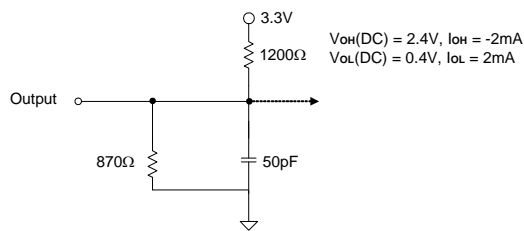
Symbol	Parameter	Test Conditions	Speed			Unit	Notes
			-6	-7	-75		
I <sub>cc1</sub>	Operating Current (One Bank Active)	Burst Length = 1 t <sub>RC</sub> = t <sub>RC</sub> (min), t <sub>CC</sub> = t <sub>CC</sub> (min), I <sub>OL</sub> = 0mA	95	85	80	mA	1
I <sub>cc2P</sub>	Precharge Standby Current in power-down mode	CKE = V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	2			mA	
I <sub>cc2PS</sub>		CLK = V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	1.5				
I <sub>cc2N</sub>	Precharge Standby Current in non power-down mode	CKE = V <sub>IH</sub> (min), $\overline{CS}$ = V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	15			mA	
I <sub>cc2NS</sub>		CKE = V <sub>IH</sub> (min), CLK = V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable.	10				
I <sub>cc3N</sub>	Active Standby current in non power-down mode (One Bank Active)	CKE = V <sub>IH</sub> (min), $\overline{CS}$ = V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	25			mA	
I <sub>cc3NS</sub>		CKE = V <sub>IH</sub> (min), CLK = V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable	20				
I <sub>cc3P</sub>	Active Standby current in power-down mode (One Bank Active)	CKE = V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	4			mA	
I <sub>cc3PS</sub>		CKE & CLK = V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	2				
I <sub>cc4</sub>	Operating Current (Burst Mode)	I <sub>OL</sub> = 0mA, Page Bust All bank Activated, t <sub>CCD</sub> = t <sub>CCD</sub> (min)	120	100	90	mA	1
I <sub>cc5</sub>	Refresh Current	t <sub>RC</sub> = t <sub>RC</sub> (min)	140	120	110	mA	2
I <sub>cc6</sub>	Self Refresh Current	CKE = 0.2V	2	2	2	mA	

- Note:** 1. Measured with outputs open. Addresses are changed only one time during t<sub>CC</sub>(min).  
 2. Refresh period is 64ms. Addresses are changed only one time during t<sub>CC</sub>(min).  
 3. Unless otherwise noted, input swing level is CMOS (V<sub>IH</sub> / V<sub>IL</sub> = VDDQ / VSSQ).

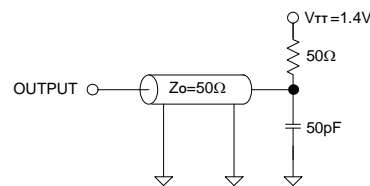
**AC Operating Test Conditions**

(VDD = 3.3V ±0.3V, TA = 0°C to +70°C, -40°C to +85°C for industrial temperature range or -40°C to +85°C for automotive temperature range)

Parameter	Value
AC input levels	V <sub>IH</sub> /V <sub>IL</sub> = 2.4V/0.4V
Input timing measurement reference level	1.4V
Input rise and all time (See note3)	tr/tf = 1ns/1ns
Output timing measurement reference level	1.4V
Output load condition	See Fig.2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

**AC Characteristics**

(AC operating conditions unless otherwise noted)

Symbol	Parameter	CAS Latency	-6		-7		-75		Unit	Note
			Min	Max	Min	Max	Min	Max		
tcc	CLK cycle time	3	6	1000	7	1000	7.5	1000	ns	1
		2	10		10		10			
tsac	CLK to valid Output delay	3	-	5.4	-	5.4	-	5.4	ns	1,2
		2	-	5.4	-	5.4	-	6		
toH	Output data hold time	3	2.5	-	3	-	3	-	ns	2
		2	3	-	3	-	3	-		
tch	CLK high pulse width	2, 3	2.5	-	2.5	-	2.5	-	ns	3
tcl	CLK low pulse width		2.5	-	2.5	-	2.5	-	ns	3
tss	Input setup time		1.5	-	1.5	-	1.5	-	ns	3
tsh	Input hold time		1	-	1	-	1	-	ns	3
tsLZ	CLK to output in Low-Z		1	-	1	-	1	-	ns	2
tshz	CLK to output In Hi-Z		3	-	5.4	-	5.4	-	5.4	ns
		2	-	5.4	-	5.4	-	6		

\*All AC parameters are measured from half to half.

- Note :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
  - Assumed input rise and fall time (tr & tf) = 1ns.  
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.



**Operating AC Parameter**

(AC operating conditions unless otherwise noted)

Symbol	Parameter	CAS Latency	Version			Unit	Note
			-6	-7	-75		
tRRD(min)	Row active to row active delay	2,3	12	14	15	ns	1
tRCD(min)	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		18	20	20	ns	1
tRP(min)	Row precharge time		18	20	20	ns	1
tRAS(min)	Row active time		42	45	45	ns	1
tRAS(max)			100	100	100	$\mu\text{s}$	
tRC(min)	Row cycle time		60	63	65	ns	1
tCDL(min)	Last data in new col. Address delay		1	1	1	CLK	2
tRDL(min)	Last data in row precharge		2	2	2	CLK	2
tCCD(min)	Col. Address to col. Address delay		1	1	1	CLK	

- Note:**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.

**Simplified Truth Table**

Command		CKEn-1	CKEn	$\overline{CS}$	RAS	$\overline{CAS}$	$\overline{WE}$	DQM	BA0 BA1	A10 /AP	A9~A0, A11	Notes	
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1,2	
Refresh	Auto Refresh	H	H	L	L	L	H	X	X			3	
	Self Refresh		Entry								L	H	H
		Exit	L	H	H	X	X	X		3			
			H	X					X	X		3	
Bank Active & Row Addr.		H	X	L	L	H	H	X	V	Row Addr.		4	
Read & Column Addr.	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Addr.	4	
	Auto Precharge Enable									H			4,5
Write & Column Addr.	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Addr.	4	
	Auto Precharge Enable									H			4,5
Reserved		H	X	L	H	H	L	X	X				
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L	X		
	Both Banks								X	H			
Clock Suspend or Active Power Down	Entry	H	L	L	H	H	H	X	X				
				H	X	X	X						
Precharge Power Down Mode	Exit	L	H	X	X	X	X	X	X				
				H	X	X	X						
	Entry	H	L	L	H	H	H	X	X				
				H	X	X	X						
Exit	L	H	L	V	V	V	X	X					
			H	X	X	X							
DQM		H			X				V	X		6	
No Operation Command		H	X	L	H	H	H	X	X				
				H	X	X	X						

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

**Note :** 1. OP Code: Operand Code

- A0~A11, BA0, BA1: Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.  
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions as same as CBR refresh of DRAM.  
The automatical precharge without Row precharge command is meant by "Auto".  
Auto/Self refresh can be issued only at both precharge state.
4. BA0, BA1 : Bank select address.  
If both BA1 and BA0 are "Low" at read, write, row active and precharge, bank A is selected.  
If both BA1 is "Low" and BA0 is "High" at read, write, row active and precharge, bank B is selected.  
If both BA1 is "High" and BA0 is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA1 and BA0 are "High" at read, write, row active and precharge, bank D is selected.  
If A10/AP is "High" at row precharge, BA1 and BA0 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read write command cannot be issued.  
Another bank read write command can be issued at every burst length.
6. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0) but masks the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2)

**Mode Register Filed Table to Program Modes**

Register Programmed with MRS

Address	BA0	BA1	A11	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU		RFU		W.B.L	TM		CAS Latency			BT	Burst Length		

(Note 1) (Note 2)

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Vendor Use Only	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0		0	1	0	2			0	1	0	4	4
1	1		0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
<b>A9</b>	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Reserved	Reserved

**Power Up Sequence**

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200µs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

The device is now ready for normal operation.

- Note :**
1. RFU(Reserved for Future Use) should stay "0" during MRS cycle.
  2. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.

**Burst Sequence (Burst Length = 4)**

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

**Burst Sequence (Burst Length = 8)**

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

## Device Operations

### Clock (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between VIL and VIH. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set up and hold time around positive edge of the clock for proper functionality and ICC specifications.

### Clock Enable (CLK)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "tSS + 1 CLOCK" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

### Bank Select (BA0, BA1)

This SDRAM is organized as two independent banks of 4,194,304 words X 8 bits memory arrays. The BA0, BA1 inputs is latched at the time of assertion of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  to select the bank to be used for the operation. The bank select BA0, BA1 is latched at bank activate, read, write mode register set and precharge operations.

### Address Input (A0 ~ A11)

The 22 address bits required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A0~A11). The 12 bit row address is latched along with  $\overline{\text{RAS}}$ , BA0 and BA1 during bank activate command. The 9 bit column address is latched along with  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ , BA0 and BA1 during read or write command.

### NOP and Device Deselect

When  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting  $\overline{\text{CS}}$  high.  $\overline{\text{CS}}$  high disables the

command decoder so that  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$ , and all the address inputs are ignored.

### Power-Up

The following sequence is recommended for POWER UP

1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the inputs before or along with VDD (and VDDQ) supply. The clock signal must also be asserted at the same time.
2. After VDD reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of 2 Auto refresh cycles to stabilize the internal circuitry.
5. Perform a MODE REGISTER SET cycle to program the CAS latency, burst length and burst type as the default value of mode register is undefined. At the end of one clock cycle from the mode register set cycle, the device is ready for operation. When the above sequence is used for Power-up, all the out-puts will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence. (cf.) Sequence of 4 & 5 may be changed.

### Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of SDRAM. It programs the CAS latency, addressing mode, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11, BA0 and BA1 in the same cycle as  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  going low is the data written in the mode register. One clock cycle is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A0~A2, burst type uses A3, addressing mode uses A4~A6, A7~A8, A11, BA0 and BA1 are used for vendor specific options or test mode. And the write burst length is programmed using A9. A7~A8, A11, BA0 and BA1 must be set to low for normal SDRAM operation. Refer to table for specific codes for various burst length, addressing modes and CAS latencies.

## Device Operations (continued)

### Bank Activate

The bank activate command is used to select a random row in an idle bank. By asserting low on  $\overline{\text{RAS}}$  and  $\overline{\text{CS}}$  with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of  $t_{\text{RC}}(\text{min})$  from the time of bank activation.  $t_{\text{RC}}(\text{min})$  is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing  $t_{\text{RC}}(\text{min})$  with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies recover before the other bank can be sensed reliably.  $t_{\text{RRD}}(\text{min})$  specifies the minimum time required between activating different banks. The number of clock cycles required between different bank activation must be calculated similar to  $t_{\text{RC}}$  specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by  $t_{\text{RAS}}(\text{min})$  specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by  $t_{\text{RAS}}(\text{max})$ . The number of cycles for both  $t_{\text{RAS}}(\text{min})$  and  $t_{\text{RAS}}(\text{max})$  can be calculated similar to  $t_{\text{RC}}$  specification.

### Burst Read

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on  $\overline{\text{CS}}$  and  $\overline{\text{CAS}}$  with  $\overline{\text{WE}}$  being high on the positive edge of the clock. The bank must be active for at least  $t_{\text{RC}}(\text{min})$  before the burst read command is issued. The first output appears CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

### Burst Write

The burst write command is similar to burst read command, and is used to write data into the SDRAM consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on  $\overline{\text{CS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can not complete to burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank. The burst stop command is valid only at full page burst length where the writing continues at the end of burst and the burst is wrap around. The write burst can also be terminated by using DQM for blocking data and precharging the bank "trpL" after the last data input to be written into the active row. See DQM OPERATION also.

### DQM Operation

The DQM is used to mask input and output operation. It works similar to  $\overline{\text{OE}}$  during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in the read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock, therefore the masking occurs for a complete cycle. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required.

### Precharge

The precharge operation is performed on an active bank by asserting low on  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{WE}}$  and A10/AP with valid BA of the bank to be precharged. The precharge command can be asserted anytime after  $t_{\text{RAS}}(\text{min})$  is satisfied from the bank activate command in the desired bank. "trp" is defined as the minimum time required to precharge a bank. The minimum number of clock cycles required to complete row precharge is calculated by dividing "trp" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by  $t_{\text{RAS}}(\text{max})$ . Therefore, each bank has to be precharged within  $t_{\text{RAS}}(\text{max})$  from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc, is possible only when both banks are in idle state.

## Device Operations (continued)

### Auto Precharge

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy  $t_{RAS}(min)$  and " $t_{RP}$ " for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A10/AP. If burst read or burst write command is issued with low on A10/AP, the bank is left active until a new command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

### Four Banks Precharge

Both banks can be precharged at the same time by using Precharge all command. Asserting low on  $\overline{CS}$ ,  $\overline{RAS}$  and  $\overline{WE}$  with high on A10/AP after both banks have satisfied  $t_{RAS}(min)$  requirement, performs precharge on both banks. At the end of  $t_{RP}$  after performing precharge all, both banks are in idle state.

### Auto Refresh

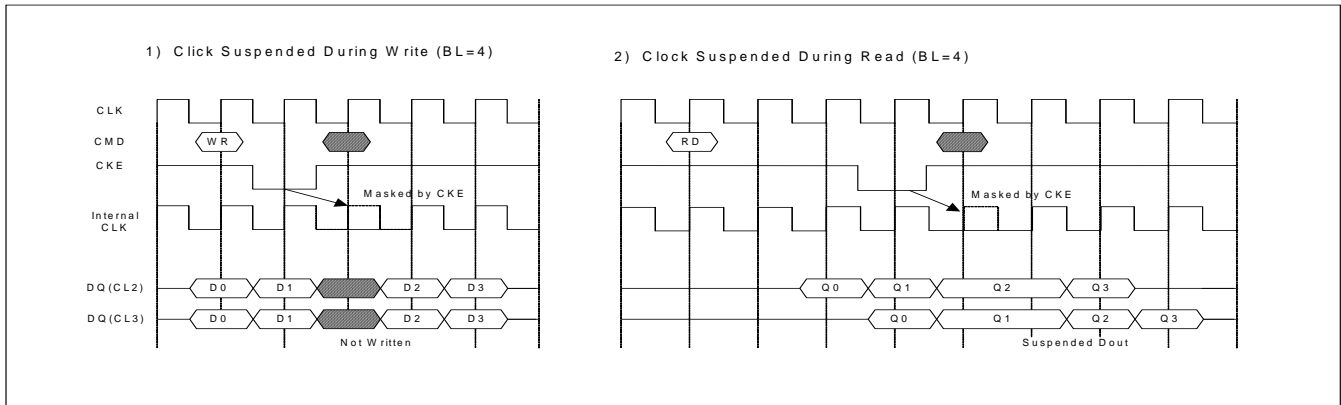
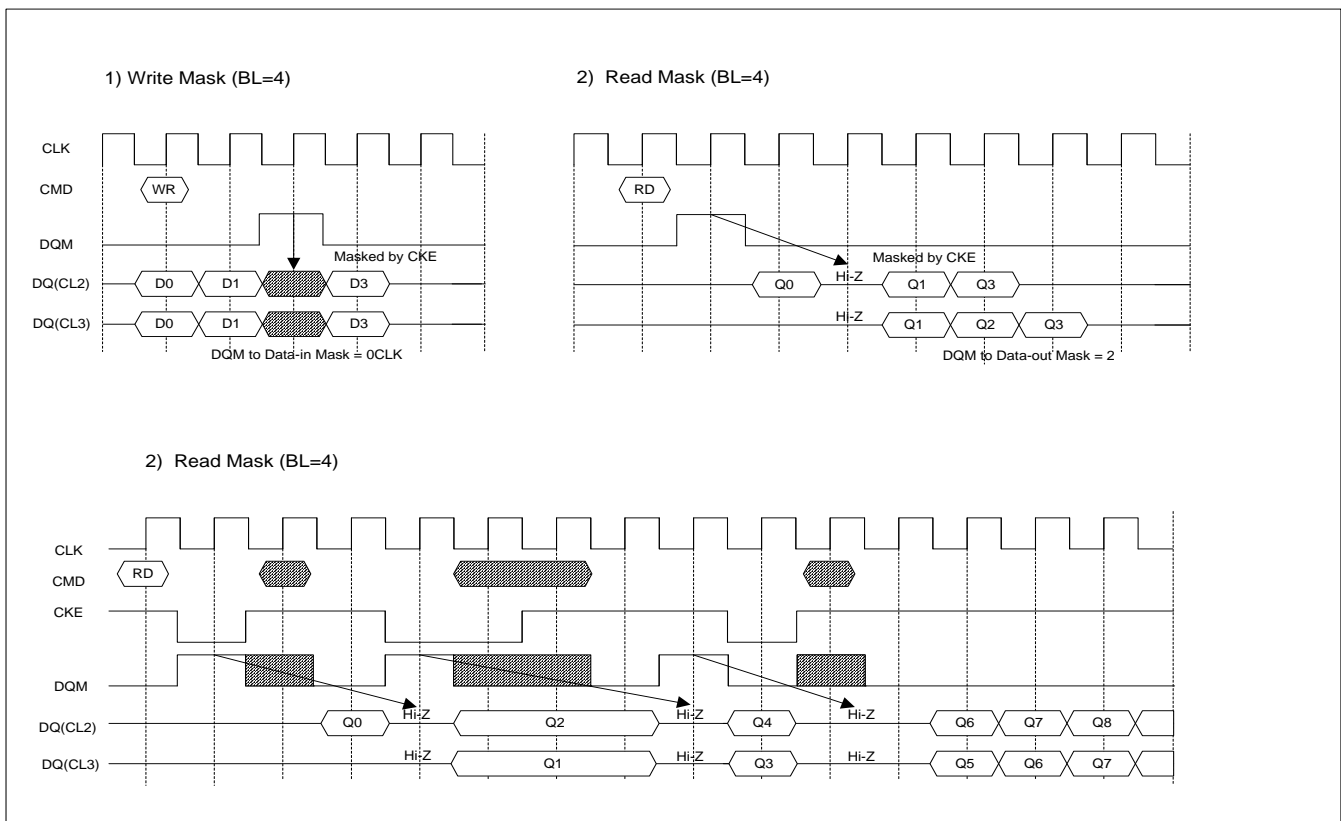
The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$  and  $\overline{CAS}$  with high on CKE and  $\overline{WE}$ . The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time

required to complete the auto refresh operation is specified by " $t_{rc}(min)$ ". The minimum number of clock cycles required can be calculated by driving " $t_{rc}$ " with clock cycle time and then rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6 $\mu$ s or a burst of 4096 auto refresh cycles once in 64ms.

### Self Refresh

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and CKE with high on  $\overline{WE}$ . Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.

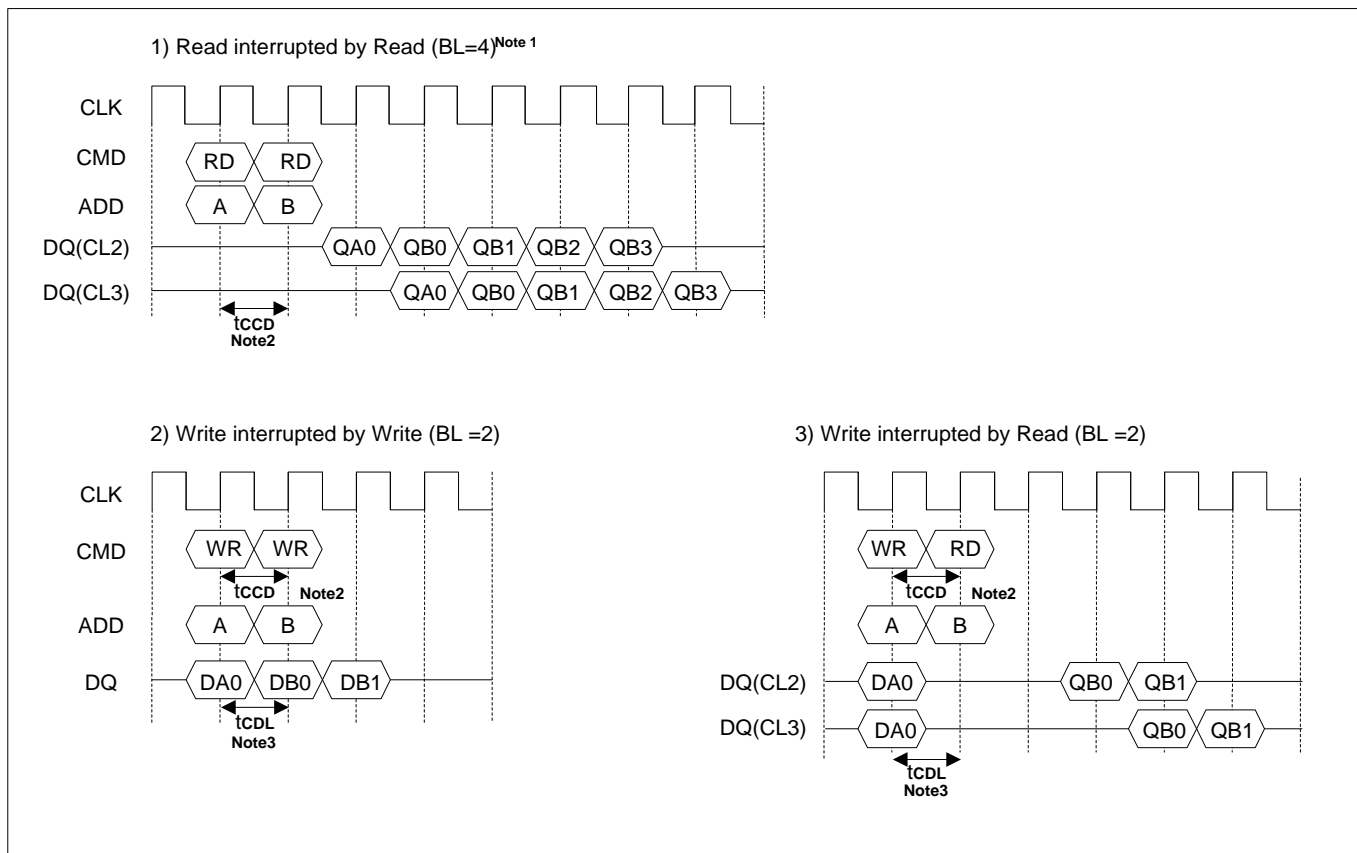
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of " $t_{rc}$ " before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

**Basic feature And Function Descriptions**
**1. CLOCK Suspend**

**2. DQM Operation**


- \* **Note** : 1. DQM makes data out Hi-Z after 2 clocks which should be masked by CKE "L".
- 2. DQM masks both data-in and data-out.



### 3. CAS Interrupt (I)

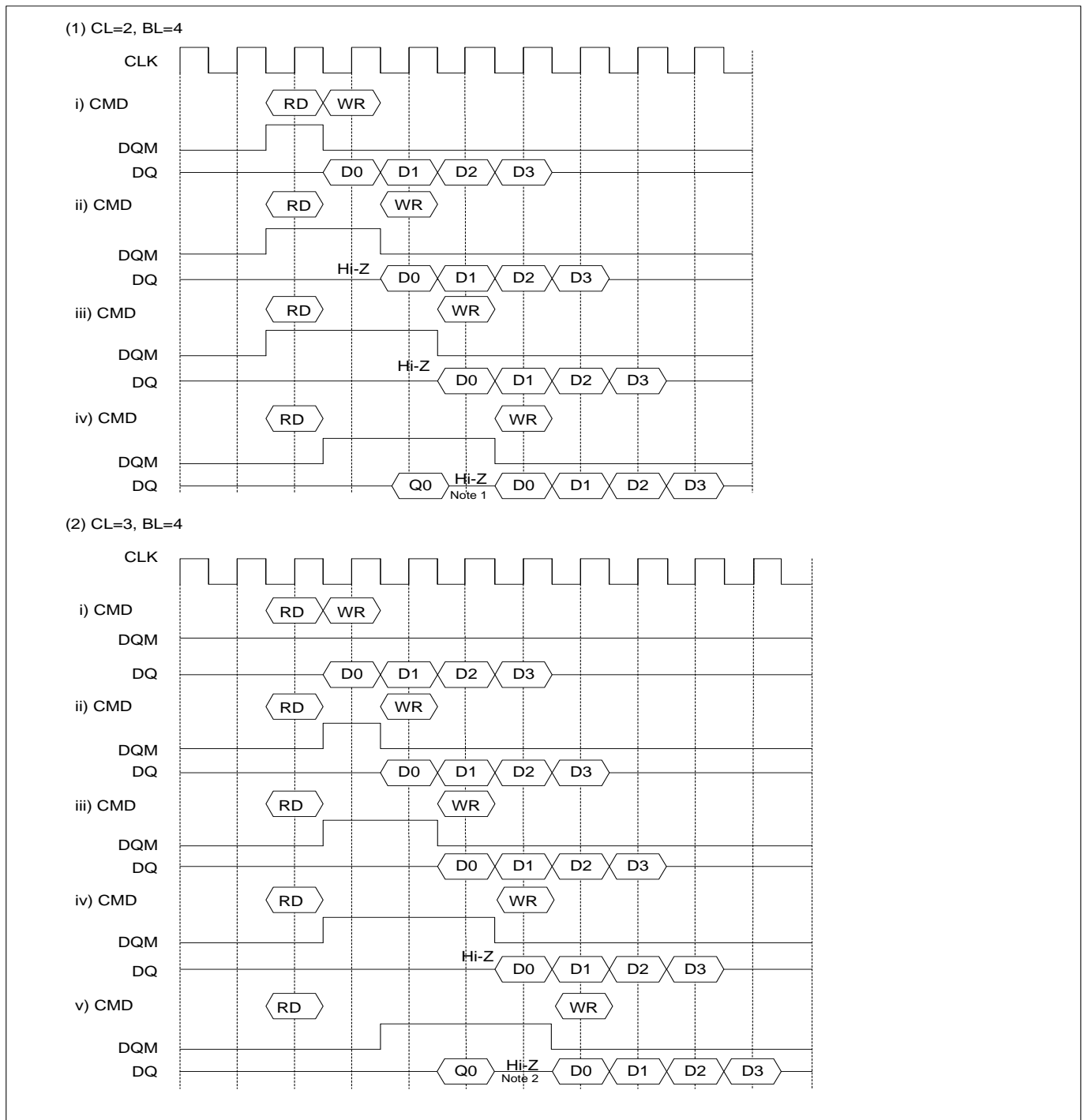


Note : 1. By "Interrupt", It is possible to stop burst read/write by external command before the end of burst.

By "CAS Interrupt", to stop burst read/write by  $\overline{\text{CAS}}$  access; read, write and block write.

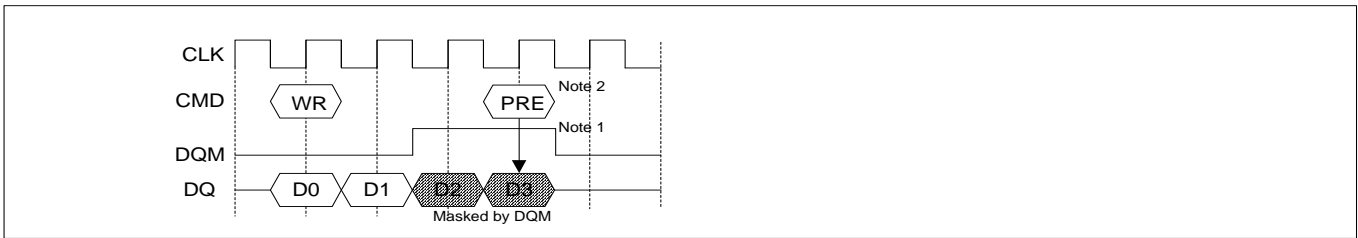
2.  $t_{CCD}$  :  $\overline{\text{CAS}}$  to  $\overline{\text{CAS}}$  delay. (=1CLK)

3.  $t_{CDL}$  : Last data in new column address delay. (= 1CLK).

**4. CAS Interrupt (II) : Read Interrupted Write & DQM**


\* Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.  
 2. To prevent bus contention, DQM should be issued which makes a least one gap between data in and data out.

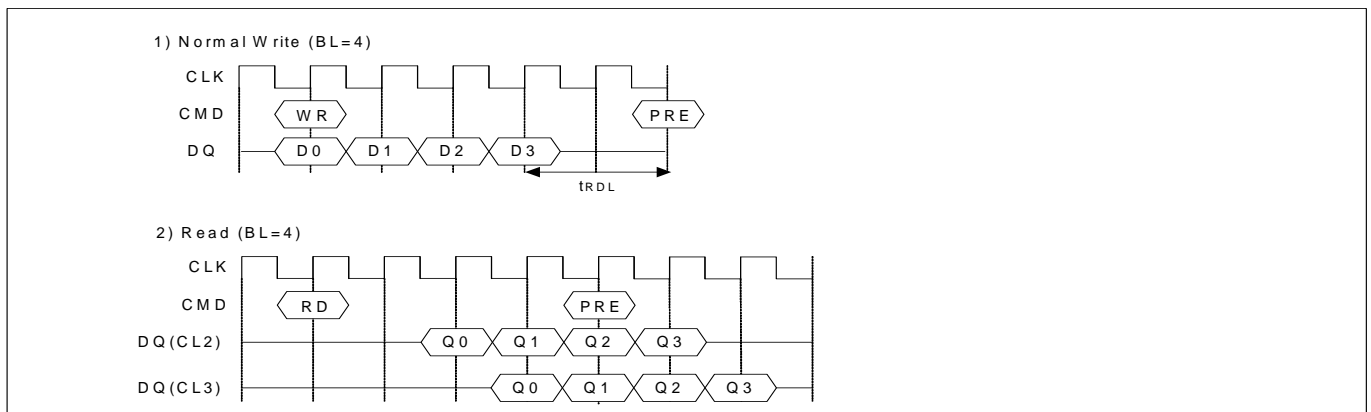
### 5. Write Interrupted by Precharge & DQM



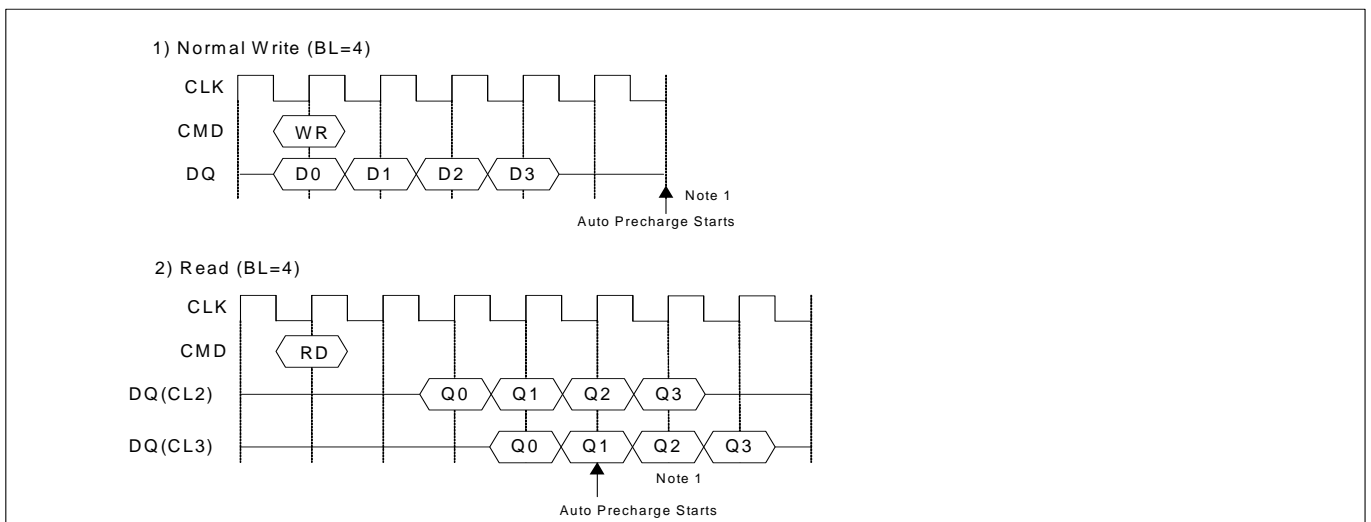
Note : 1. To inhibit invalid write, DQM should be issued.

2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual banks operation.

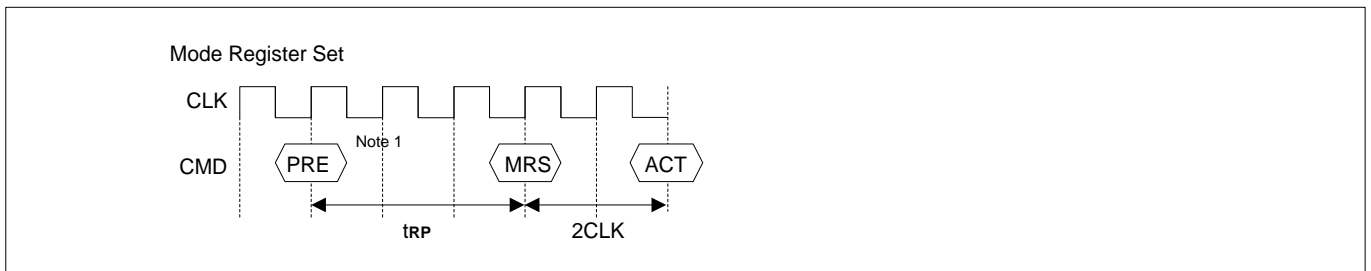
### 6. Precharge



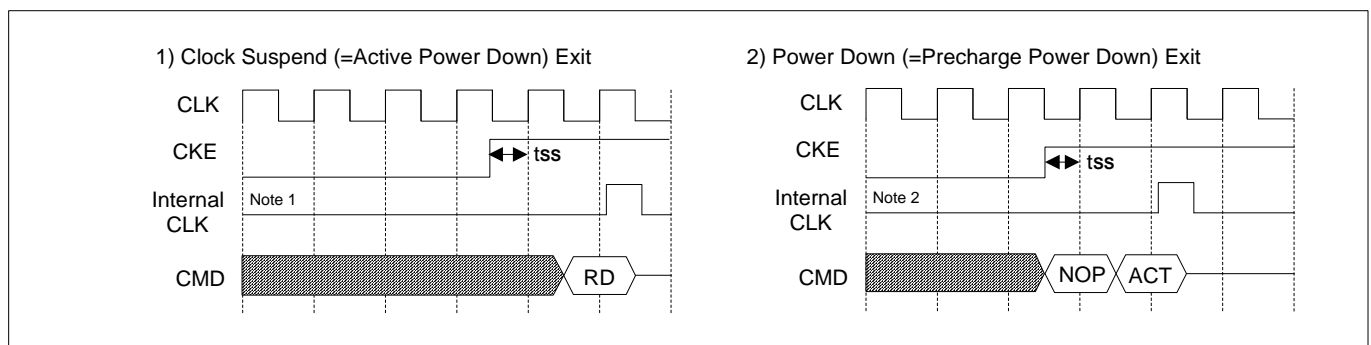
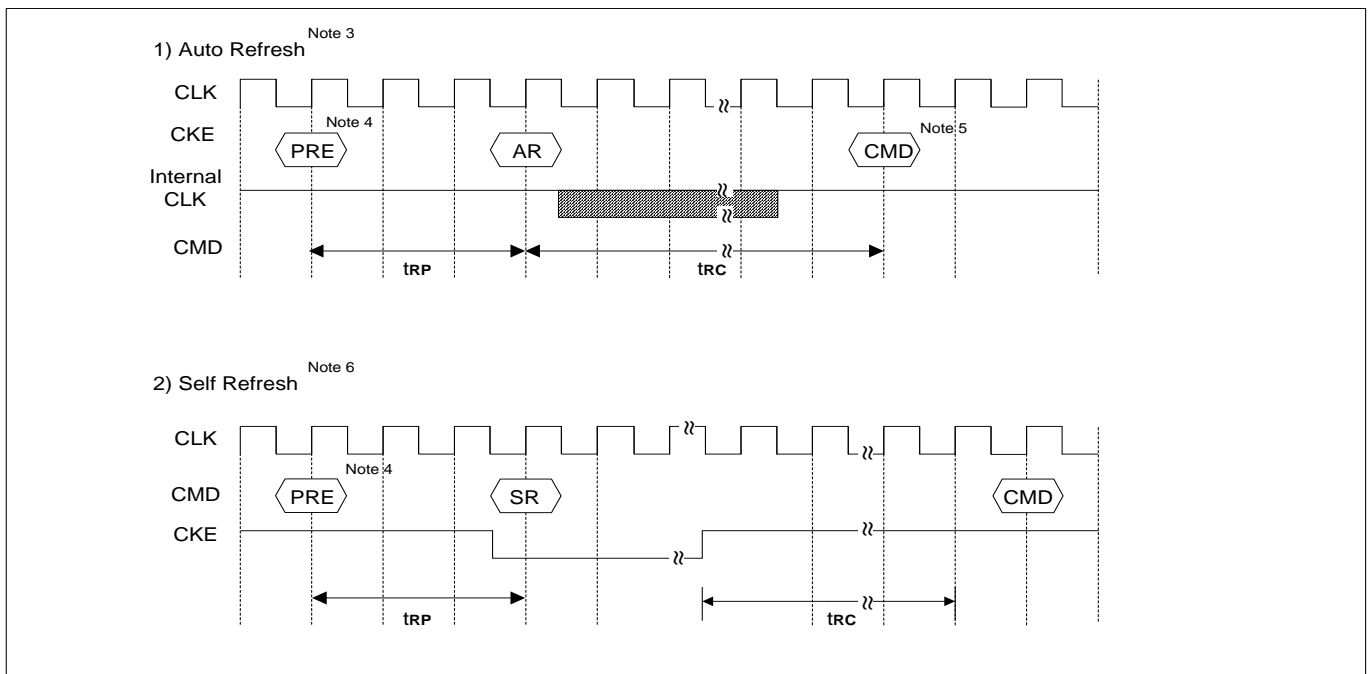
### 7. Auto Precharge



\* Note : 1. The row active command of the precharge bank can be issued after  $t_{RP}$  from this point.  
 The new read/write command of other active bank can be issued from this point.  
 At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

**8. MRS**


**Note :** 1. PRE : Both banks precharge if necessary.  
MRS can be issued only at all bank precharge state.

**9. Clock Suspend Exit & Power Down Exit**

**10. Auto Refresh & Self Refresh**


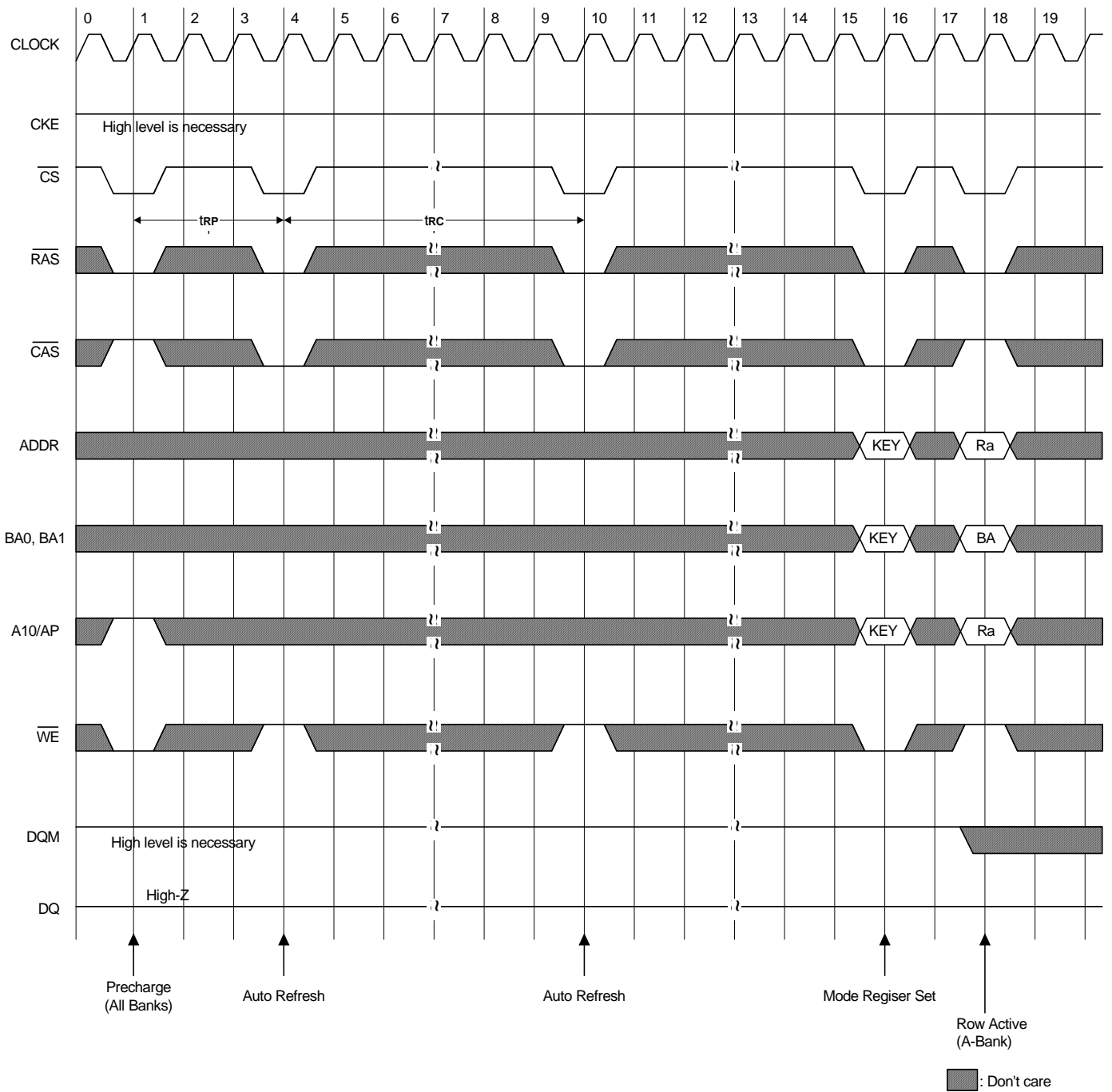
- \* Note :
1. Active power down : one or more bank active state.
  2. Precharge power down : both bank precharge state.
  3. The auto refresh is the same as CBR refresh of conventional DRAM.  
No precharge commands are required after Auto Refresh command.  
During  $t_{RC}$  from auto refresh command, any other command can not be accepted.
  4. Before executing auto/self refresh command, both banks must be idle state.
  5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
  6. During self refresh mode, refresh interval and refresh operation are performed internally.  
After self refresh entry, self refresh mode is kept while CKE is LOW.  
During self refresh mode, all inputs except CKE will be don't cared, and outputs will be in Hi-Z state.  
During self refresh exit command, any other command can not be accepted.  
Before/After self refresh mode, burst auto refresh cycle (4K cycles ) is recommended.

### 11. About Burst Type Control

Basic MODE	Sequential counting	At MRS A3="0". See the BURST SEQUENCE TABE.(BL=4,8) BL=1,2,4,8 and full page wrap around.
	Interleave counting	At MRS A3=" 1". See the BURST SEQUENCE TABE.(BL=4,8) BL=4,8 At BL=1,2 Interleave Counting = Sequential Counting
Random MODE	Random column Access $t_{CCD} = 1 \text{ CLK}$	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of convention DRAM.

### 12. About Burst Length Control

Basic MODE	1	At MRS A2,1,0 = "000". At auto precharge, $t_{RAS}$ should not be violated.
	2	At MRS A2,1,0 = "001". At auto precharge, $t_{RAS}$ should not be violated.
	4	At MRS A2,1,0 = "010"
	8	At MRS A2,1,0 = "011".
Special MODE	BRSW	At MRS A9="1". Read burst = 1,2,4,8, full page/write Burst =1 At auto precharge of write, $t_{RAS}$ should not be violated.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank Stops read/write burst with Row precharge. $t_{RD}$ =1 with DQM, valid DQ after burst stop is 1,2 for CL=2,3 respectively During read/write burst with auto precharge, $\overline{RAS}$ interrupt cannot be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

**Power On Sequence & Auto Refresh**




- \* Note : 1. All inputs can be don't care when  $\overline{CS}$  is high at the CLK high going edge.  
 2. Bank active & read/write are controlled by BA0, BA1.

BA1	BA0	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

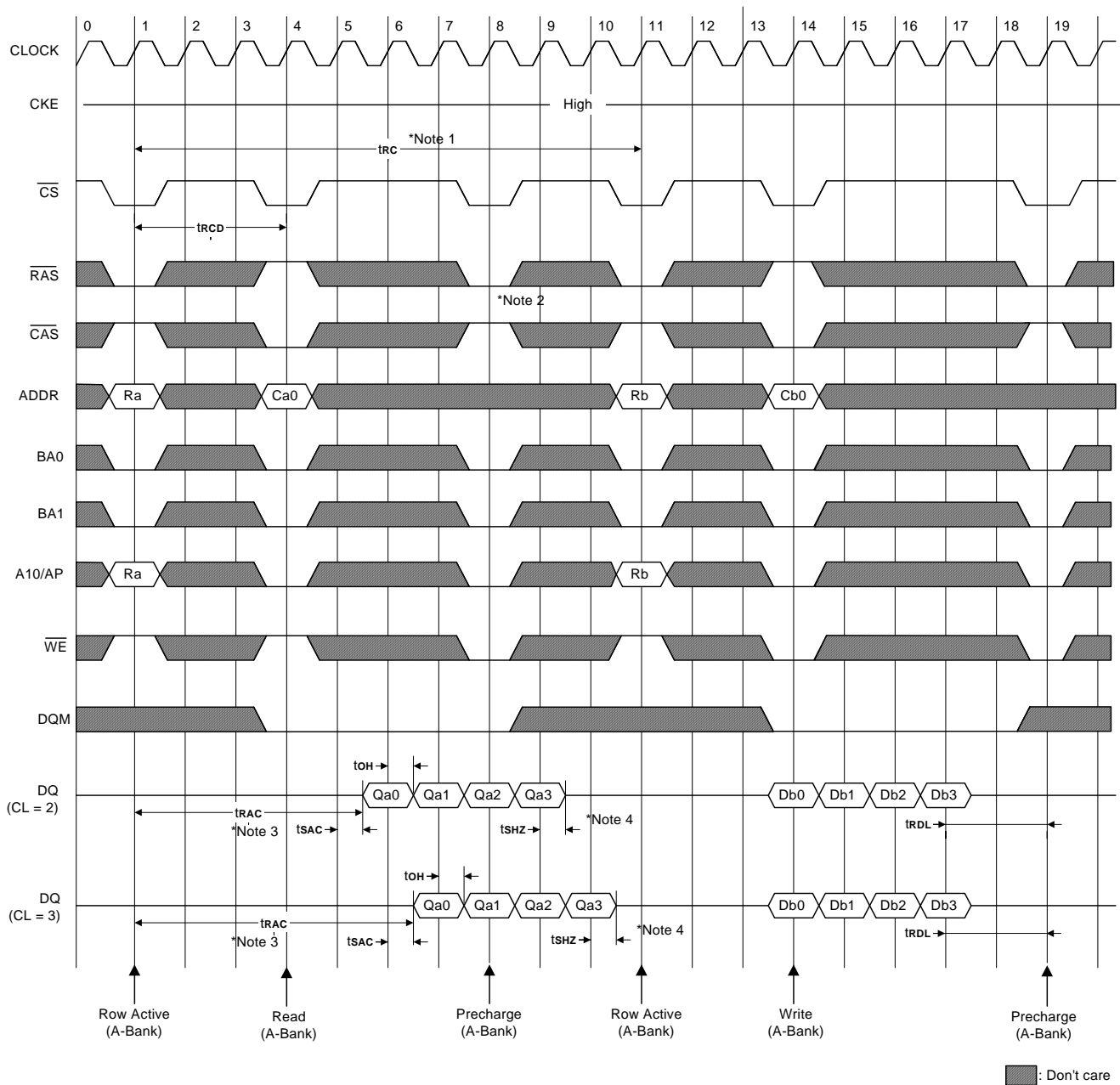
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA1	BA0	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

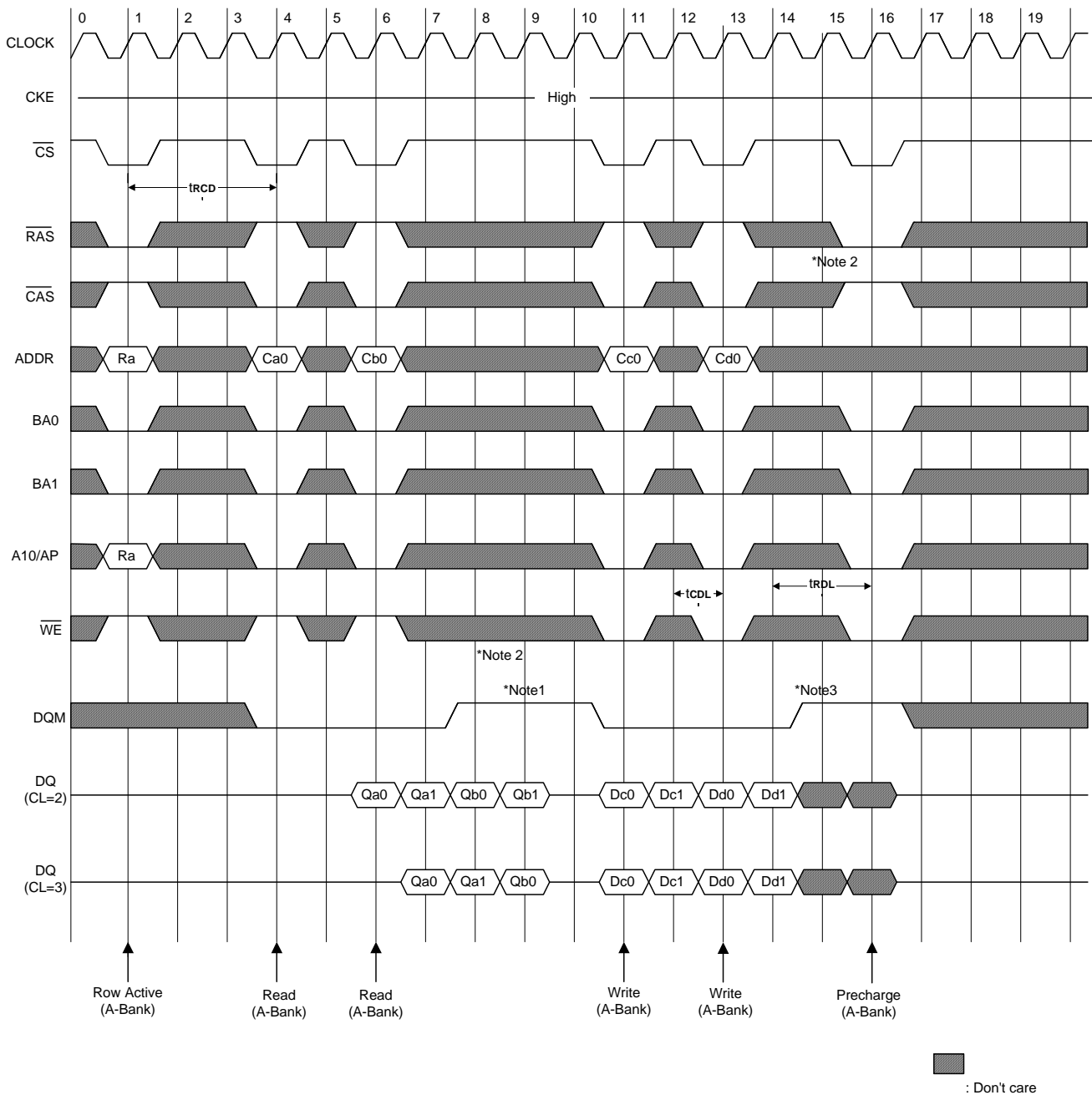
4. A10/AP and BA0, BA1 control bank precharge when precharge command is asserted.

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

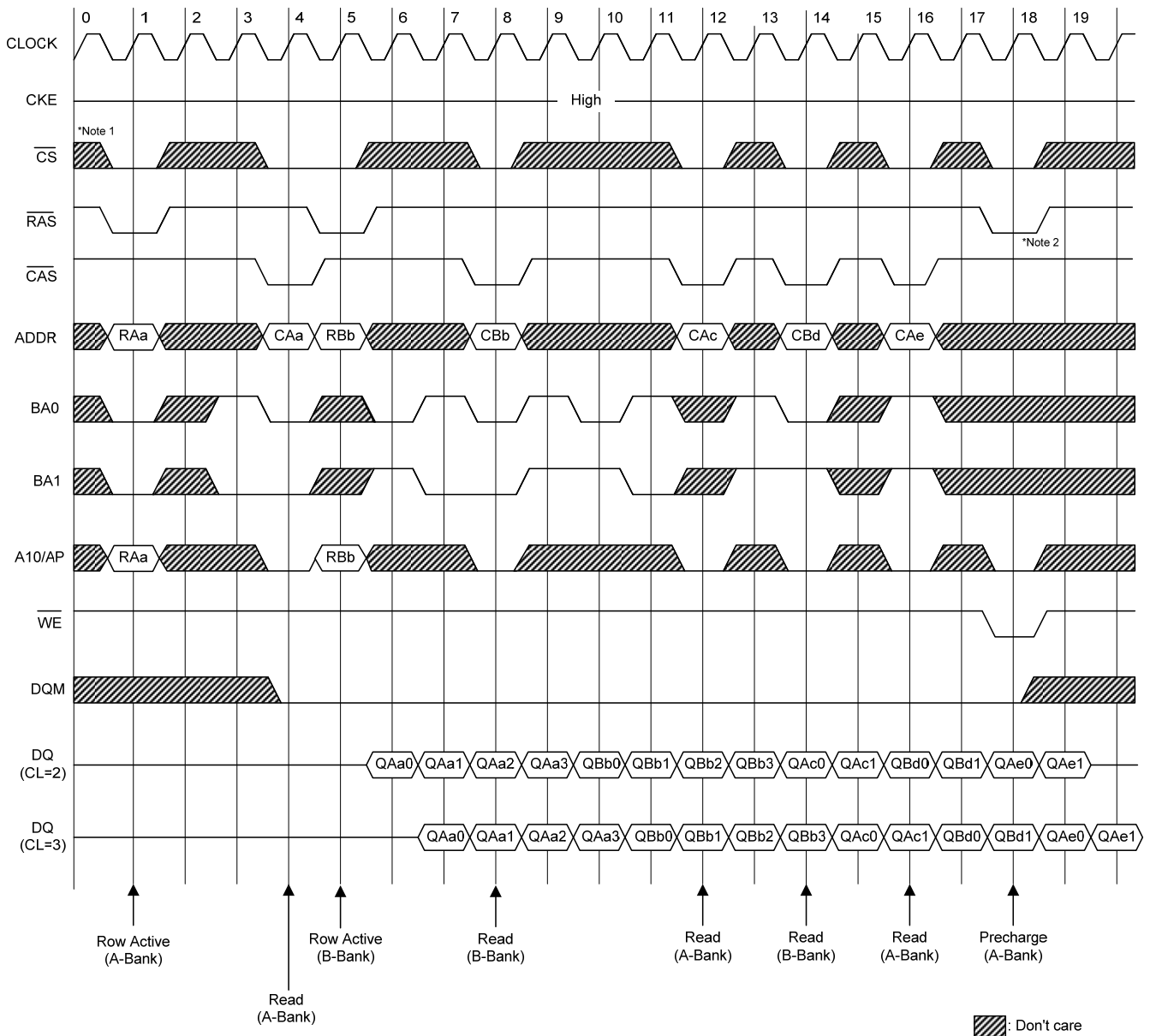


**Read & Write Cycle at Same Bank @Burst Length=4**


- \*Note :**
1. Minimum row cycle times is required to complete internal DRAM operation.
  2. Row precharge can interrupt burst on any cycle. [CAS latency-1] valid output data available after Row enters precharge. Last valid output will be Hi-Z after  $t_{SHZ}$  from the clock.
  3. Access time from Row address.  $t_{CC}^*(t_{RCD} + \text{CAS latency}-1) + t_{sAC}$
  4. Output will be Hi-Z after the end of burst. (1,2,4 & 8)

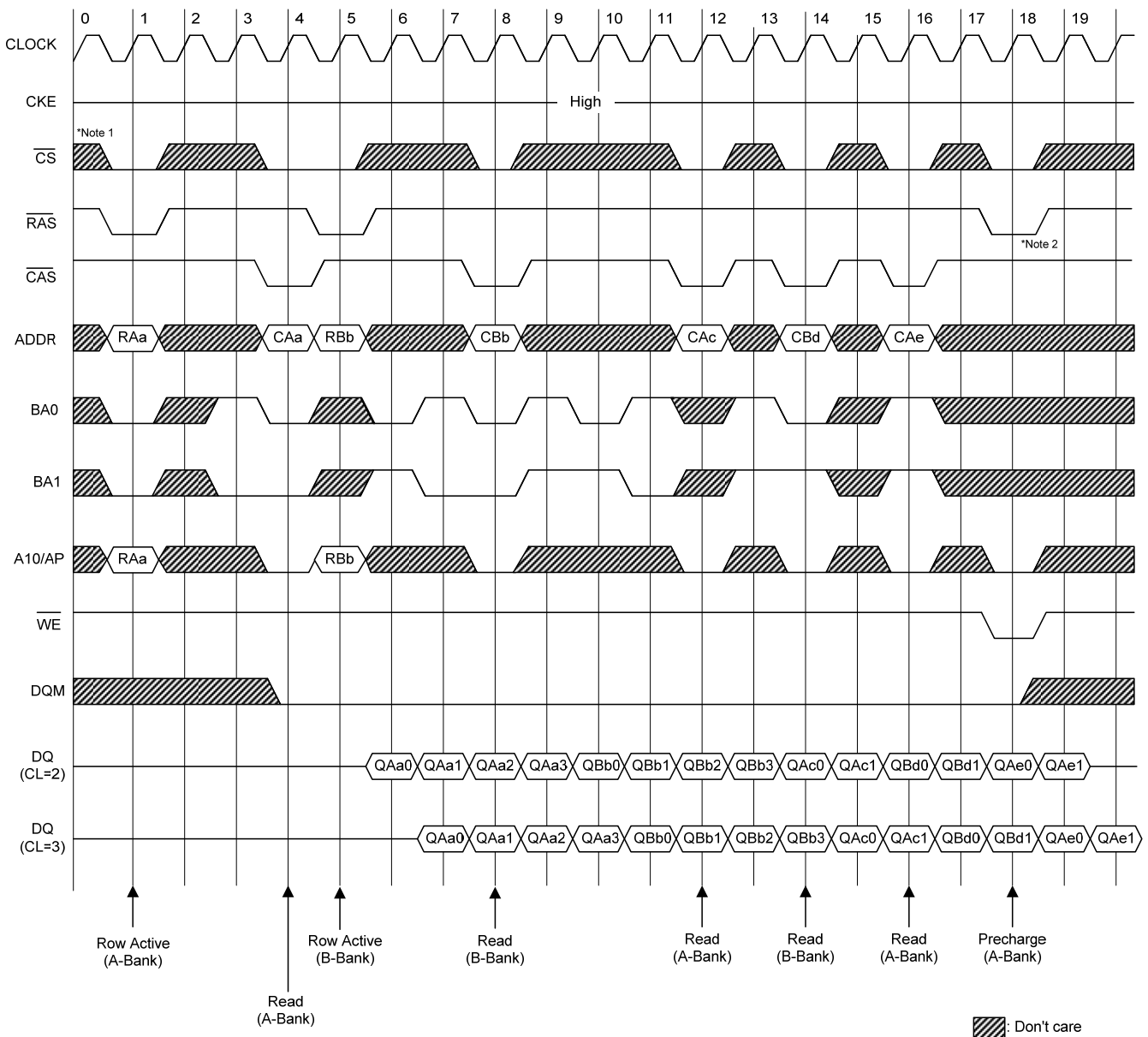
**Page Read & Write Cycle at Same Bank @Burst Length=4**


- \*Note :**
1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
  2. Row precharge will interrupt writing. Last data input,  $t_{rDL}$  before Row precharge, will be written.
  3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

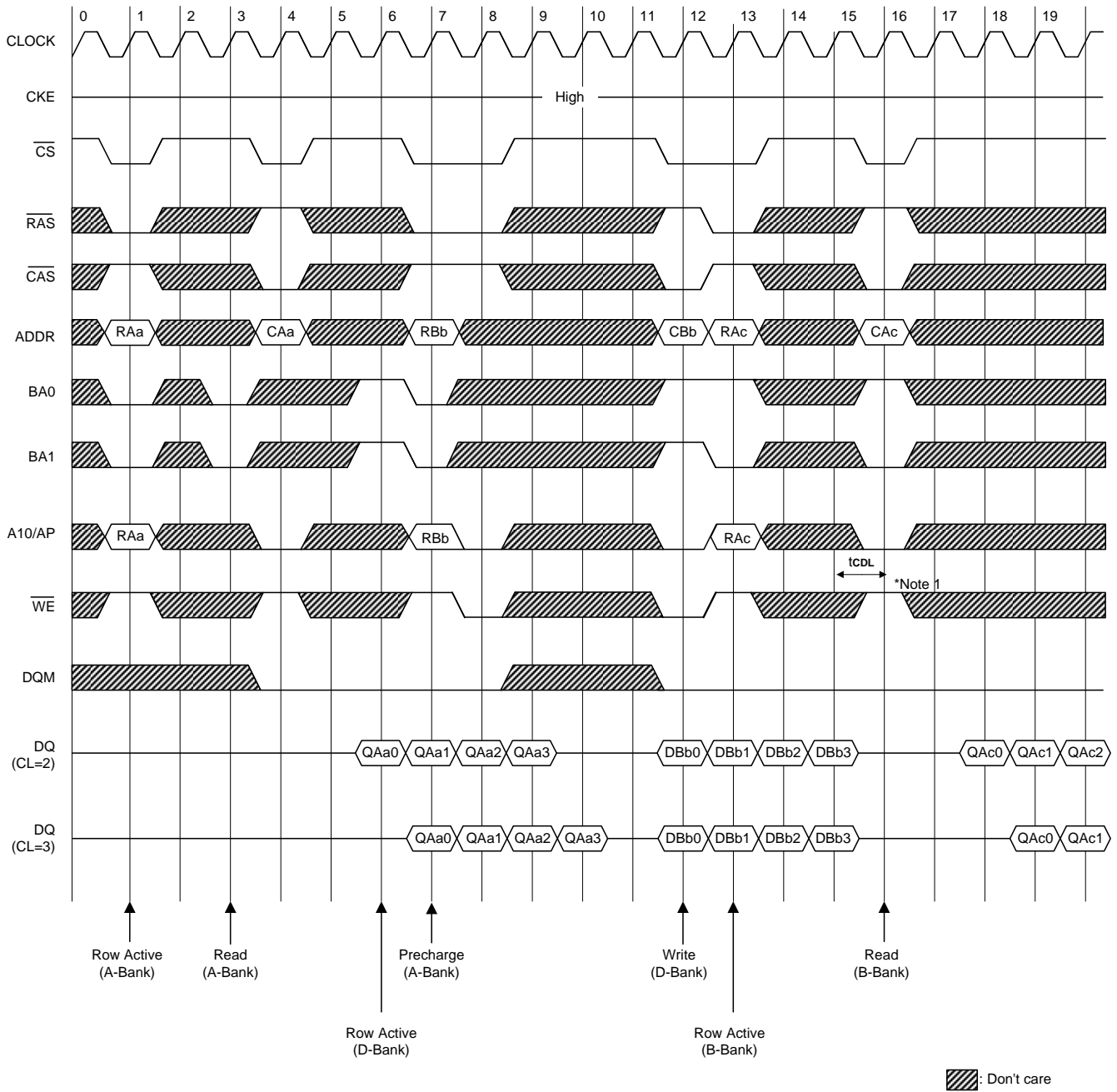
**Page Read Cycle at Different Bank @Burst Length = 4**


\* Note : 1.  $\overline{CS}$  can be don't care when  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  are high at the clock high going edge.

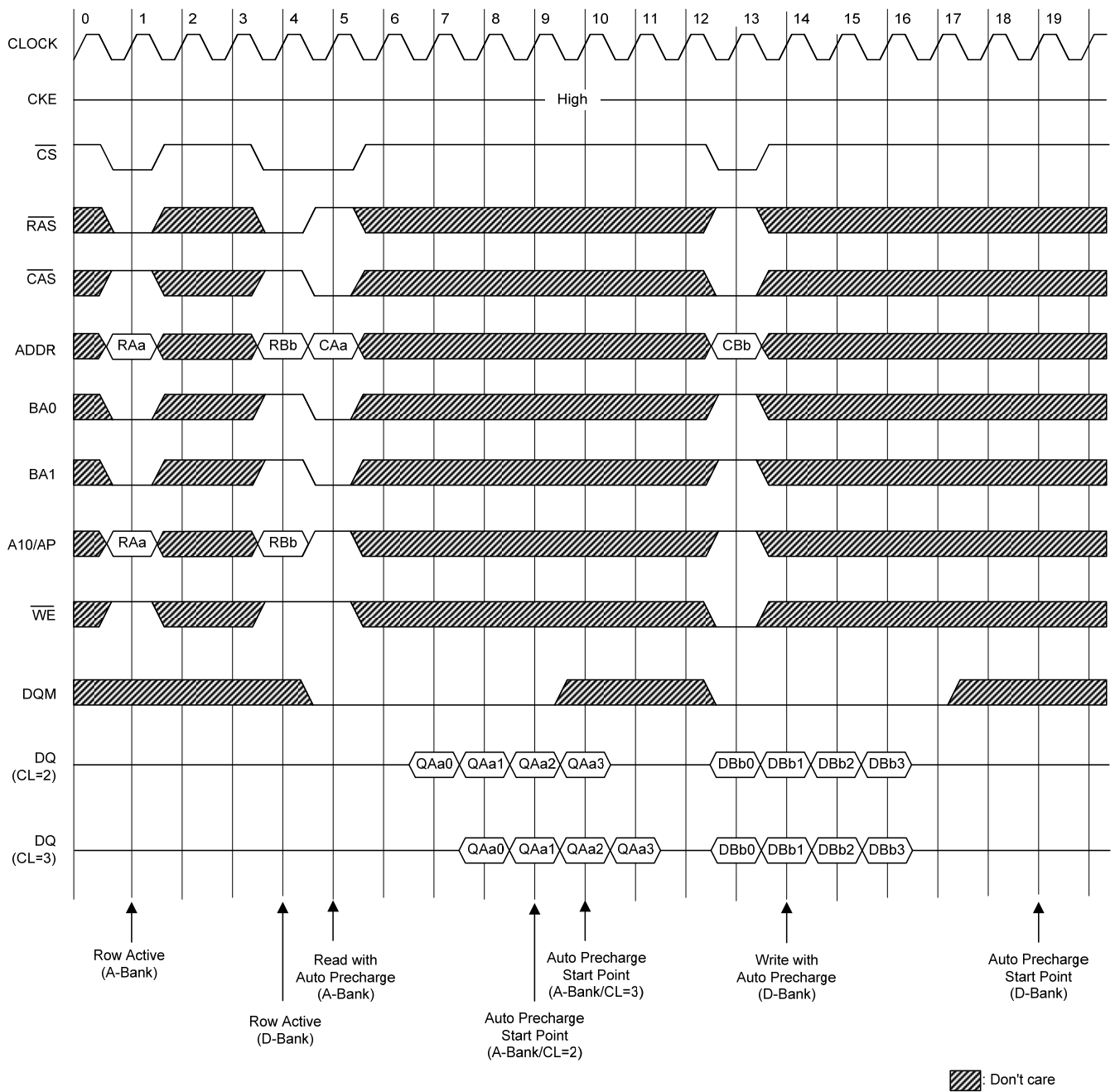
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

**Page Write Cycle at Different Bank @Burst Length=4**

**\* Note:**

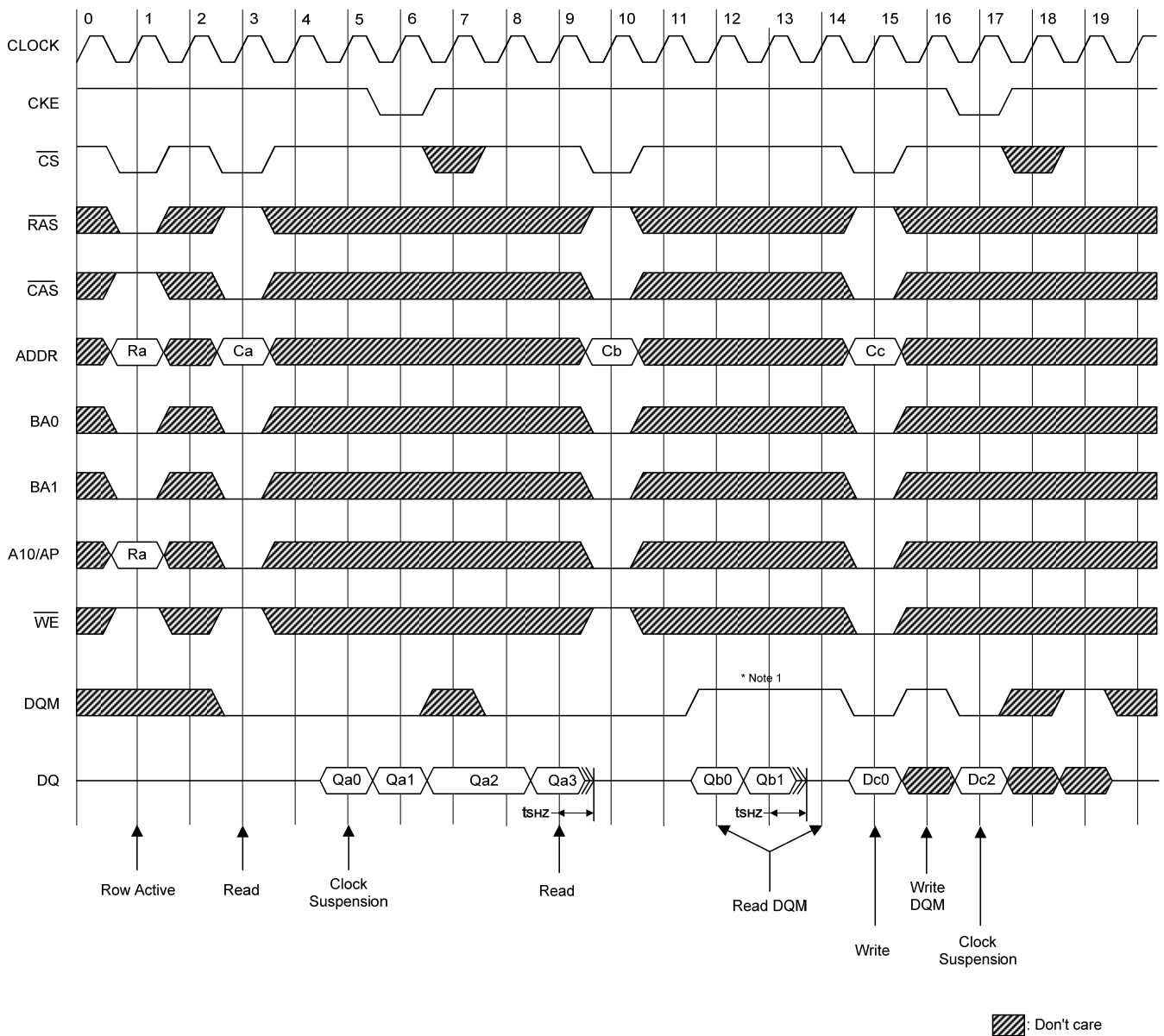
1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and precharge banks must be the same.

**Read & Write Cycle at Different Bank @Burst Length=4**


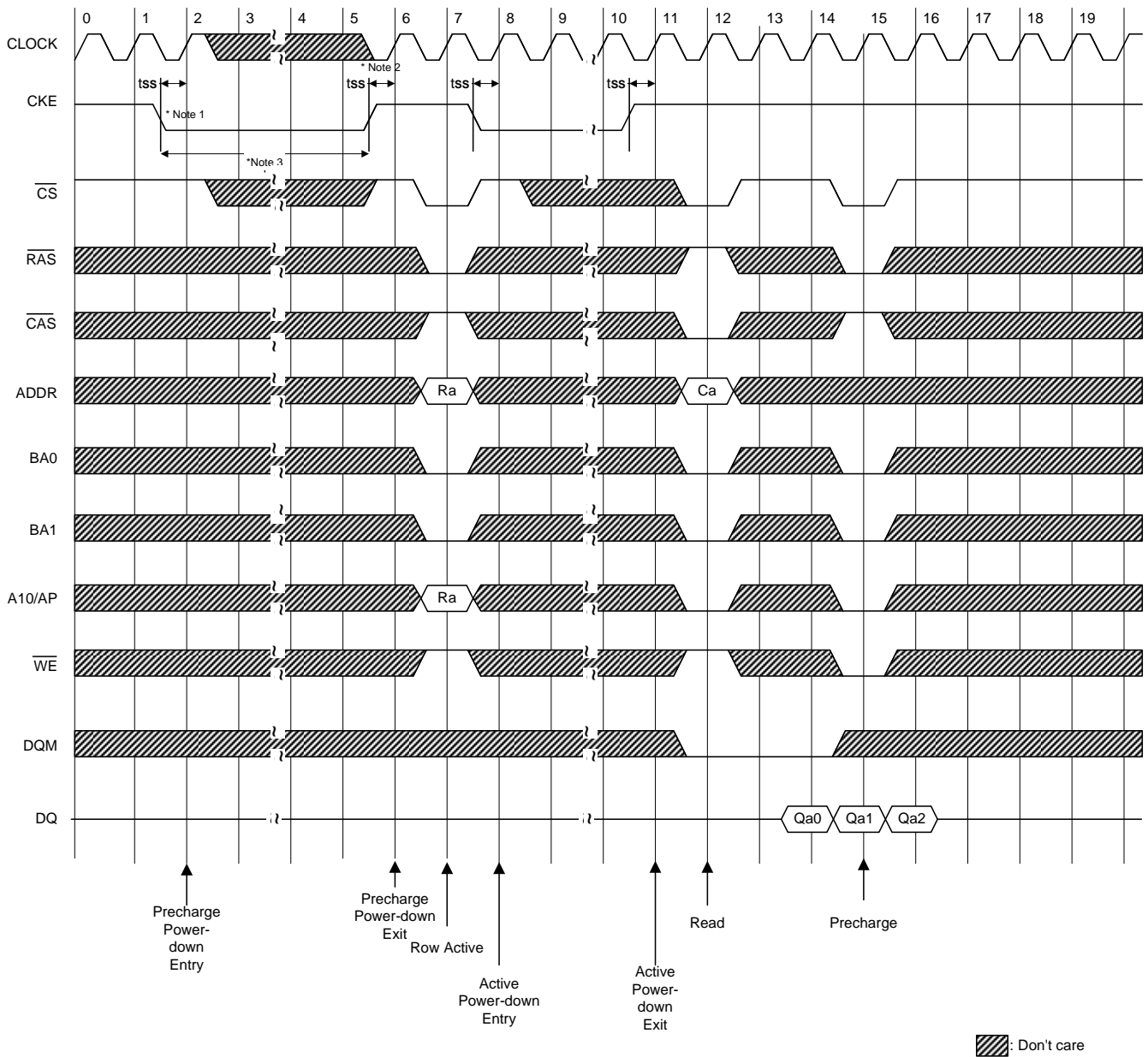
\* Note : tcDL should be met to complete write.

**Read & Write Cycle with Auto Precharge @Burst Length=4**


\*Note : tRCD should be controlled to meet minimum tRAS before internal precharge start.  
(In the case of Burst Length=1 & 2, BRSW mode)

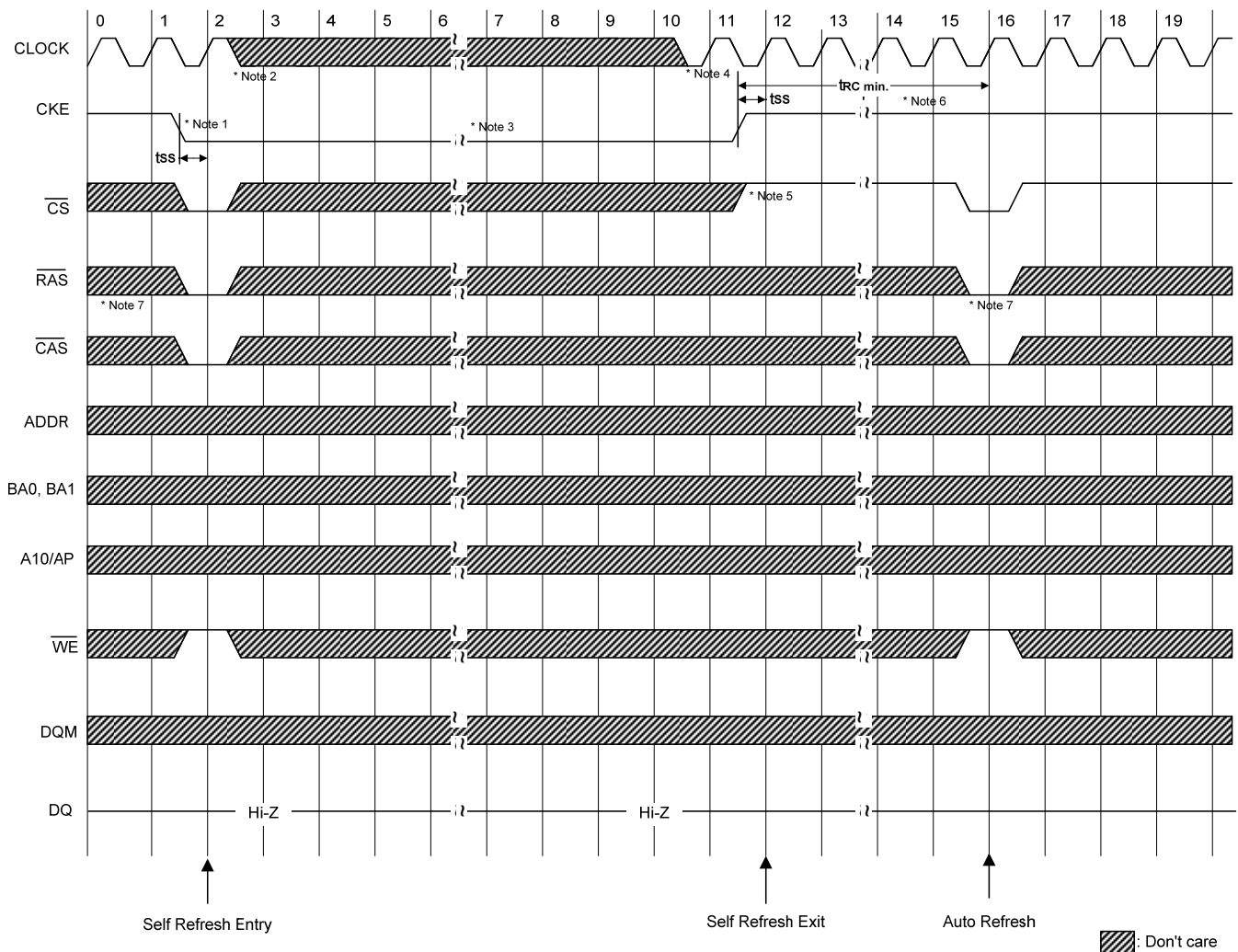
**Clock Suspension & DQM Operation Cycle @CAS Latency = 2, Burst Length=4**


\* Note : DQM needed to prevent bus contention.

**Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4**


- \* Note : 1. All banks should be in idle state prior to entering precharge power down mode.  
 2. CKE should be set high at least "1CLK + tss" prior to Row active command.  
 3. Cannot violate minimum refresh specification. (64ms)

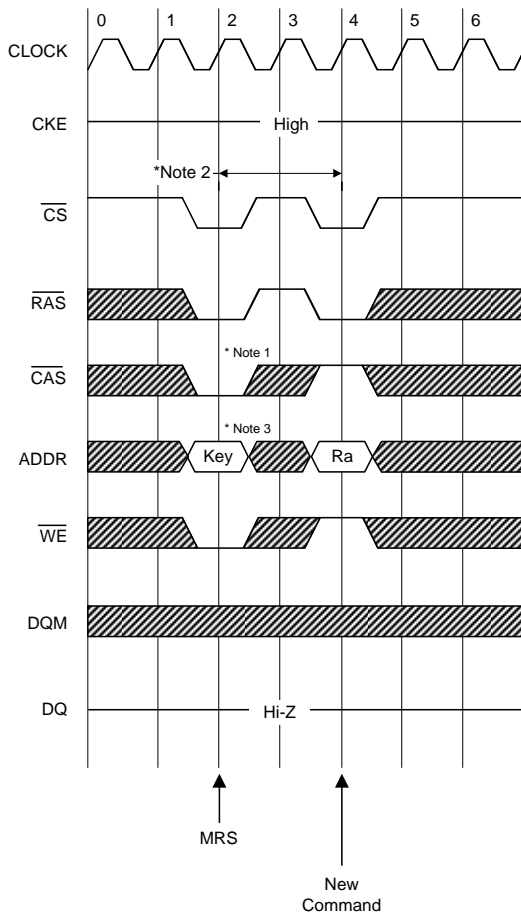
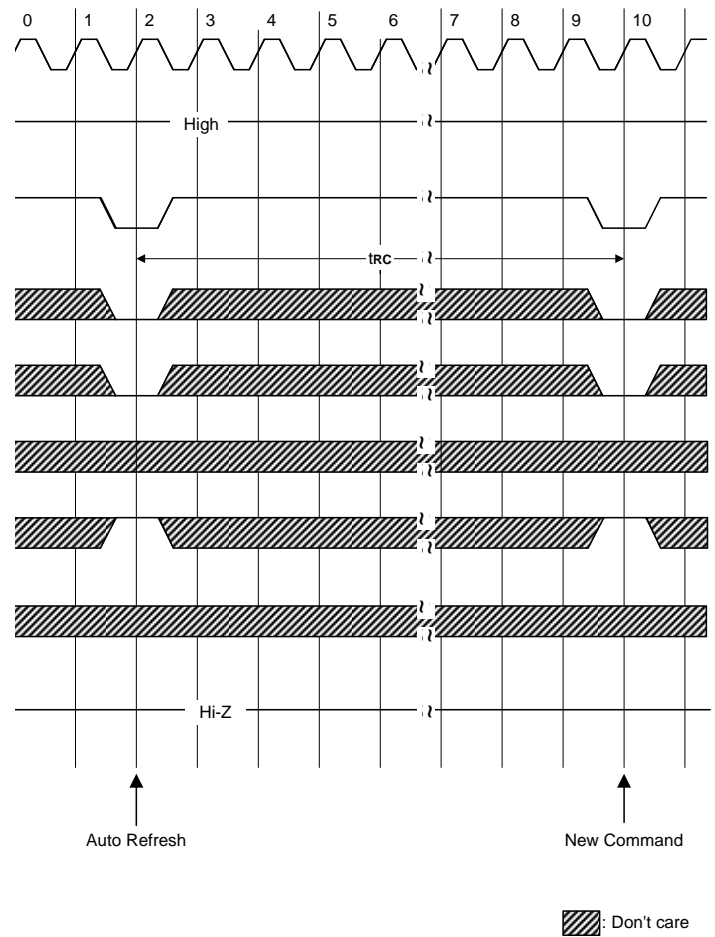


**Self Refresh Entry & Exit Cycle**

**\* Note : TO ENTER SELF REFRESH MODE**

1.  $\overline{CS}$ ,  $\overline{RAS}$  &  $\overline{CAS}$  with  $\overline{CKE}$  should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for  $\overline{CKE}$ .
3. The device remains in self refresh mode as long as  $\overline{CKE}$  stays "Low".  
(cf.) Once the device enters self refresh mode, minimum  $t_{RAS}$  is required before exit from self refresh.

**TO EXIT SELF REFRESH MODE**

4. System clock restart and be stable before returning  $\overline{CKE}$  high.
5.  $\overline{CS}$  starts from high.
6. Minimum  $t_{RC}$  is required after  $\overline{CKE}$  going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit.  
If the system uses burst refresh.

**Mode Register Set Cycle**

**Auto Refresh Cycle**


\* Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

**MODE REGISTER SET CYCLE**

- \* Note : 1.  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  &  $\overline{WE}$  activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new  $\overline{RAS}$  activation.
  3. Please refer to Mode Register Set table.

**Function Truth Table (Table 1)**

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	Address	Action	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row Active; Latch Row Address	
	L	L	H	L	BA	PA	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP Code		Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA,A10/AP	Begin Read; Latch CA; Determine AP	
	L	H	L	L	BA	CA,A10/AP	Begin Write; Latch CA; Determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	PA	Precharge	
Read	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	H	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	L	X	X	Term burst →Row Active	
	L	H	L	H	BA	CA,A10/AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	L	BA	CA,AP	Term burst; Begin Write; Latch CA; Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
Write	L	L	H	L	BA	PA	Term Burst; Precharge timing for Reads	3
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	H	X	X	NOP(Continue Burst to End →Row Active)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	BA	CA,A10/AP	Term burst; Begin Read; Latch CA; Determine AP	3
	L	H	L	L	BA	CA,A10/AP	Term burst; Begin Read; Latch CA; Determine AP	3
Read with Auto Precharge	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term Burst; Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP(Continue Burst to End →Precharge)	
	L	H	H	H	X	X	NOP(Continue Burst to End →Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	BA	CA,A10/AP	ILLEGAL	2
	L	H	L	L	BA	CA,A10/AP	ILLEGAL	2
	L	L	H	X	BA	RA, PA	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	2

**Function Truth Table (Table 1, Continued)**

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	Address	Action	Note
Write with Auto Precharge	H	X	X	X	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	H	X	X	NOP(Continue Burst to End→Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	H	BA	CA,A10/AP	ILLEGAL	2
	L	H	L	L	BA	CA,A10/AP	ILLEGAL	2
	L	L	H	X	BA	RA, PA	ILLEGAL	
Precharge	L	L	L	X	X	X	ILLEGAL	2
	H	X	X	X	X	X	NOP→Idle after $t_{RP}$	
	L	H	H	H	X	X	NOP→Idle after $t_{RP}$	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA,A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
Row Activating	L	L	H	L	BA	PA	NOP→Idle after $t_{RP}$	2
	L	L	L	X	X	X	ILLEGAL	4
	H	X	X	X	X	X	NOP→Row Active after $t_{rCD}$	
	L	H	H	H	X	X	NOP→Row Active after $t_{rCD}$	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA,A10/AP	ILLEGAL	2
Refreshing	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	PA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	2
	H	X	X	X	X	X	NOP→Idle after $t_{rc}$	
	L	H	H	X	X	X	NOP→Idle after $t_{rc}$	
	L	L	H	X	X	X	ILLEGAL	
Refreshing	L	L	L	X	X	X	ILLEGAL	

**Abbreviations**

RA = Row Address

BA = Bank Address

AP = Auto Precharge

NOP = No Operation Command

CA = Column Address

PA = Precharge All

Note: 1. All entries assume that CKE was active (High) during the preceding clock cycle and the current clock cycle.

2. Illegal to bank in specified state: Function may be legal in the bank indicated by BA, depending on the state of that bank.

3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and PA).

5. Illegal if any banks is not idle.

**Function Truth Table for CKE (Table 2)**

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh→ABI after $t_{rc}$	6
	L	H	L	H	H	H	X	Exit Self Refresh→ABI after $t_{rc}$	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP(Maintain Self Refresh)	
Both Bank Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down→ABI	7
	L	H	L	H	H	H	X	Exit Power Down→ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP(Maintain Power Down Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	X	X	ILLEGAL	
	H	L	L	L	L	H	X	Enter Self Refresh	8
	L	L	L	L	L	L	X	ILLEGAL	
Any State Other than Listed Above	L	L	X	X	X	X	X	NOP	
	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain clock Suspend	

Abbreviations : ABI = All Banks Idle

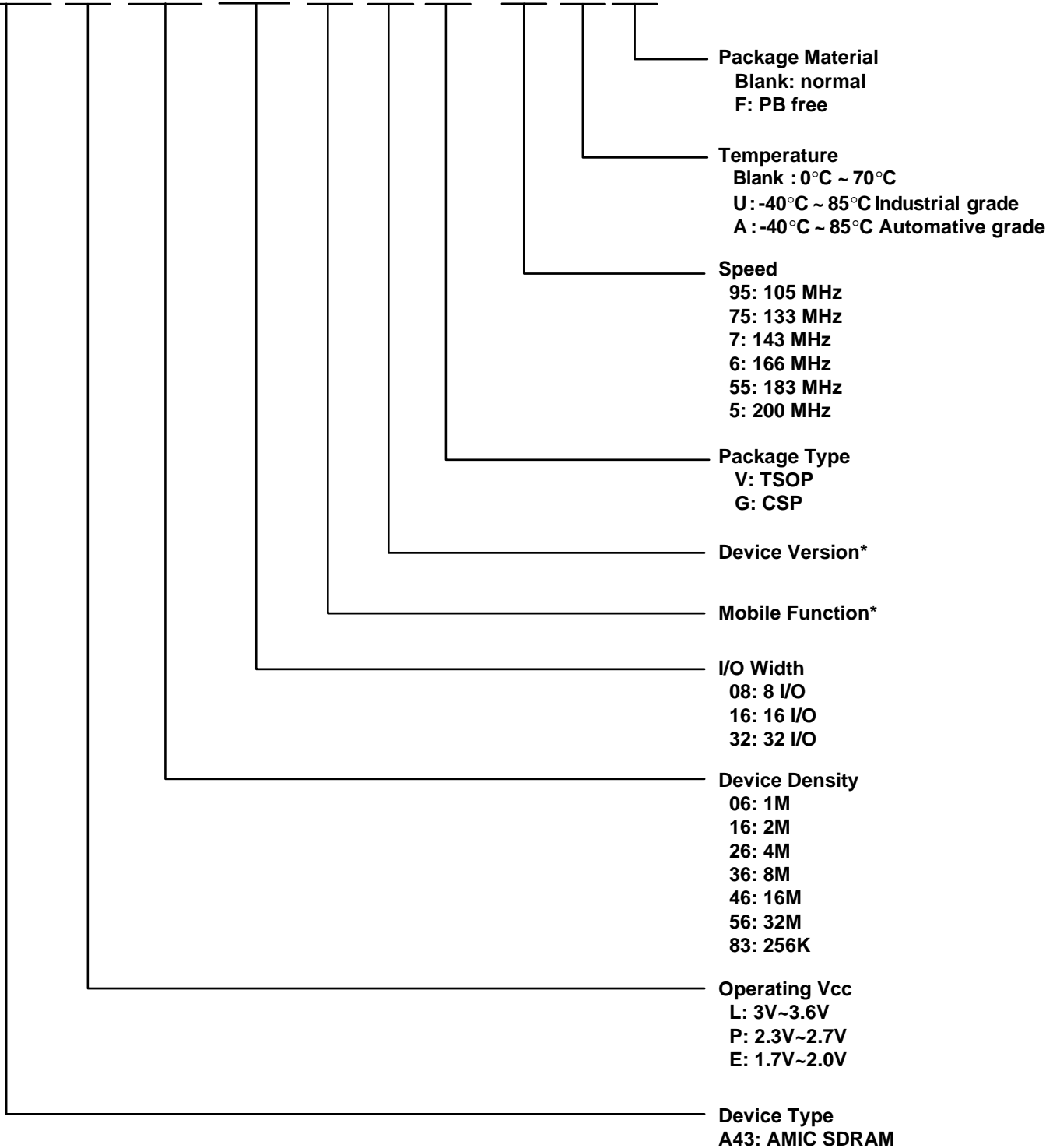
Note: 6. After CKE's low to high transition to exit self refresh mode. And a time of  $t_{rc}(\min)$  has to be elapse after CKE's low to high transition to issue a new command.

7. CKE low to high transition is asynchronous as if restarts internal clock.

A minimum setup time "tSS + one clock" must be satisfied before any command other than exit.

8. Power-down and self refresh can be entered only from the all banks idle state.

9. Must be a legal command.

**Part Numbering Scheme**
**A43 X XX XX X X X - X X X**


\* Optional

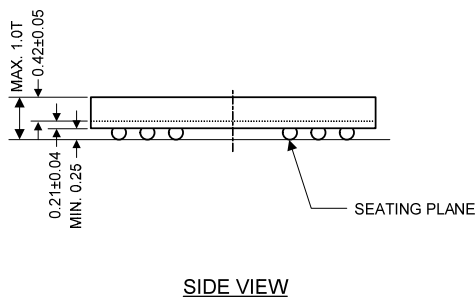
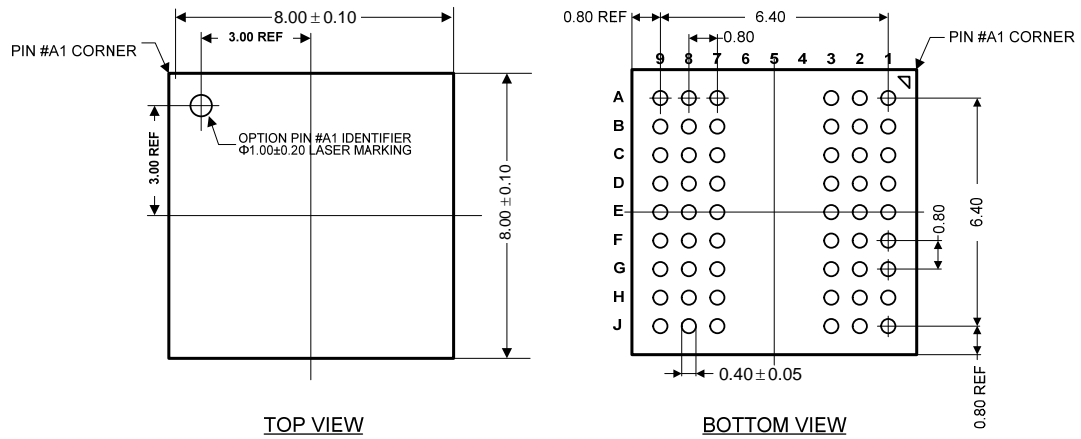
**Ordering Information**

Part No.	Cycle Time (ns)	Clock Frequency (MHz)	Access Time	Package	
A43L3616AV -6F	6	166 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)	
		100 @ CL = 2	5.4 ns @ CL = 2		
A43L3616AV -6UF		166 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)	
		100 @ CL = 2	5.4 ns @ CL = 2		
A43L3616AG -6F		166 @ CL = 3	5.4 ns @ CL = 3	54B Pb-Free CSP	
		100 @ CL = 2	5.4 ns @ CL = 2		
A43L3616AG -6UF		166 @ CL = 3	5.4 ns @ CL = 3	54B Pb-Free CSP	
		100 @ CL = 2	5.4 ns @ CL = 2		
A43L3616AV -7F		7	143 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)
			100 @ CL = 2	5.4 ns @ CL = 2	
A43L3616AV -7UF			143 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)
			100 @ CL = 2	5.4 ns @ CL = 2	
A43L3616AV -7AF	143 @ CL = 3		5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)	
	100 @ CL = 2		5.4 ns @ CL = 2		
A43L3616AG -7F	143 @ CL = 3		5.4 ns @ CL = 3	54B Pb-Free CSP	
	100 @ CL = 2		5.4 ns @ CL = 2		
A43L3616AG -7UF	143 @ CL = 3		5.4 ns @ CL = 3	54B Pb-Free CSP	
	100 @ CL = 2		5.4 ns @ CL = 2		
A43L3616AG -7AF	143 @ CL = 3		5.4 ns @ CL = 3	54B Pb-Free CSP	
	100 @ CL = 2		5.4 ns @ CL = 2		
A43L3616AV -75F	7.5	133 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)	
		100 @ CL = 2	6 ns @ CL = 2		
A43L3616AV -75UF		133 @ CL = 3	5.4 ns @ CL = 3	54 TSOP (II) (Pb-Free)	
		100 @ CL = 2	6 ns @ CL = 2		
A43L3616AG -75F		133 @ CL = 3	5.4 ns @ CL = 3	54B Pb-Free CSP	
		100 @ CL = 2	6 ns @ CL = 2		
A43L3616AG -75UF		133 @ CL = 3	5.4 ns @ CL = 3	54B Pb-Free CSP	
		100 @ CL = 2	6 ns @ CL = 2		

Note: -U is for industrial operating temperature range -40°C to +85°C.  
 -A is for automotive operating temperature range -40°C to +85°C.

**Package Information**
**54 Balls CSP (8 x 8 mm) Outline Dimensions**

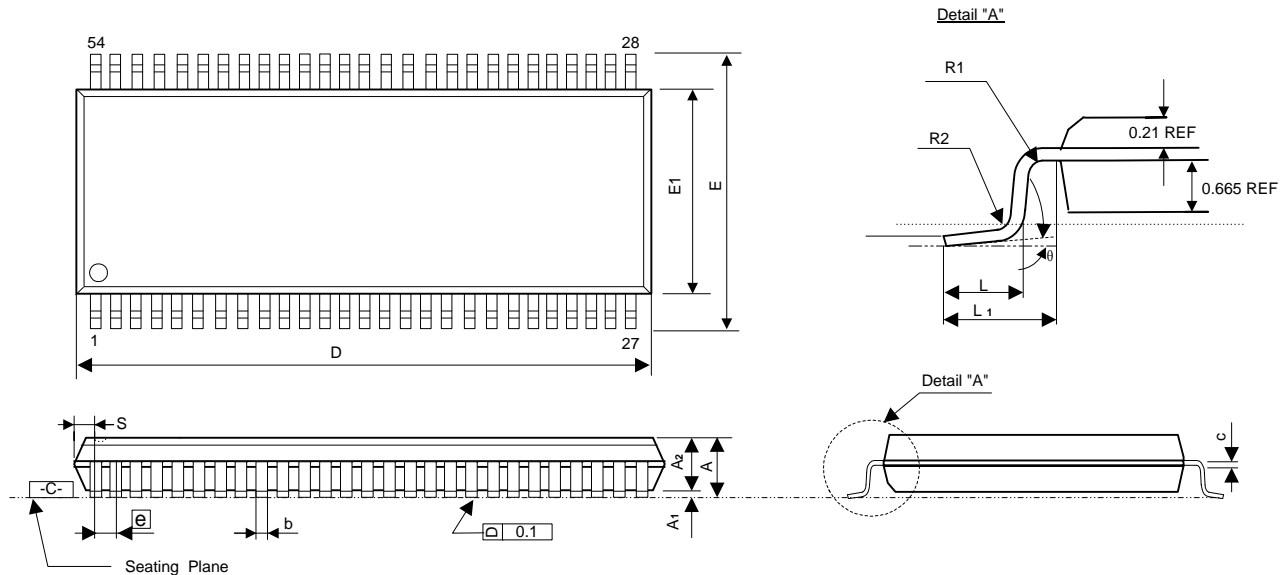
unit: mm





**Package Information**
**TSOP 54 (Type II) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.875 BSC			22.22 BSC		
S	0.028 REF			0.71 REF		
E	0.463 BSC			11.76 BSC		
E1	0.400 BSC			10.16 BSC		
e	0.031 BSC			0.80 BSC		
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	0.031 REF			0.80 REF		
R1	0.005	-	-	0.12	-	-
R2	0.005	-	0.010	0.12	-	0.25
θ	0°	-	8°	0°	-	8°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.