Future Technology Devices International Ltd
UM232H Single Channel USB Hi-Speed FT232H Development Module
Datasheet

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1 Introduction

The UM232H is a USB-to-serial/FIFO development module in the FTDI product range which utilises the FT232H USB Hi-Speed (480Mb/s) single-port bridge chip to handle the USB signaling and protocols. The UM232H is ideal for development purposes to quickly prove functionality of adding USB to a target design. The UM232H is a module designed to plug into a standard 0.6” wide 28 pin DIP socket. The USB connection to a host system is via a mini-B USB connector. All components used, including the FT232H, are Pb-free (RoHS compliant).

Figure 1.1: UM232H USB to Serial/FIFO Development Module

1.1 FT232H

The FT232H is a single channel USB 2.0 Hi-Speed (480Mb/s) to Serial/FIFO IC. It can be configured in a variety of serial or parallel interfaces, such as UART, FIFO or FTDI’s MPSSE mode which can configure either of the following interfaces: JTAG, SPI and I2C. For MPSSE mode, there is also 14 bit-banging lines available along with the four interface lines. In addition to these, the FT232H supports a CPU-Style FIFO mode and a fast serial interface mode. It also introduces a half-duplex FT1248 interface that provides a flexible data communication and high performance interface between the FT232H device and external logic. For further
details on the FT232H and the FT1248 mode, please refer to the FT232H datasheet and application note: AN_167 FT1248 Parallel Serial Interface Basics, located at the FTDI website.
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2 Typical Applications

The UM232H module can be used for prototyping and evaluation in an application using the FT232H.

- Rapid USB integration into existing and new electronic systems
- USB to FT1248 interfaces (half duplex)
- USB to RS232 / RS422 / RS485 Converters
- USB Instrumentation
- USB Industrial Control
- USB Electronic Point Of Sale Control
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- USB Smart Card Readers
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB dongle applications
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles
- USB Medical applications

2.1 Driver Support

The UM232H development module requires USB device drivers, available free from FTDI website. There is the Virtual Com Port driver which allows the UM232H to appear as a serial port allowing legacy applications for serial ports to function over USB (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT232H on the UM232H through a DLL.

Supported platforms include: current Microsoft® Windows® operating systems, Linux® version 2.6.39 or later (VCP drivers), Linux® version 2.6.32 or later (D2XX drivers), Mac OS® and Microsoft Windows CE® version 4.2 onwards.

2.2 Part Numbers

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UM232H</td>
<td>Development module for FT232H</td>
</tr>
</tbody>
</table>
2.3 Features

The UM232H has the following features:

- Based on the Single chip USB Hi-Speed FT232H device.
- USB 2.0 Hi-Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible
- Entire USB protocol handled on the chip – No USB-specific firmware programming required.
- Small USB Type B connector common on many commercial devices
- USB bus or self powered options.
- Asynchronous UART transfer data rate up to 12Mbaud.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- Fully assisted hardware or X-On / X-Off software handshaking.
- Auto-transmit buffer control for RS485 applications.
- Supports a half duplex FT1248 interface with a bi-directional data bus (1, 2, 4 or 8 bits wide).
- Synchronous Serial (MPSSE) data rates of up to 30Mbps on JTAG, SPI and I2C
- Support for USB suspend and resume
- UHCI / OHCI / EHCI host controller compatible
- FTDI’s royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- 1kByte receive and transmit buffers for high data throughput.
- Transmit and receive LED drive signals.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes.
- Support for USB suspend and resume.
- Integrated 3.3V level converter for USB I/O.
- USB bulk transfer mode.
- +2.97V to +5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- -40°C to +85°C operating temperature range
- Rapid integration into existing systems
3 FT232H Features and Enhancement

3.1 Key Features

**USB Hi-Speed to UART/FIFO Interface.** The FT232H provides a USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable UART/FIFO Interfaces.

**Functional Integration.** The FT232H integrates a USB protocol engine, which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. The FT232H includes an integrated +1.8V/3.3V Low Drop-Out (LDO) regulator. It also includes 1Kbytes Tx and Rx data buffers. The FT232H integrates the entire USB protocol on a chip with no firmware required.

**MPSSE.** Multi-Protocol Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

**FT1248 interface.** The FT232H supports a half-duplex FT1248 interface with a bi-directional data bus interface that can be configured as 1, 2, 4 or 8-bits wide and this enables the flexibility to expand the size of the data bus to 8 pins. The FT1248 interface provides flexible data communication between an FT232H FT1248 slave and an external FT1248 master. The FT1248 interface consists of four signals called MIOSIO, the bi-directional data lines between the FT232H and an external master controller, SCLK, which is the external clock input for latching data in or out the device at frequency up to 30MHz, SS_N Slave select input

**MISO,** which is the Master In Slave Out output from the FT232H in FT1248 mode. An external FT1248 master selects one of the FT1248 slave devices or enables the interface by pulling the Slave select input (SS_N) to logic 0. The FT1248 mode can be configured via the EEPROM settings with the free utility called FT_PROG which can be downloaded from the FTDI Utilities page. For further details about FT1248 mode, see FT232H datasheet and application note AN_167 FT232H Parallel Serial Interface Basics at the FTDI website.

**Data Transfer rate.** The FT232H supports a data transfer rate up to 12 Mbaud when configured as an RS232/RS422/RS485 UART interface or up to 40 Mbytes/second over a synchronous 245 parallel FIFO interface or up to 8 Mbyte/Sec over an asynchronous 245 FIFO interface.

**Latency Timer.** A feature of the driver used as a timeout to transmit short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 255ms.

**Bus (ACBUS) functionality, signal inversion and drive strength selection.** There are 11 configurable ACBUS I/O pins. These configurable options are:

1. TXDEN - transmit enable for RS485 designs.
2. PWREN# - Power control for high power, bus powered designs.
3. TXLED# - for pulsing an LED upon transmission of data.
4. RXLED# - for pulsing an LED upon receiving data.
5. TX&RXLED# - which will pulse an LED upon transmission OR reception of data.
6. SLEEP# - indicates that the device going into USB suspend mode.
7. CLK30 / CLK15 / CLK7.5 - 30MHz, 15MHz and 7.5MHz clock output signal options.
8. TriSt-PU – Input pulled up, not used
9. DRIVE 1 – Output driving high
10. DRIVE 0 – Output driving low
11. I/O mode – ACBUS Bit Bang

The ACBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins which are available during normal operation.

The ACBUS lines can be configured with any one of these input/output options by setting bits in the external EEPROM

**Multi-Purpose UART/FIFO Controllers.** The FT232H has one independent Serial/FIFO Controller. This controls the UART data, 245 FIFO data, Fast Serial (opto isolation) or Bit-Bang mode which can be selected
by SETUP (SetBitMode) command. Each Multi-Purpose UART/FIFO Controller also contains an MPSSE (Multi-Protocol Synchronous Serial Engine). Using this MPSSE, the Multi-Purpose Serial/FIFO Controller can be configured under software command, to have one of the MPSSE interfaces (SPI, I²C, and JTAG).

**USB Protocol Engine and FIFO control.** The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

**Port FIFO TX Buffer (1Kbytes).** Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

**Port FIFO RX Buffer (1Kbytes).** Data from the Multi-purpose Serial/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

**RESET Generator** – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT232H. RESET# should be tied to VCCIO (+3.3V) if not being used.

**Baud Rate Generators** – The Baud Rate Generators provides a x16 or a x10 clock input to the UART’s from a 120MHz reference clock and consists of a 14 bit prescaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART, which is programmable from 183 baud to 12 Mbaud. See FTDI application note AN_120 on the FTDI website for more details.

**EEPROM Interface.** If the external EEPROM is fitted, the FT232H can be configured as an asynchronous serial UART (default mode), parallel FIFO (245) mode, FT1248, fast serial (opto isolation) or CPU-Style FIFO. The EEPROM should be a 16 bit wide configuration such as a 93LC56B or equivalent capable of a 1Mbit/s clock rate at VCCIO = +2.97V to 3.63V. The EEPROM is programmable in-circuit over USB using a utility program called FT_Prog available from FTDI web site.

**+1.8/3.3V LDO Regulator.** The +3.3/+1.8V LDO regulator generates +1.8 volts for the core and the USB transceiver cell and +3.3V for the IO and the internal PLL and USB PHY power supply.

**UTMI PHY.** The Universal Transceiver Macrocell Interface (UTMI) physical interface cell is the USB transceiver. This block handles the Full speed / Hi-Speed SERDES (serialise – deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal must be connected to the OSCI and OSCO pins or 12 MHz Oscillator must be connected to the OSCI, and the OSCO is left unconnected. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s “Hi-Speed” (HS)/ 12 Mbit/s “Full Speed” (FS).
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.
4 UM232H Pin Out and Signal Descriptions

4.1 UM232H Pin Out

The signal labels and pin designators for each pin of the UM232H are illustrated in Fig. 4.1.

![UM232H Pin Diagram]

Figure 4.1: Module Pin Out
### 4.2 Signal Descriptions

**FT232H**

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>ASYNC Serial (RS232)</th>
<th>SYNC 245 FIFO</th>
<th>STYLE ASYNC 245 FIFO</th>
<th>SYNC Bit-bang</th>
<th>SYNCH Bit-bang</th>
<th>MPSSE</th>
<th>Fast Serial interface</th>
<th>CPU Style FIFO</th>
<th>FT1248</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>ADBUS0</td>
<td>TXD</td>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>D0</td>
<td>TCK/CLK</td>
<td>FSDI</td>
<td>D0</td>
<td>MIOUS0</td>
</tr>
<tr>
<td>14</td>
<td>ADBUS1</td>
<td>RXD</td>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>D1</td>
<td>TDI/DDI</td>
<td>FSCLK</td>
<td>D1</td>
<td>MIOUS1</td>
</tr>
<tr>
<td>15</td>
<td>ADBUS2</td>
<td>RTS#</td>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>D2</td>
<td>TDO/DO</td>
<td>FSDD</td>
<td>D2</td>
<td>MIOUS2</td>
</tr>
<tr>
<td>16</td>
<td>ADBUS3</td>
<td>CTS#</td>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>D3</td>
<td>TMS/CS</td>
<td>FSCTS</td>
<td>D3</td>
<td>MIOUS3</td>
</tr>
<tr>
<td>17</td>
<td>ADBUS4</td>
<td>DTR#</td>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>D4</td>
<td>GPIOL0</td>
<td>TriSt-Up</td>
<td>D4</td>
<td>MIOUS4</td>
</tr>
<tr>
<td>18</td>
<td>ADBUS5</td>
<td>DSR#</td>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>D5</td>
<td>GPIOL1</td>
<td>TriSt-Up</td>
<td>D5</td>
<td>MIOUS5</td>
</tr>
<tr>
<td>19</td>
<td>ADBUS6</td>
<td>DCD#</td>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>D6</td>
<td>GPIOL2</td>
<td>TriSt-Up</td>
<td>D6</td>
<td>MIOUS6</td>
</tr>
<tr>
<td>20</td>
<td>ADBUS7</td>
<td>RI#</td>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>D7</td>
<td>GPIOL3</td>
<td>TriSt-Up</td>
<td>D7</td>
<td>MIOUS7</td>
</tr>
<tr>
<td>21</td>
<td>ACBUS0</td>
<td>* RXDEN</td>
<td>RXF#</td>
<td>RXF#</td>
<td>ACBUS0</td>
<td>ACBUS0</td>
<td>GPIOL0</td>
<td>** ACBUS0</td>
<td>CS#</td>
<td>SCLK</td>
</tr>
<tr>
<td>22</td>
<td>ACBUS1</td>
<td>** ACBUS1</td>
<td>TXE#</td>
<td>TXE#</td>
<td>WRSTB#</td>
<td>WRSTB#</td>
<td>GPIOL1</td>
<td>** ACBUS1</td>
<td>A0</td>
<td>SS_N</td>
</tr>
<tr>
<td>23</td>
<td>ACBUS2</td>
<td>** ACBUS2</td>
<td>RD#</td>
<td>RD#</td>
<td>RDSTB#</td>
<td>RDSTB#</td>
<td>GPIOL2</td>
<td>** ACBUS2</td>
<td>RD#</td>
<td>MISO</td>
</tr>
<tr>
<td>24</td>
<td>ACBUS3</td>
<td>* RXLED#</td>
<td>WR</td>
<td>WR</td>
<td>ACBUS3</td>
<td>ACBUS3</td>
<td>GPIOL3</td>
<td>** ACBUS3</td>
<td>WR</td>
<td>ACBUS3</td>
</tr>
<tr>
<td>25</td>
<td>ACBUS4</td>
<td>* TXLED#</td>
<td>SIWU#</td>
<td>SIWU#</td>
<td>SIWU#</td>
<td>SIWU#</td>
<td>GPIOL4</td>
<td>SIWU#</td>
<td>SIWU#</td>
<td>ACBUS4</td>
</tr>
<tr>
<td>26</td>
<td>ACBUS5</td>
<td>** ACBUS5</td>
<td>CLKOUT</td>
<td>ACBUS5</td>
<td>** ACBUS5</td>
<td>** ACBUS5</td>
<td>GPIOH5</td>
<td>** ACBUS5</td>
<td>** ACBUS5</td>
<td>ACBUS5</td>
</tr>
<tr>
<td>27</td>
<td>ACBUS6</td>
<td>** ACBUS6</td>
<td>OE#</td>
<td>ACBUS6</td>
<td>ACBUS6</td>
<td>ACBUS6</td>
<td>GPIOH6</td>
<td>** ACBUS6</td>
<td>** ACBUS6</td>
<td>ACBUS6</td>
</tr>
<tr>
<td>28</td>
<td>ACBUS7</td>
<td>** ACBUS7</td>
<td>PWRSAV#</td>
<td>PWRSAV</td>
<td>PWRSAV#</td>
<td>PWRSAV#</td>
<td>** GPIOL7</td>
<td>PWRSAV#</td>
<td>PWRSAV#</td>
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<td>29</td>
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<tr>
<td>30</td>
<td>ACBUS9</td>
<td>** ACBUS9</td>
<td>ACBUS9</td>
<td>** ACBUS9</td>
<td>** ACBUS9</td>
<td>** ACBUS9</td>
<td>** ACBUS9</td>
<td>** ACBUS9</td>
<td>** ACBUS9</td>
<td>ACBUS9</td>
</tr>
</tbody>
</table>

Pins marked * are EEPROM selectable

**Table 4.1 : UM232H Signals**

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx) pull up resistor to VCCIO.

Pin marked *** default to GPIO line with an internal 75KΩ pull down resistor to GND. Using the EEPROM this pin can be enabled USBVCC mode instead of GPIO mode.
The following 2 tables provide a description of the signals available on each pin of the UM232H module

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1-1</td>
<td>GND</td>
<td>PWR</td>
<td>Module Ground Supply Pins</td>
</tr>
<tr>
<td>J1-2</td>
<td>5V0</td>
<td>Input</td>
<td>+5.0V or +3.3V power supply input.</td>
</tr>
<tr>
<td>J1-3</td>
<td>USB</td>
<td>Output</td>
<td>5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.</td>
</tr>
<tr>
<td>J1-4</td>
<td>RST#</td>
<td>Input</td>
<td>Can be used by an external device to reset the FT232H. If not required can be left unconnected, or pulled up to VCCIO</td>
</tr>
<tr>
<td>J1-5</td>
<td>AC9</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-6</td>
<td>AC8</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-7</td>
<td>AC7</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PD. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-8</td>
<td>AC6</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-9</td>
<td>AC5</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-10</td>
<td>AC4</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-11</td>
<td>AC3</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-12</td>
<td>AC2</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-13</td>
<td>AC1</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
<tr>
<td>J1-14</td>
<td>AC0</td>
<td>I/O</td>
<td>Configurable ACBUS I/O Pin. Function of this pin is configured by EEPROM. The default configuration is TriSt-PU. See ACBUS Signal Options, Table 4.3</td>
</tr>
</tbody>
</table>

Table 4.2: UM232H Connector J1 Signal Description
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2-1</td>
<td>SLD</td>
<td>Shield to GND</td>
<td>USB Cable Shield shorted to GND via a 0Ω resistor.</td>
</tr>
<tr>
<td>J2-2</td>
<td>VIO</td>
<td>PWR</td>
<td>Supply to the UART Interface and ACBUS I/O pins. Nominally 3.3V. Full range is 2.97V to 3.63V.</td>
</tr>
<tr>
<td>J2-3</td>
<td>3V3</td>
<td>Output/Input</td>
<td>+3.3V output from the integrated L.D.O. regulator if the UM232H is running on 5V self or bus powered designs. Therefore this pin can be used to supply the FT232HL’s VCCIO pin by connecting this pin to J2-2 (VIO). This pin can also be an input if the UM232H is running on 3.3V self powered designs.</td>
</tr>
<tr>
<td>J2-4</td>
<td>PU2</td>
<td>Control</td>
<td>Pull up resistor pin connection 1. Connect to J1-3 (USB) in a self powered configuration.</td>
</tr>
<tr>
<td>J2-5</td>
<td>PU1</td>
<td>Control</td>
<td>Pull up resistor pin connection 2. Connect to J1-4 (RST#) in a self powered configuration.</td>
</tr>
<tr>
<td>J2-6</td>
<td>GND</td>
<td>PWR</td>
<td>Module Ground Supply Pins</td>
</tr>
<tr>
<td>J2-7</td>
<td>AD0</td>
<td>Output</td>
<td>Configurable Output Pin, the default configuration is Transmit Asynchronous Data Output / Handshake Signal.</td>
</tr>
<tr>
<td>J2-8</td>
<td>AD1</td>
<td>Input</td>
<td>Configurable Input Pin, the default configuration is Receiving Asynchronous Data Input / Handshake Signal.</td>
</tr>
<tr>
<td>J2-9</td>
<td>AD2</td>
<td>Output</td>
<td>Configurable Output Pin, the default configuration is Request to Send Control Output / Handshake Signal.</td>
</tr>
<tr>
<td>J2-10</td>
<td>AD3</td>
<td>Input</td>
<td>Configurable Input Pin, the default configuration is Clear To Send Control Input / Handshake Signal.</td>
</tr>
<tr>
<td>J2-11</td>
<td>AD4</td>
<td>Output</td>
<td>Configurable Output Pin, the default configuration is Data Terminal Ready Control Output / Handshake Signal.</td>
</tr>
<tr>
<td>J2-12</td>
<td>AD5</td>
<td>Input</td>
<td>Configurable Input Pin, the default configuration is Data Set Ready Control Input / Handshake Signal.</td>
</tr>
<tr>
<td>J2-13</td>
<td>AD6</td>
<td>Input</td>
<td>Configurable Input Pin, the default configuration is Data Carrier Detect Control Input / Handshake Signal.</td>
</tr>
<tr>
<td>J2-14</td>
<td>AD7</td>
<td>Input</td>
<td>Configurable Input Pin, the default configuration is RI#, Ring Indicator Control Input/ Handshake Signal. When remote wake up is enabled in the EEPROM taking RI# low &gt;20ms can be used to resume the PC USB host controller from suspend.</td>
</tr>
</tbody>
</table>

Table 4.3 : UM232H Connector J2 Signal Description

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = “1”) by setting an option in the EEPROM.
4.3 ACBUS Signal Options

The table below describes the EEPROM options which can be configured on the ACBUS I/O pins using the software utility FT_PROG (which can be downloaded from the FTDI utilities page) The default EEPROM configuration is described in section 9.

<table>
<thead>
<tr>
<th>ACBUS Signal Option</th>
<th>Available On ACBUS Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXDEN</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>TXDEN = (TTL level). Used with RS485 level converters to enable the line driver during data transmit. TXDEN is active from one-bit time before the start bit is transmitted on TXD until one bit time after the last stop bit.</td>
</tr>
<tr>
<td>*PWREN#</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*</td>
</tr>
<tr>
<td>TXLED#</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device. This can be connected to an LED.</td>
</tr>
<tr>
<td>RXLED#</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device. This can be connected to an LED.</td>
</tr>
<tr>
<td>TX&amp;RXLED#</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>LED drive – pulses low when transmitting or receiving data from or to the external device. For more details, refer to the FT232H datasheet on the FTDI website.</td>
</tr>
<tr>
<td>SLEEP#</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.</td>
</tr>
<tr>
<td>**CLK30</td>
<td>ACBUS0, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>30MHz Clock output.</td>
</tr>
<tr>
<td>**CLK15</td>
<td>ACBUS0, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>15MHz Clock output.</td>
</tr>
<tr>
<td>**CLK7.5</td>
<td>ACBUS0, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>7.5MHz Clock output.</td>
</tr>
<tr>
<td>TriSt-PU</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>Input Pull Up</td>
</tr>
<tr>
<td>DRIVE 1</td>
<td>ACBUS0, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>Output High</td>
</tr>
<tr>
<td>DRIVE 0</td>
<td>ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>Output Low</td>
</tr>
<tr>
<td>I/O mode</td>
<td>ACBUS5, ACBUS6, ACBUS8, ACBUS9</td>
<td>ACBUS BitBang</td>
</tr>
</tbody>
</table>

* A 10kΩ resistor pull up is also recommended.
**When in USB suspend mode, the output clocks are also suspended.
5 Module Dimensions

Figure 5.1: UM232H Module Dimensions

All dimensions are in millimetres.

The UM232H module uses lead free components, and are fully compliant with European Union specifications directive 2002/95/EC.
6 FT232H Device Characteristics and Ratings

6.1 DC Characteristics

The I/O signal levels are +3.3V, and all IO pins are +5V tolerant (except the USB PHY pins).

DC Characteristics (Ambient Temperature = -40°C to +85°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCIO*</td>
<td>VCCIO Operating Supply Voltage</td>
<td>2.97</td>
<td>3.63</td>
<td></td>
<td>V</td>
<td>Cells are 5V tolerant</td>
</tr>
<tr>
<td>VREGIN</td>
<td>VREGIN Voltage regulator Input</td>
<td>3.6</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
<td>+5V Supply</td>
</tr>
<tr>
<td>Ireg</td>
<td>Regulator Output Current</td>
<td></td>
<td></td>
<td>100</td>
<td>mA</td>
<td>+3V3 Output</td>
</tr>
<tr>
<td>ICC5V0</td>
<td>UM232H current drawn</td>
<td>2</td>
<td>62</td>
<td></td>
<td>mA</td>
<td>+5V Supply</td>
</tr>
<tr>
<td>ICC3V3</td>
<td>UM232H current drawn</td>
<td>1.2</td>
<td>59</td>
<td></td>
<td>mA</td>
<td>+3.3V Supply</td>
</tr>
</tbody>
</table>

Table 6.1: Operating Voltage and Current (except PHY)

*NOTE: Failure to connect all VCCIO pins will result in unpredictable device behaviour.

For the electrical characteristics of the FT232H device, please refer to the FT232H datasheet.
7 Module Configurations

The UM232H Module can be configured as USB Bus-Powered or USB Self-Powered. This section describes how to configure the UM232H for a number of different power supply arrangements.

7.1 BUS Powered Configuration

Bus powered configuration, where the +5V supply that powers the module is sourced from the USB bus, and the 3V3 regulator output powers the core of the FT232H.

![Image](image)

**Figure 7.1 : Bus Powered Configuration**

Figure 7.1 illustrates the UM232H in a typical USB bus powered design configuration, which consists of two connections, a J1-2 to J1-3 connection and a J2-2 to J2-3 connection.

Connecting J1-2 (5V0) to J1-3 (USB) takes the power from the VBUS pin (J1-3) and supplies it to the on chip voltage regulator input of the FT232H via pin 5V0 (J1-2).

Connecting J2-2 (VIO) (power input for core of the FT232H) and J2-3 (3V3) (power output from the FT232H) powers the VCCIO, VPLL and VPHY pins of the FT232H chip.

A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

i) On plug-in to USB, the device must draw no more than 100mA.

ii) On USB Suspend the device must draw no more than 500μA.

iii) A Bus Powered High Power USB Device (one that draws more than 100mA) should use PWREN# to keep the current below 100mA on plug-in and 500μA on USB suspend.

iv) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub.

v) No device can draw more that 500mA from the USB Bus.

Interfacing the UM232H module to a microcontroller (MCU), or other logic for a bus powered design would be done in exactly the same way as for Self-Powered designs (see Section 7.3), except that the MCU or external logic would take its power supply from the USB bus (either the 5V on the USB pin, or 3.3V on the 3V3 pin).
7.2 USB Bus Powered with Power Switching Configuration

USB Bus Powered circuits need to be able to power down in USB suspend mode in order to meet the \( \leq 500\mu A \) total USB suspend current requirement (including external logic). Some external hardware can power itself down into a low current state by monitoring the PWREN\# signal. For external logic that cannot power itself down in this way the FT232H provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 7.2 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1k\( \Omega \) series resistor and a 0.1\( \mu F \) capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT232H, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

A 100k\( \Omega \) resistor to VBUS creates a weak pull up on the gate, this can prevent current from flowing through the transistor during a power up or power down of the FT232H.

Alternatively, a dedicated power switch I.C. with inbuilt "soft-start" can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BM or equivalent.

Please note the following points in connection with power controlled designs:

i) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is applied on coming out of suspend.

ii) Set the Pull-down on Suspend option in the internal EEPROM.

iii) One of the ACBUS pins should be configured as PWREN\# in the internal EEPROM, and should be used to switch the power supply to the external circuitry.

iv) For USB high-power bus powered device (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the device should be set in the max power field in the internal EEPROM. A high-power bus powered device must use this descriptor in the internal EEPROM to inform the system of its power requirements.

v) For 3.3V power controlled circuits the FT232H’s VIO pin must not be powered down with the external circuitry (the PWREN\# signal gets its VCC supply from VIO). Either connect the power switch between...
the output of the 3.3V regulator and the external 3.3V logic or power VIO from the 3V3 pin of the FT232H.

7.3 Self Powered Configuration

7.3.1 Self-Powered Configuration with 3V3 I/O and running on +5V external supply:

Figure 7.3 : Self-Powered Configuration – 5V0 External Supply

Figure 7.3 illustrates the UM232H in a typical USB Self-Powered configuration. An external supply +5.0V is connected to the module’s 5V0 pin. J2-2 (VIO) is also connected to J2-3 (3V3) to supply the VCCIO supply from the on board regulator but a separate supply could have been used.

A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB Self powered devices are as follows:

i) A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller use powered down.

ii) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.

iii) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hub. In this case, the power descriptor in the internal EEPROM should be programmed to a value of zero (Self-Powered).

In order to meet requirement (i) the USB Power is used to control the RESET# Pin of the FT232H device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the devices as a full speed device to USB. When the USB Host or Hub Power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down.

To do this J1-3 (USB) is connected to PU2 and PU1 is connected to J2-4 (RST#). Failure to do this may cause some USB host or hub controllers to power up erratically.

Note: When the FT232H is in reset, the UART interface pins all go tri-state. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

Figure 7.3 is also an example of interfacing the FT232H to a Microcontroller (MCU) UART interface. This example uses TXD and RXD for transmission and reception of data and RTS# / CTS# hardware handshaking.
Optionally, RI# can be connected to another I/O pin on the MCU and could be used to wake up the USB host controller from suspend mode. If the MCU is handling power management functions, then an ACBUS pin can be configured as PWREN# and should be connected to an I/O pin of the MCU.

An alternative to connecting the pull-up network to the Reset pin, to prevent current from flowing back the USB power bus line, is to connect the network ACBUS7 pin to achieve the same results but with additional benefits. A function called PWRSAV# is used to prevent current from flowing the USB line in the same way as connecting the reset to the pull-up network. However, the PWRSAV# function has the additional feature of being able to put FT232H into sleep mode when the USB host is powered down. There is one trade off using reset instead of PWRSAV#, in MPSSE mode the ACBUS7 pin can be selected as a GPIO pin, using this pin from both PWRSAV# and GPIO mode can cause a conflict. PWRSAV# is enabled and disabled using the EEPROM, this function is disabled by default. Figure 7.4 illustrates an alternative USB Self-Power configuration.

Figure 7.4: Alternative Self-Powered Configuration – 5V0 External Supply
Self-Powered Configuration with 3V3 I/O and running on +3.3V external supply:

Figure 7.5: Self-Powered Configuration – 3V3 External Supply

Figure 7.4 illustrates the UM232H in a typical USB Self-Powered configuration similar to Figure 7.3. The difference here is that the UM232H module is powered from an external 3.3V supply which is connected to the 5V0 (+3V3 power supply input can also be supplied to 5V0 pin), VIO and 3V3 pins of the modules. Please note that when the UM232H running from +3V3, the 3V3 pin becomes an input. The VIO and 3V3 pins connection provides 3V3 to the VCCIOs, VPLL and VPHY on the FT232H chip.

Similarly to the USB-Powered configuration an alternative configuration which utilised PWRSAV# can be implemented. Figure 7.6 illustrated this configuration.
Figure 7.6: Alternative Self-Powered Configuration – 3V3 External Supply
8 UM232H Module Circuit Schematic
Figure 8.1 : Module Circuit Schematic
9 EEPROM Configuration

The FT232H uses an external EEPROM (on the UM232H module). This EEPROM can be programmed over USB using FT_Prog. The default settings of the EEPROM are shown in the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB Vendor ID (VID)</td>
<td>0403h</td>
<td>FTDI default VID (hex)</td>
</tr>
<tr>
<td>USB Product UD (PID)</td>
<td>6014h</td>
<td>FTDI default PID (hex)</td>
</tr>
<tr>
<td>bcd Device</td>
<td>009h</td>
<td></td>
</tr>
<tr>
<td>Serial Number Enabled?</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Serial Number</td>
<td>See Note</td>
<td>A unique serial number is generated and programmed into the EEPROM during device final test.</td>
</tr>
<tr>
<td>Pull down I/O Pins in USB Suspend</td>
<td>Disabled</td>
<td>Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).</td>
</tr>
<tr>
<td>Manufacturer Name</td>
<td>FTDI</td>
<td></td>
</tr>
<tr>
<td>Product Description</td>
<td>UM232H</td>
<td></td>
</tr>
<tr>
<td>Max Bus Power Current</td>
<td>90mA</td>
<td></td>
</tr>
<tr>
<td>Power Source</td>
<td>Bus Powered</td>
<td></td>
</tr>
<tr>
<td>Device Type</td>
<td>FT232H</td>
<td></td>
</tr>
<tr>
<td>USB Version</td>
<td>0200</td>
<td>Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 Hi-Speed device (480Mb/s).</td>
</tr>
<tr>
<td>Remote Wake Up</td>
<td>Enabled</td>
<td>Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms.</td>
</tr>
<tr>
<td>High Current I/Os</td>
<td>Disabled</td>
<td>Enables the high drive level on the UART and ACBUS I/O pins.</td>
</tr>
<tr>
<td>Load VCP Driver</td>
<td>Enabled</td>
<td>Makes the device load the VCP driver interface for the device.</td>
</tr>
<tr>
<td>ACBUS0</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS0 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS1</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS1 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS2</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS2 Input pulled up</td>
</tr>
<tr>
<td>ACBUS3</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS3 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS4</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS4 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS5</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS5 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS6</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS6 – Input pulled up</td>
</tr>
<tr>
<td>ACBUS7</td>
<td>TriSt-PU</td>
<td>Default configuration of ACBUS7 – Input pulled down</td>
</tr>
<tr>
<td>ACBUS8</td>
<td>PWRENn</td>
<td>Default configuration of ACBUS8 – PWR LED</td>
</tr>
<tr>
<td>ACBUS9</td>
<td>TX&amp;RXLED</td>
<td>Default configuration of ACBUS9 – Tx/Rx LED</td>
</tr>
</tbody>
</table>

Table 9.1: Default Internal EEPROM Configuration
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Appendix B – Revision History

<table>
<thead>
<tr>
<th>Document Title:</th>
<th>UM232H Single Channel USB Hi-Speed FT232H Development Module</th>
</tr>
</thead>
<tbody>
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<td>FT_000367</td>
</tr>
<tr>
<td>Clearance No.:</td>
<td>FTDI# 198</td>
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<tr>
<td>Document Feedback:</td>
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</tr>
</tbody>
</table>

Version Draft

<table>
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<tr>
<th>Version</th>
<th>Date</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Draft</td>
<td>31st January 2011</td>
<td>Initial Datasheet Created</td>
</tr>
<tr>
<td>1.0</td>
<td>14th February 2011</td>
<td>Initial release</td>
</tr>
<tr>
<td>1.1</td>
<td>21st March 2011</td>
<td>Additional dimensions added, EEPROM Default current limit updated</td>
</tr>
<tr>
<td>1.2</td>
<td>18th April 2011</td>
<td>Added and corrected details about ACBUS7 Updated schematic</td>
</tr>
<tr>
<td>1.21</td>
<td>9th January 2012</td>
<td>Updated section 2.1, Linux version</td>
</tr>
<tr>
<td>1.3</td>
<td>24th Oct 2012</td>
<td>Correct pin define position of ADBUS in Fig7.1 to Fig 7.6 Corrected VIO on pg 10 (3.3V)</td>
</tr>
</tbody>
</table>