

RoHS COMPLIANT

Vishay Siliconix

P-Channel 20-V (D-S) MOSFET

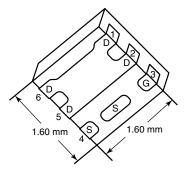
PRODUCT SUMMARY									
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^{a, f}	Q _g (Typ.)						
- 20	0.075 at V _{GS} = - 4.5 V	- 9	4.56 nC						
	0.143 at V _{GS} = - 2.5 V	- 7.8	4.50 110						

FEATURES

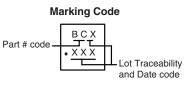
- · Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package
 - Small Footprint Area

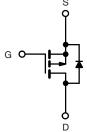
APPLICATIONS

Load Switch, PA Switch and Battery Switch for Portable Devices



PowerPAK SC-75-6L-Single





P-Channel MOSFET

Ordering Information: SiB413DK-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 20	V		
Gate-Source Voltage		V _{GS}	± 12	- v		
	T _C = 25 °C		- 9 ^a			
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	- 8.6			
	T _A = 25 °C	טי	- 4.5 ^{a, b}			
	T _A = 70 °C		- 3.7 ^{a, b}	A		
Pulsed Drain Current		I _{DM}	12			
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 9 ^a			
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	- 2 ^{a, b}			
	T _C = 25 °C		13			
Maximum Power Dissipation	T _C = 70 °C	PD	8.4	w		
	T _A = 25 °C	U U	2.4 ^{a, b}	~ ~ ~		
	T _A = 70 °C		1.6 ^{a, b}			
Operating Junction and Storage Temperature R	ange	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperatur	e) ^{c, d}		260			

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{a, e}	t ≤ 5 s	R _{thJA}	41	51	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	State R _{thJC} 7.5 9.5		0/11					

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 5 s.

- c. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Maximum under Steady State conditions is 105 °C/W.

f. Based on $T_C = 25$ °C.

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SPECIFICATIONS $T_J = 25 \ ^{\circ}C$,	unless oth	erwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = -250 \mu A$	- 20			V			
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 18.7		mV/°			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η - 200 μλ		2.56					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 0.6		- 1.5	V			
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA			
		$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1				
Zero Gate Voltage Drain Current	IDSS	V_{DS} = - 20 V, V_{GS} = 0 V, T_{J} = 55 °C		- 10	μΑ				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 5$ V, V_{GS} = - 4.5 V	12			Α			
	_	V _{GS} = - 4.5 V, I _D = - 6.5 A		0.062	0.075	~			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 1.8 A		0.119	0.143	Ω			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 6.5 A		8		S			
Dynamic ^b	<u> </u>			J	<u> </u>				
Input Capacitance	C _{iss}			357		pF			
Output Capacitance	C _{oss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		93					
Reverse Transfer Capacitance	C _{rss}			63					
Tatal Cata Oberra	Qg	V_{DS} = - 10 V, V_{GS} = - 5 V, I_D = - 6.5 A		5.09	7.63	0			
Total Gate Charge				4.56	6.84				
Gate-Source Charge	Q _{gs}	Q_{gs} V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 6.5 A		0.77		nC			
Gate-Drain Charge	Q _{gd}			0.93		1			
Gate Resistance	Rg	f = 1 MHz		8.1		Ω			
Turn-On Delay Time	t _{d(on)}			20.5	30.75				
Rise Time	t _r	V_{DD} = - 10 V, R_L = 2.70 Ω		46	69	ns			
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong$ - 3.7 A, V_GEN = - 4.5 V, R_g = 1 Ω		20	30				
Fall Time	t _f			6.5	9.75				
Drain-Source Body Diode Characteristi	cs	· · · · · · · · · · · · · · · · · · ·							
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 9	A			
Pulse Diode Forward Current	I _{SM}				12				
Body Diode Voltage	V _{SD}	$I_{\rm S}$ = - 3.2 A, $V_{\rm GS}$ = 0 V		- 0.8	- 1.2	V			
Body Diode Reverse Recovery Time	t _{rr}			19.3	29	ns			
Body Diode Reverse Recovery Charge	Q _{rr}			7.6	11.4	nC			
Reverse Recovery Fall Time	t _a	· I _F = - 3.2 A, di/dt = 100 A/μs, T _J = 25 °C		7.1		ns			
Reverse Recovery Rise Time	t _b	1		12.2					

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

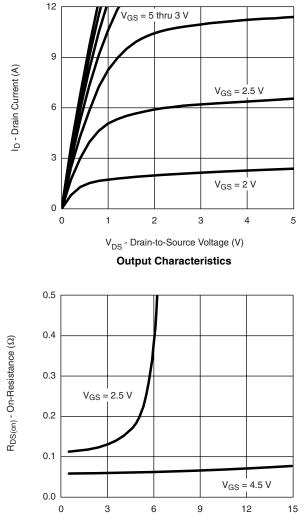
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



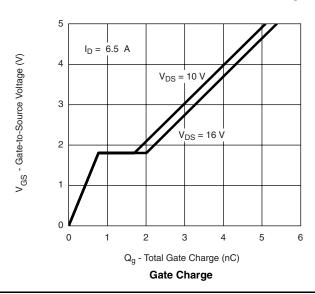
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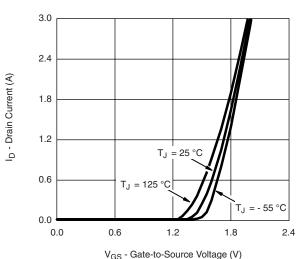
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



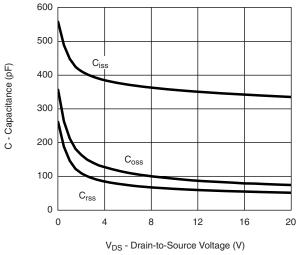
I_D - Drain Current (A)

On-Resistance vs. Drain Current and Gate Voltage

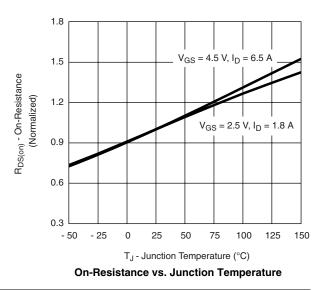




Transfer Characteristics



Capacitance

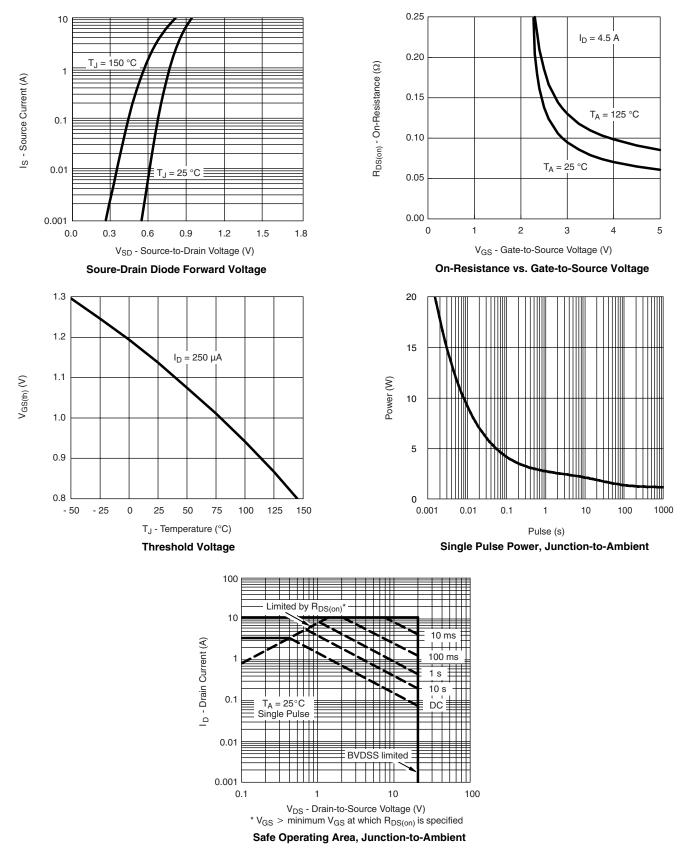


Document Number: 70441 S-80515-Rev. C, 10-Mar-08

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

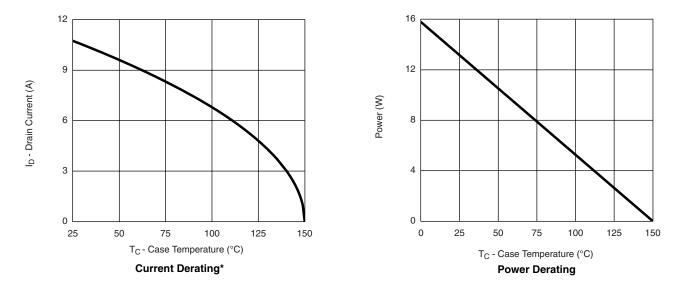






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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

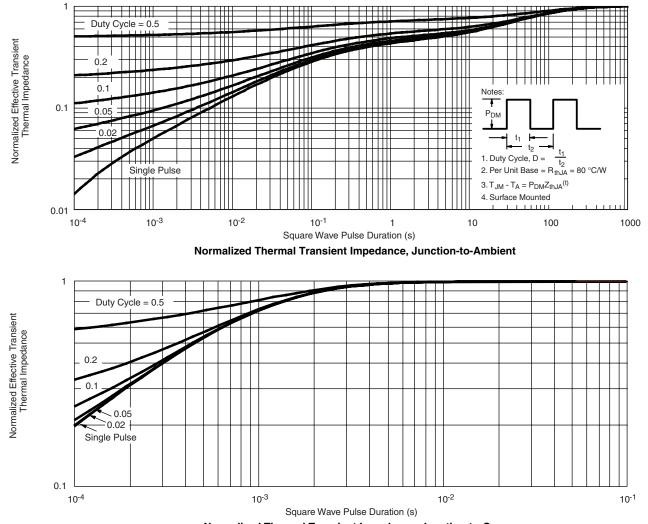


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



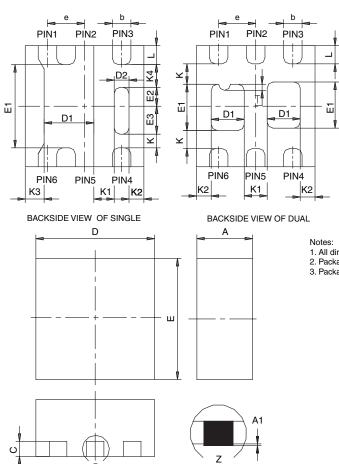
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70441.

Package Information

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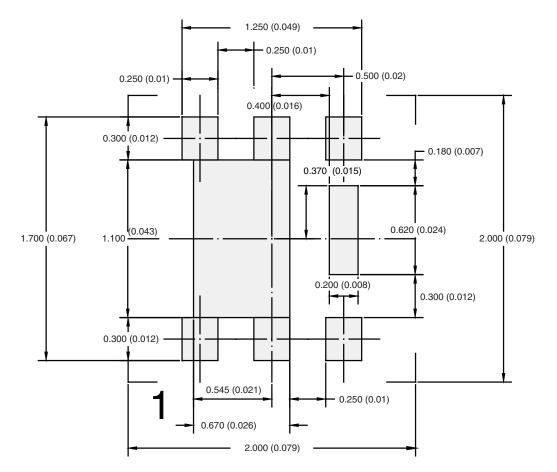
- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

DETAIL Z

		SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067	
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021	
D2	0.10	0.20	0.30	0.004	0.008	0.012							
Е	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067	
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028	
E2	0.20	0.25	0.30	0.008	0.010	0.012							
E3	0.32	0.37	0.42	0.013	0.015	0.017							
е		0.50 BSC			0.020 BSC		0.50 BSC			0.020 BSC			
К		0.180 TYP			0.007 TYP		0.245 TYP		0.010 TYP				
K1		0.275 TYP			0.011 TYP		0.320 TYP			0.013 TYP			
K2		0.200 TYP 0.008 TYP			0.200 BSC 0.008 TYP								
K3		0.255 TYP 0.010 TYP											
K4	0.300 TYP			0.012 TYP									
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014	
Т							0.03	0.08	0.13	0.001	0.003	0.005	
ECN: C-07431 – Rev. C, 06-Aug-07 DWG: 5935													



RECOMMENDED PAD LAYOUT FOR PowerPAK[®] SC75-6L Single



Dimensions in mm/(Inches)

Return to Index



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