

## P-Channel 40 V (D-S) MOSFET

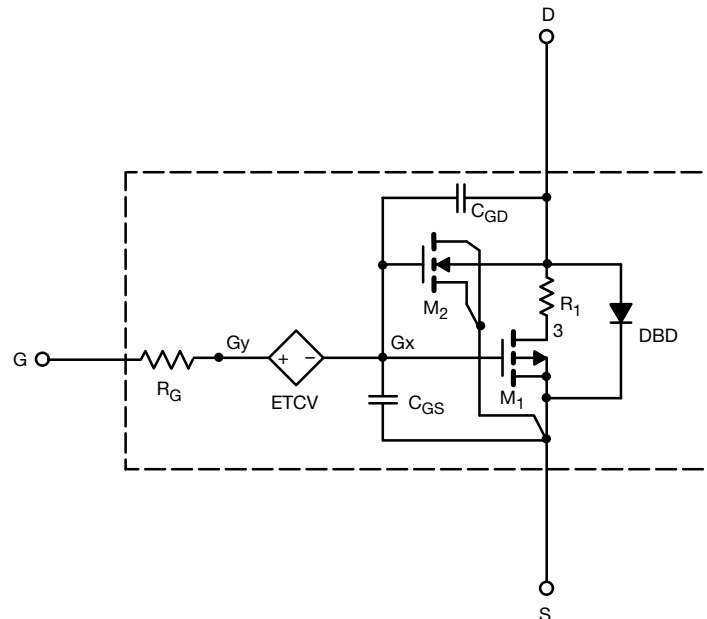
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



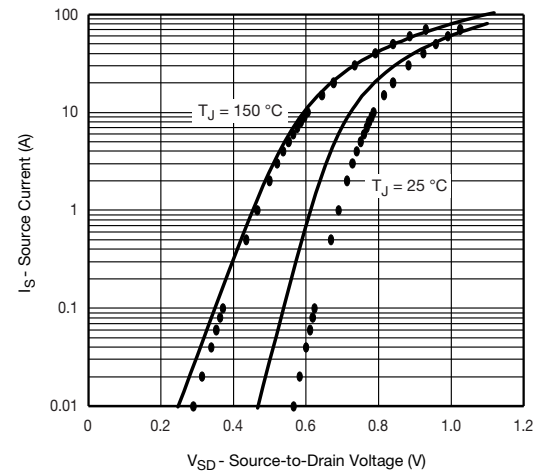
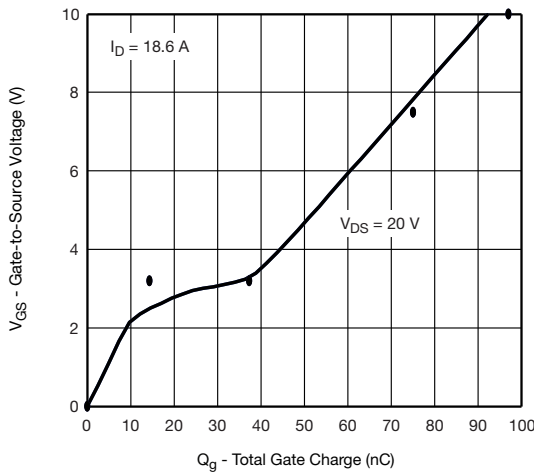
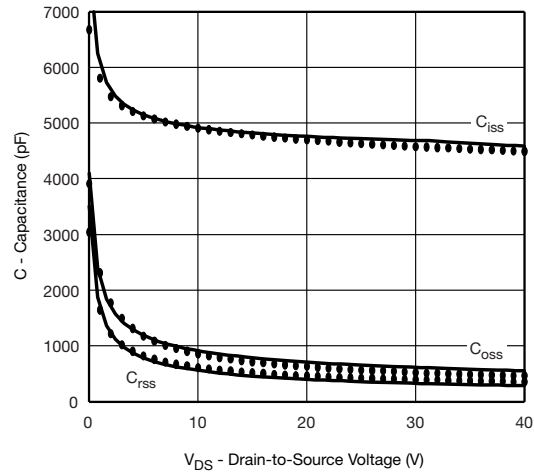
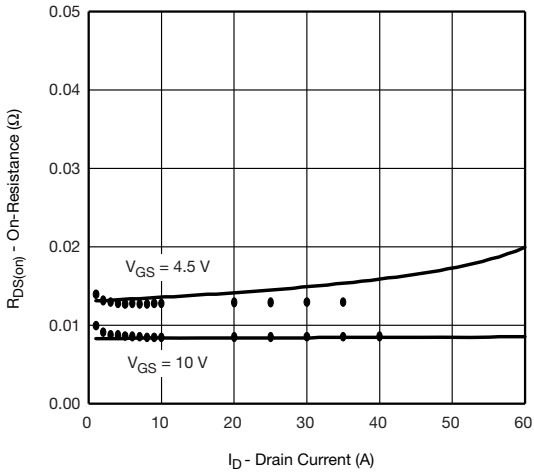
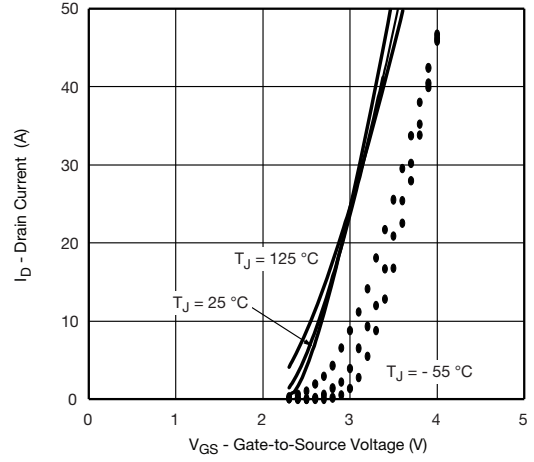
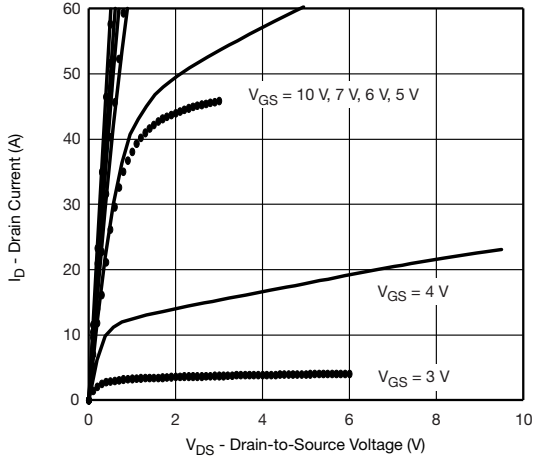
| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                     |   |                |               |      |
|---|---------------------|---|----------------|---------------|------|
| PARAMETER   | SYMBOL              | TEST CONDITIONS   | SIMULATED DATA | MEASURED DATA | UNIT |
| <b>Static</b>   |                     |   |                |               |      |
| Gate-Source Threshold Voltage                                   | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA                 | 1.4            | -             | V    |
| Drain-Source On-State Resistance <sup>a</sup>                   | R <sub>DS(on)</sub> | V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 18 A                             | 0.008          | 0.007         | Ω    |
|   |                     | V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 15 A                            | 0.013          | 0.011         |      |
| Forward Transconductance <sup>a</sup>                           | g <sub>fs</sub>     | V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 18 A                             | 42             | 45            | S    |
| Diode Forward Voltage   | V <sub>SD</sub>     | I <sub>S</sub> = - 4.5 A  | - 0.70         | - 0.80        | V    |
| <b>Dynamic<sup>b</sup></b>                                      |                     |   |                |               |      |
| Input Capacitance   | C <sub>iss</sub>    | V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz                    | 4760           | 4700          | pF   |
| Output Capacitance  | C <sub>oss</sub>    |   | 700            | 625           |      |
| Reverse Transfer Capacitance                                    | C <sub>rss</sub>    |   | 400            | 460           |      |
| Total Gate Charge   | Q <sub>g</sub>      | V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 18.6 A | 95             | 97            | nC   |
| Gate-Source Charge  | Q <sub>gs</sub>     |   | 14             | 14            |      |
| Gate-Drain Charge   | Q <sub>gd</sub>     |   | 23             | 23            |      |

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.



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