





DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = 25°C
-20V	0.9Ω @ V _{GS} = -4.5V	-530A
	1.4Ω @ V _{GS} = -2.5V	-440A

Description

This MOSFET has been designed to minimize the on-state resistance $(R_{DS(on)})$ and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Battery Charging
- Power Management Functions
- DC-DC Converters
- Portable Power Adaptors

Features

- Dual P-Channel MOSFET
- Low On-Resistance
- Very Low Gate Threshold Voltage V_{GS(TH)} < 1V
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

- Case: SOT563
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper lead frame.
 Solderable per MIL-STD-202, Method 208
- Weight: 0.006 grams (approximate)

SOT563

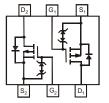




Top View



Bottom View



Top View Internal Schematic

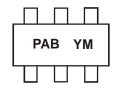
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2004VK-7	SOT563	3000/Tape & Reel

Notes:

- $1.\ No\ purposely\ added\ lead.\ Fully\ EU\ Directive\ 2002/95/EC\ (RoHS)\ \&\ 2011/65/EU\ (RoHS\ 2)\ compliant.$
- 2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com.

Marking Information



PAB = Marking Code YM = Date Code Marking Y = Year (ex: U = 2007) M = Month (ex: 9 = September)

Date Code Key

Year	2007	20	08	2009	2010	20)11	2012	2013	20	14	2015
Code	U	/	/	W	Х	,	Y	Z	Α	E	3	С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings $(@T_A = +25^{\circ}C, \text{ unless otherwise specified.})$

Characteristic		Symbol	Value	Units	
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V	
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I _D	-0.53 -0.44	А
Continuous Drain Current (Note 5) V _{GS} = -2.5V	Steady State	I _D	-0.44 -0.35	А	
Pulsed Drain Current (Note 6)		I _{DM}	-1.8	Α	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

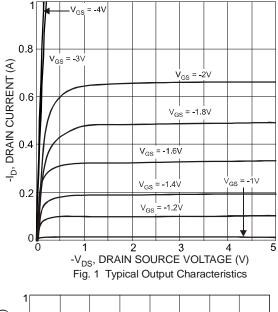
Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_{D}	400	mW
Thermal Resistance, Junction to Ambient	$R_{ heta JA}$	312	°C/W
Operating and Storage Temperature Range	T_J,T_STG	-65 to +150	°C

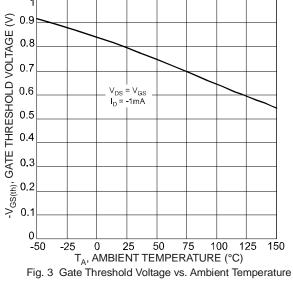
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

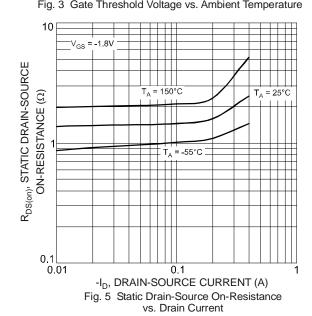
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	-20	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}		_	-1.0	μΑ	$V_{DS} = -20V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±1.0	μΑ	$V_{GS} = \pm 4.5V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	_	-1.0	٧	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
			0.7	0.9		$V_{GS} = -4.5V$, $I_D = -430mA$	
Static Drain-Source On-Resistance	R _{DS} (ON)		1.1	1.4	Ω	$V_{GS} = -2.5V$, $I_D = -300mA$	
			1.7	2.0		$V_{GS} = -1.8V, I_D = -150mA$	
Forward Transfer Admittance	Y _{fs}	200	_	_	mS	$V_{DS} = -10V, I_{D} = -0.2A$	
Diode Forward Voltage (Note 5)	V_{SD}	-0.5	_	-1.2	V	$V_{GS} = 0V, I_{S} = 115mA$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	_	175	pF		
Output Capacitance	Coss	1	_	30	pF	$V_{DS} = -16V, V_{GS} = 0V$ -f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}		_	20	pF	1 = 1.0ivii iz	

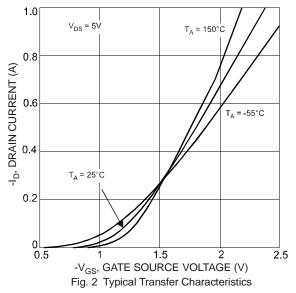
- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.6. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.











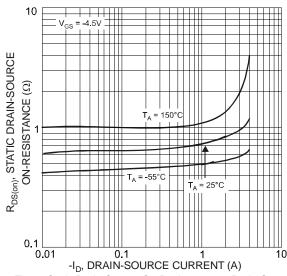


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

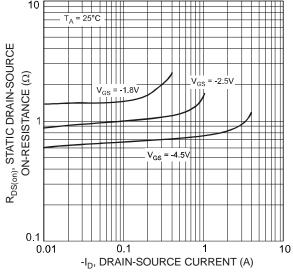


Fig. 6 Static Drain-Source On-Resistance vs.
Drain-Source Current



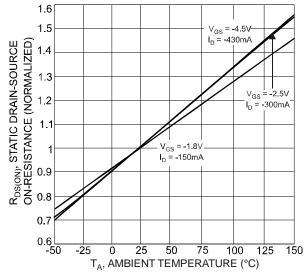


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

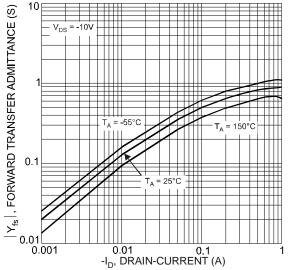


Fig. 9 Forward Transfer Admittance vs. Drain-Current

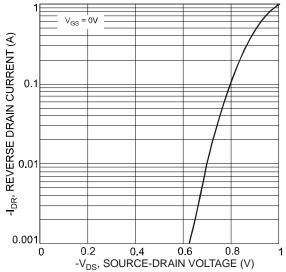
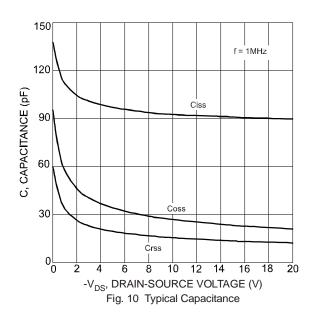
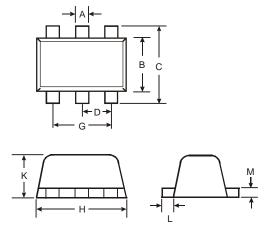


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage



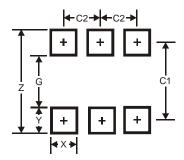
Package Outline Dimensions



	SOT563							
Dim	Min	Max	Тур					
Α	0.15	0.30	0.20					
В	1.10	1.25	1.20					
С	1.55	1.70	1.60					
D	-	-	0.50					
G	0.90	1.10	1.00					
Н	1.50	1.70	1.60					
K	0.55	0.60	0.60					
L	0.10	0.30	0.20					
M	0.10	0.18	0.11					
All	Dimens	sions in	mm					



Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.2
G	1.2
Х	0.375
Υ	0.5
C1	1.7
C2	0.5

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