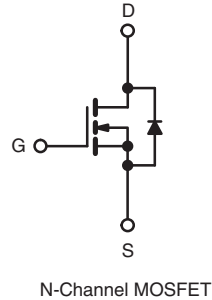
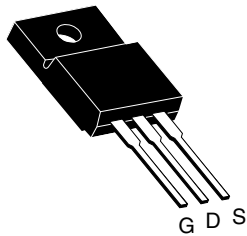


## D Series Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	450
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V   1.0
$Q_g$ max. (nC)	18
$Q_{gs}$ (nC)	3
$Q_{gd}$ (nC)	4
Configuration	Single

**TO-220 FULLPAK**

**FEATURES**

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance ( $C_{iss}$ )
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM):  $R_{on} \times Q_g$
  - Fast Switching
- Compliant to RoHS Directive 2011/65/EU


**RoHS\***  
COMPLIANT

**Note**

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**APPLICATIONS**

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
  - SMPS
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
- Battery Chargers


ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF6N40D-E3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	400	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Gate-Source Voltage AC ( $f > 1$ Hz)		30	
Continuous Drain Current ( $T_J = 150$ °C) <sup>e</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	13	
Linear Derating Factor		0.24	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	104	mJ
Maximum Power Dissipation	$P_D$	30	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		0.48	
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 9.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ , starting  $T_J = 25$  °C.
- Limited by maximum junction temperature.

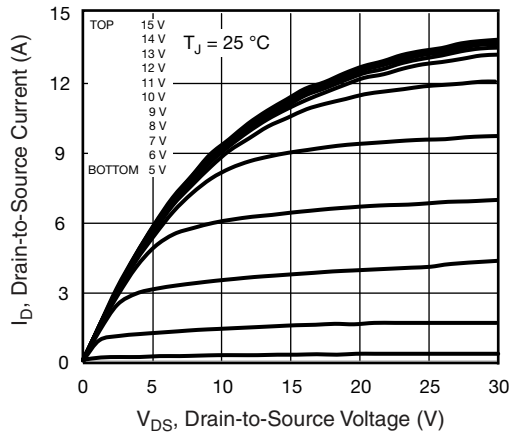
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	4.1	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 250\text{ }\mu\text{A}$		-	0.53	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3	-	5	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$	-	0.85	1.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 3\text{ A}$		-	1.7	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	311	-	pF
Output Capacitance	$C_{oss}$			-	38	-	
Reverse Transfer Capacitance	$C_{rss}$			-	7	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 0\text{ V to } 320\text{ V}$		-	44	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$			-	54	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}, V_{DS} = 320\text{ V}$	-	9	18	nC
Gate-Source Charge	$Q_{gs}$			-	3	-	
Gate-Drain Charge	$Q_{gd}$			-	4	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 3\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	12	24	ns
Rise Time	$t_r$			-	11	22	
Turn-Off Delay Time	$t_{d(off)}$			-	14	28	
Fall Time	$t_f$			-	8	16	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{ open drain}$		-	1.9	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	6	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	24	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 3\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$		-	236	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	1.1	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	9	-	A

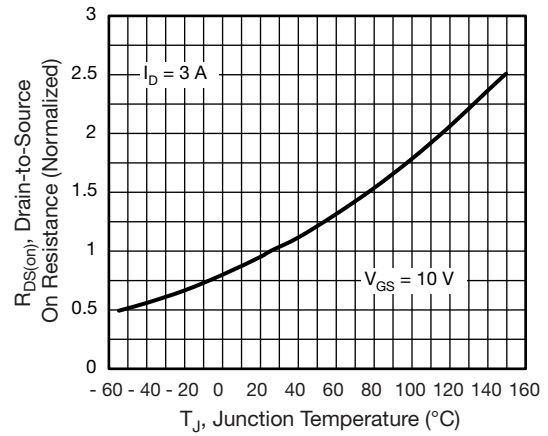
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

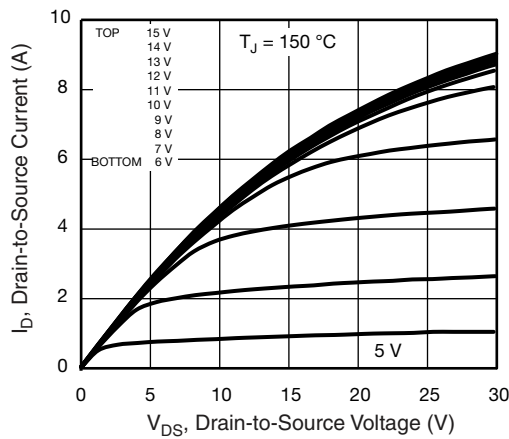
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



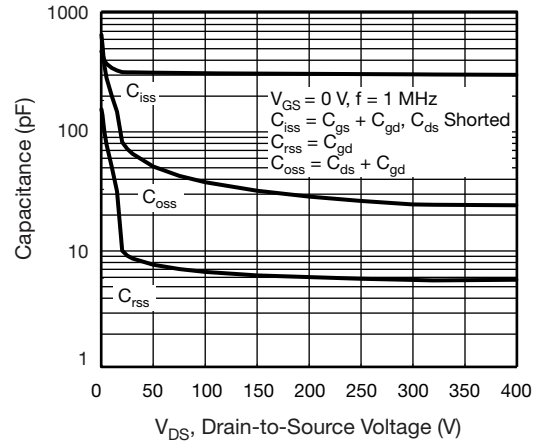
**Fig. 1 - Typical Output Characteristics**



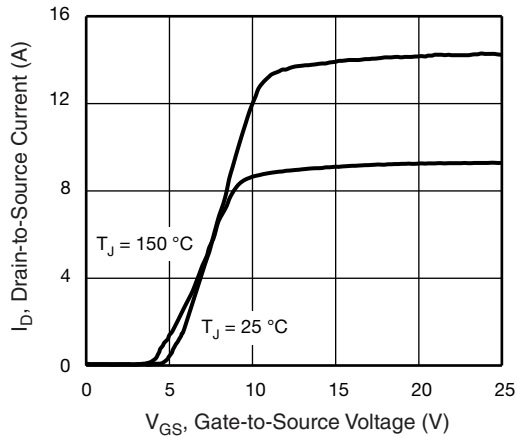
**Fig. 4 - Normalized On-Resistance vs. Temperature**



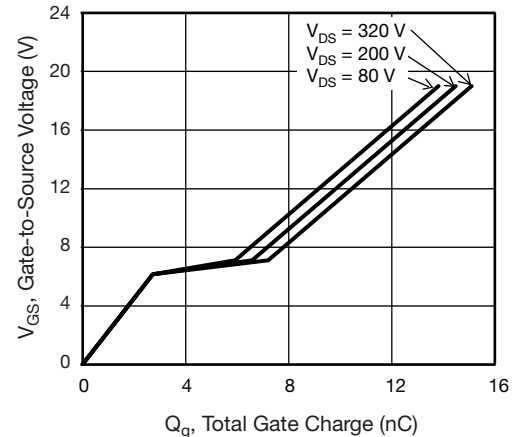
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

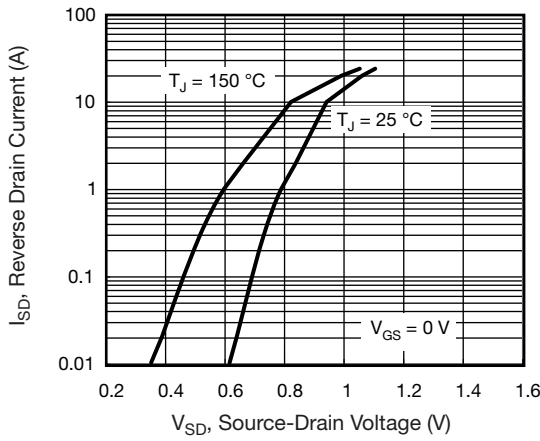


Fig. 7 - Typical Source-Drain Diode Forward Voltage

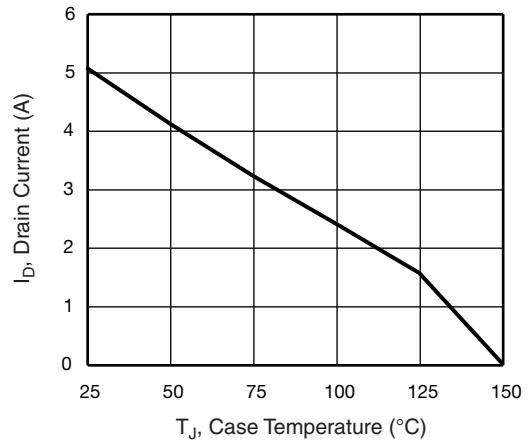


Fig. 9 - Maximum Drain Current vs. Case Temperature

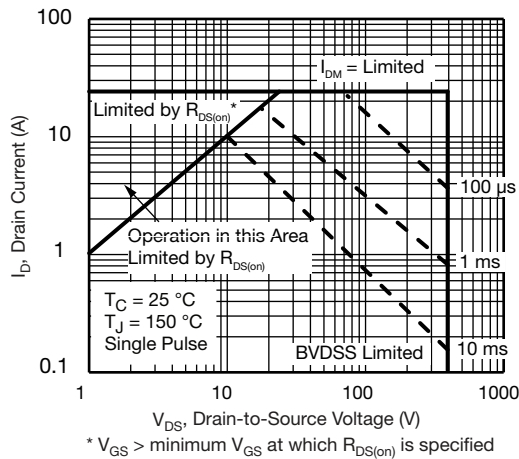


Fig. 8 - Maximum Safe Operating Area

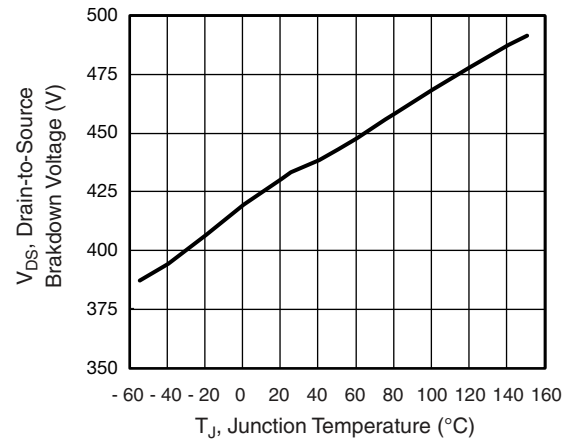


Fig. 10 - Temperature vs. Drain-to-Source Voltage

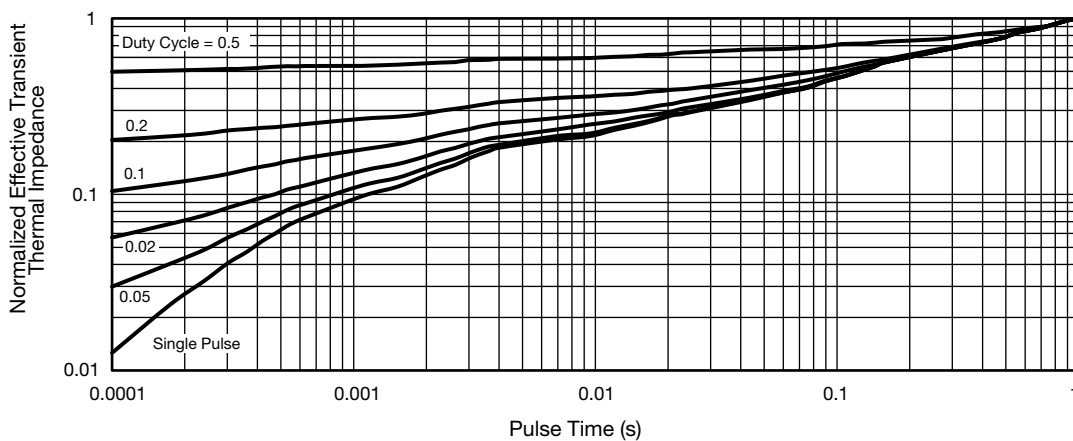
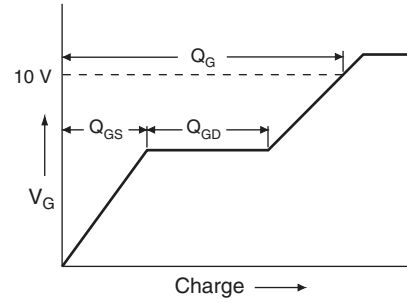


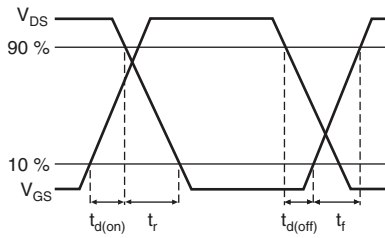
Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



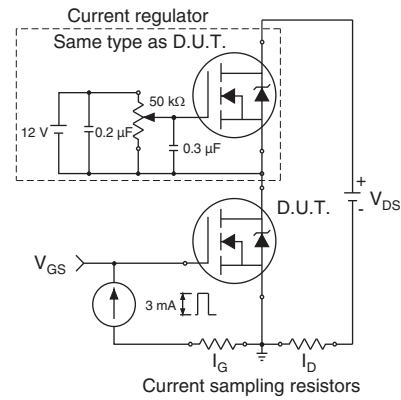
**Fig. 12 - Switching Time Test Circuit**



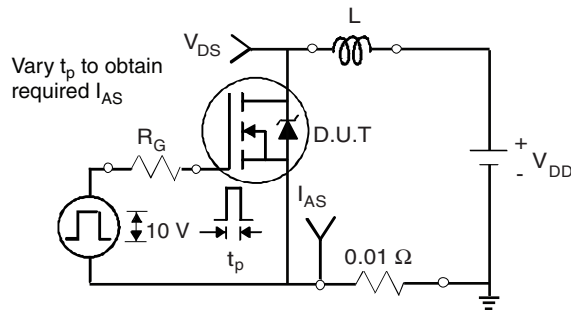
**Fig. 16 - Basic Gate Charge Waveform**



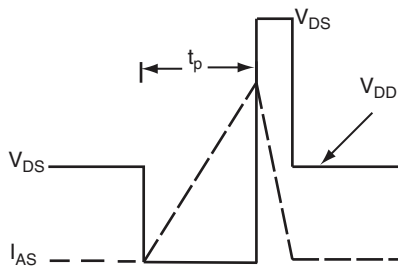
**Fig. 13 - Switching Time Waveforms**



**Fig. 17 - Gate Charge Test Circuit**



**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 18 - For N-Channel

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## TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

### Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.



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