Normally – OFF Silicon Carbide Junction Transistor

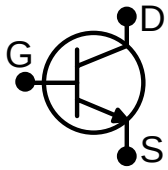
V_{DS}	=	600 V
$R_{DS(ON)}$	=	60 mΩ
$I_{D\ (Tc\ =\ 25°C)}$	=	32 A
$h_{FE\ (Tc\ =\ 25°C)}$	=	80

Features

- 225°C maximum operating temperature
- Electrically Isolated Base Plate
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Compatible with 5 V TTL Gate Drive
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

- RoHS Compliant



TO – 257 (Isolated Base-plate Hermetic Package)

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling
- Geothermal Instrumentation
- Solenoid Actuators
- General Purpose High-Temperature Switching
- Amplifiers
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	600	V
Continuous Drain Current	I_D	T_J = 225°C, T_C = 25°C	32	A
Gate Peak Current	I_{GM}		2	A
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 225°C, I_G = 1.5 A, Clamped Inductive Load	$I_{D,max}$ = 32 @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 225°C, I_G = 1.5 A, V_{DS} = 400 V, Non Repetitive	>20	µs
Reverse Gate – Source Voltage	V_{GS}		30	V
Reverse Drain – Source Voltage	V_{DS}		40	V
Power Dissipation	P_{tot}	T_J = 225°C, T_C = 25°C	172	W
Operating and Storage Temperature	T_j, T_{stg}		-55 to 225	°C

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
A: On State						
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 20 A, T_j = 25 °C I_D = 20 A, T_j = 125 °C I_D = 20 A, T_j = 175 °C I_D = 20 A, T_j = 250 °C		60 96 128 155		mΩ
Gate – Source Saturation Voltage	$V_{GS,SAT}$	I_D = 20 A, I_D/I_G = 40, T_j = 25 °C I_D = 20 A, I_D/I_G = 30, T_j = 175 °C		3.44 3.24		V
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 20 A, T_j = 25 °C V_{DS} = 5 V, I_D = 20 A, T_j = 125 °C V_{DS} = 5 V, I_D = 20 A, T_j = 175 °C V_{DS} = 5 V, I_D = 20 A, T_j = 250 °C		80 50 43 35		
B: Off State						
Drain Leakage Current	I_{DSS}	V_R = 600 V, V_{GS} = 0 V, T_j = 25 °C V_R = 600 V, V_{GS} = 0 V, T_j = 175 °C V_R = 600 V, V_{GS} = 0 V, T_j = 250 °C		3 10 50		μA
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA
C: Thermal						
Thermal resistance, junction - case	R_{thJC}			1.16		°C/W

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit	
A: Capacitance and Gate Charge							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 100 V, f = 1 MHz		2500		pF	
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 100 V, f = 1 MHz		158		pF	
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_D = 100 V, *f* = 1 MHz		0.8		μJ	
Effective Output Capacitance, time related	$C_{oss,tr}$	I_D = constant, V_{GS} = 0 V, V_{DS} = 0…100 V		260		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	V_{GS} = 0 V, V_{DS} = 0…100 V		202		pF	
Gate-Source Charge	Q_{GS}	V_{GS} = -5…3 V		27		nC	
Gate-Drain Charge	Q_{GD}	V_{GS} = 0 V, V_{DS} = 0…100 V		26		nC	
Gate Charge - Total	Q_G			53		nC	
B: Switching[1]							
Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	*f* = 1 MHz, V_{AC} = 50 mV, V_{DS} = V_{GS} = 0 V, T_j = 225 ºC		2.6		Ω	
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 225 ºC		0.16		Ω	
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 400 V,		90		ns	
Fall Time, V_{DS}	t_f	I_D = 20 A, Inductive Load		80		ns	Fig. 11, 13
Turn Off Delay Time	$t_{d(off)}$	Refer to Section V: for additional		50		ns	
Rise Time, V_{DS}	t_r	driving information		55		ns	Fig. 12, 14
Turn On Delay Time	$t_{d(on)}$	T_j = 225 ºC, V_{DS} = 400 V,		90		ns	
Fall Time, V_{DS}	t_f	I_D = 20 A, Inductive Load		85		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$	Refer to Section V: for additional		50		ns	
Rise Time, V_{DS}	t_r	driving information		50		ns	Fig. 12
Turn-On Energy Per Pulse	E_{on}	T_j = 25 ºC, V_{DS} = 400 V,		810		μJ	Fig. 11, 13
Turn-Off Energy Per Pulse	E_{off}	I_D = 20 A, Inductive Load		95		μJ	Fig. 12, 14
Total Switching Energy	E_{tot}			905		μJ	
Turn-On Energy Per Pulse	E_{on}	T_j = 225 ºC, V_{DS} = 400 V,		140		μJ	Fig. 11
Turn-Off Energy Per Pulse	E_{off}	I_D = 20 A, Inductive Load		45		μJ	Fig. 12
Total Switching Energy	E_{tot}			185		μJ	

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

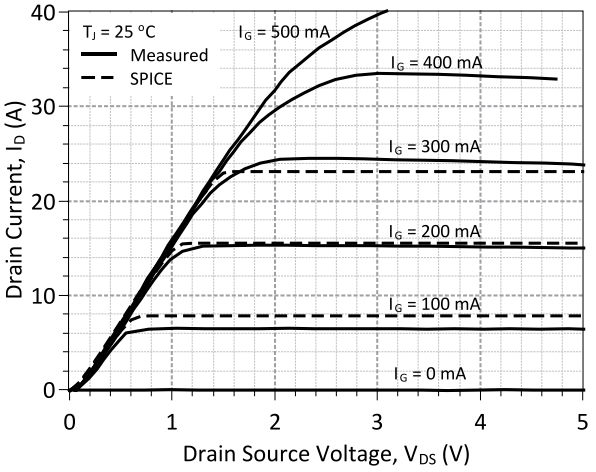


Figure 1: Typical Output Characteristics at 25 °C

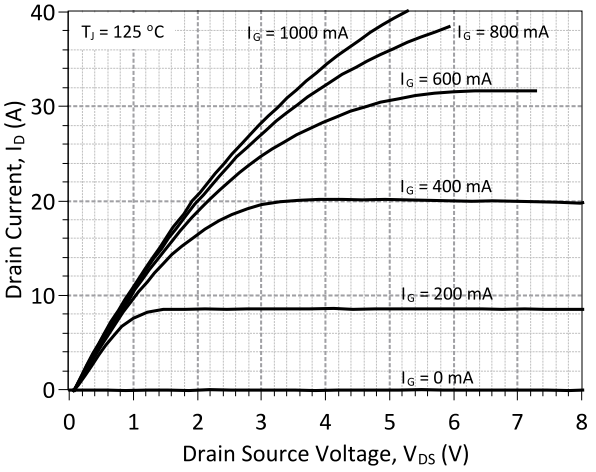


Figure 2: Typical Output Characteristics at 125 °C

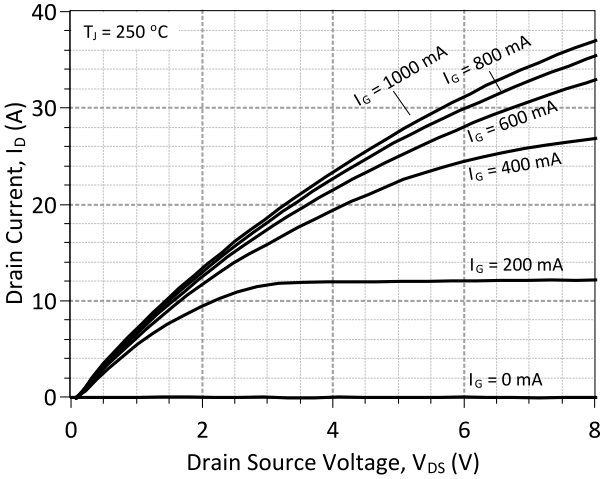


Figure 3: Typical Output Characteristics at 250 °C

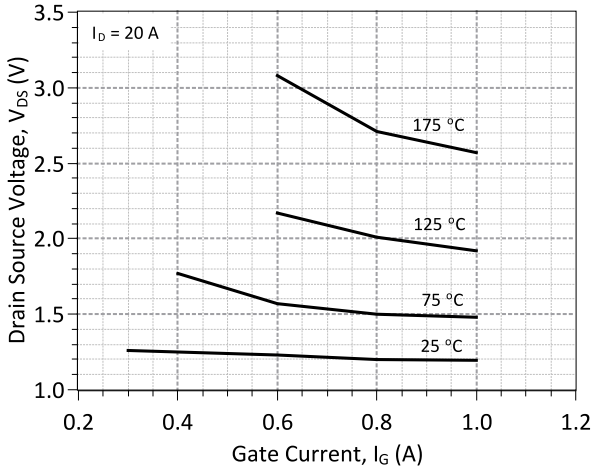


Figure 4: Drain-Source Voltage vs. Gate Current

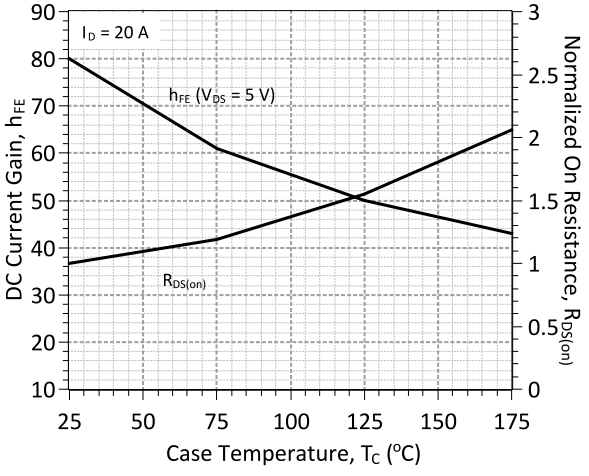


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

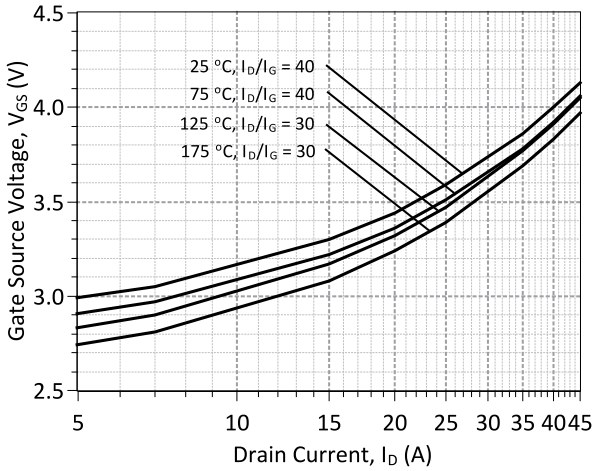


Figure 6: Typical Gate – Source Saturation Voltage

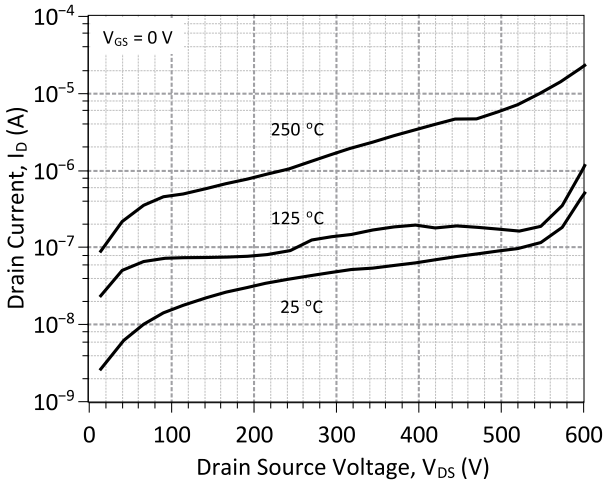


Figure 7: Typical Blocking Characteristics

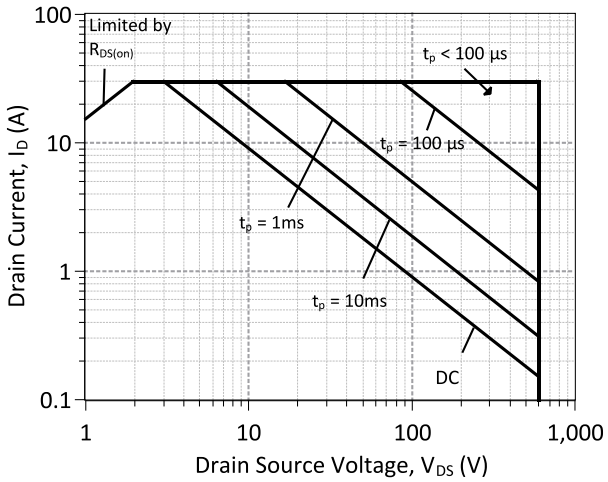


Figure 8: Forward Bias Safe Operating Area at T_c=120 °C

B: Dynamic Characteristics

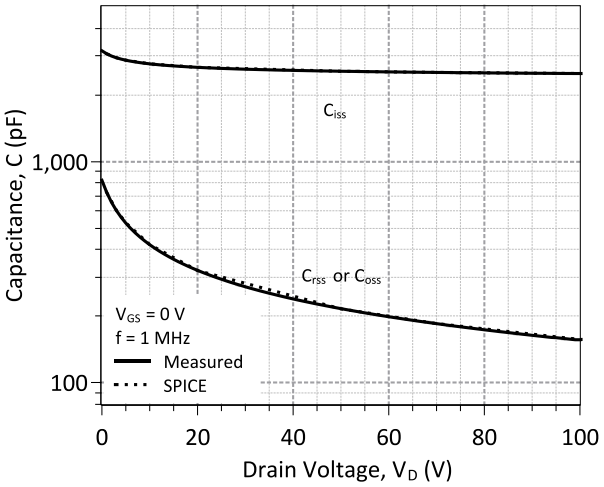


Figure 9: Capacitance Characteristics

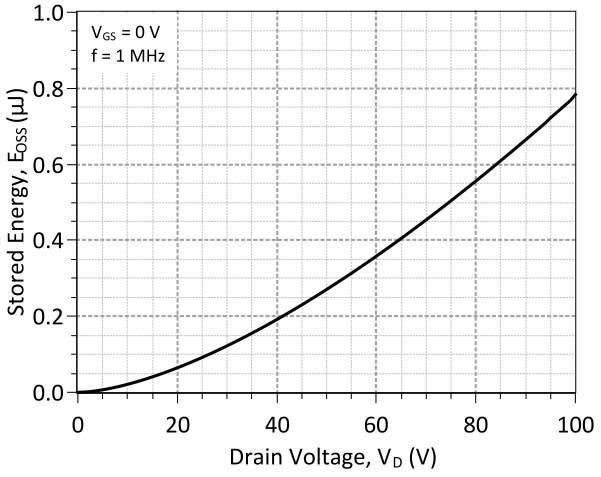


Figure 10: Output Capacitance Stored Energy

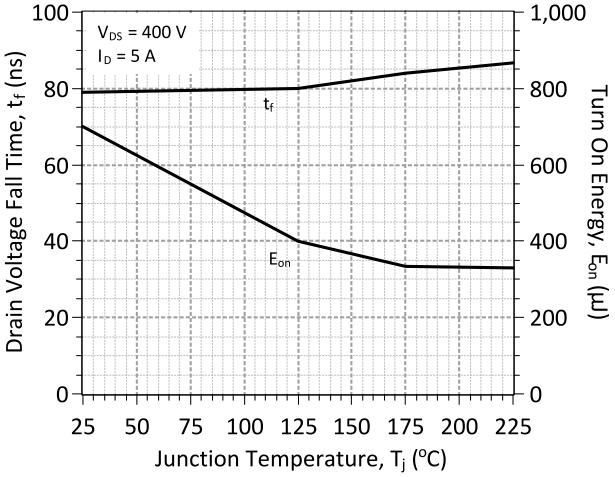


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

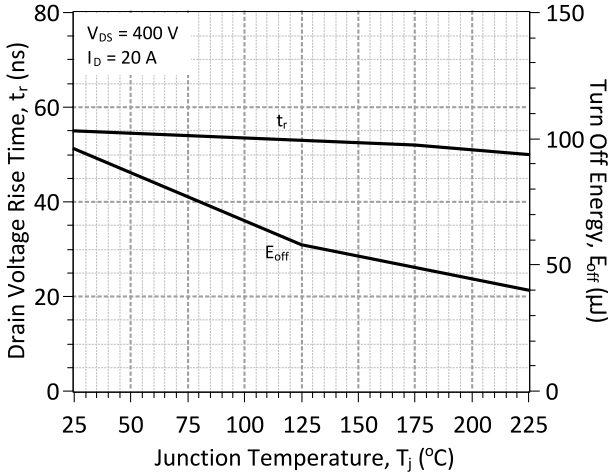


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

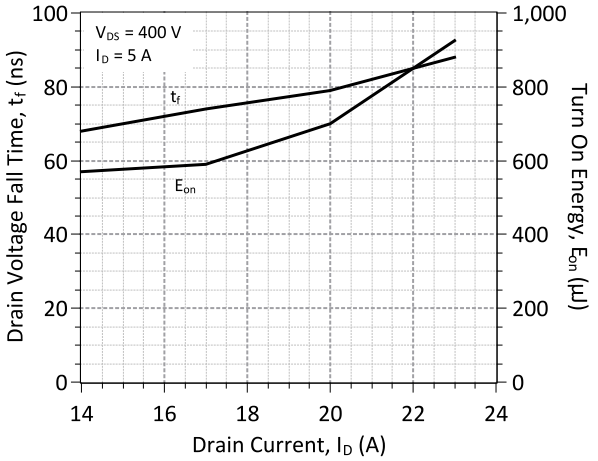


Figure 13: Typical Turn On Energy Losses and Switching Times vs. Drain Current

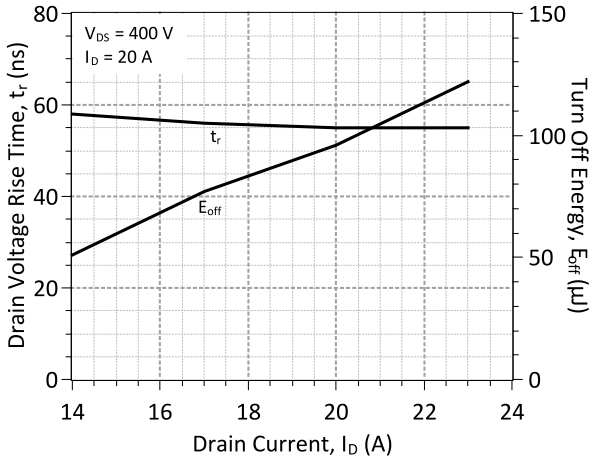


Figure 14: Typical Turn Off Energy Losses and Switching Times vs. Drain Current

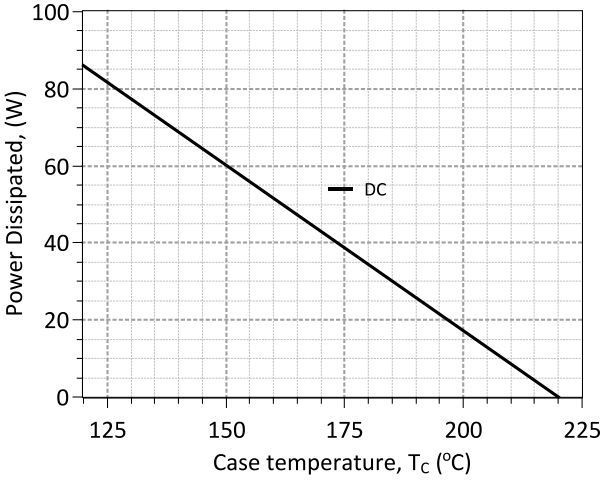


Figure 15: Power Derating Curve

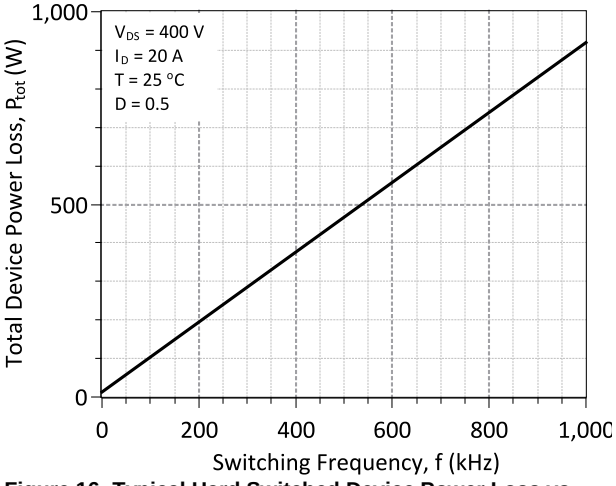


Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [2]

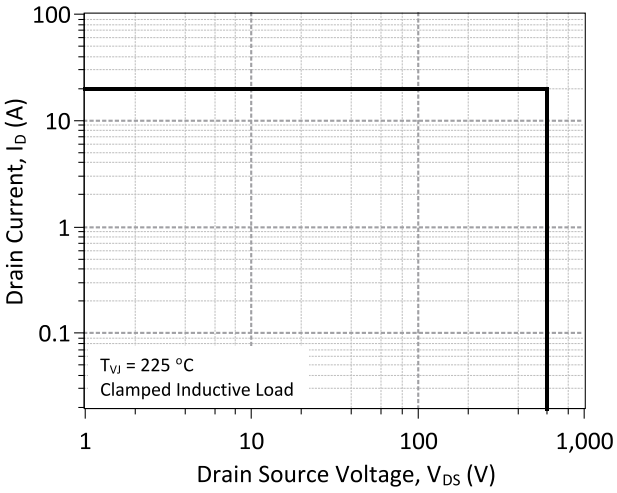


Figure 17: Turn-Off Safe Operating Area

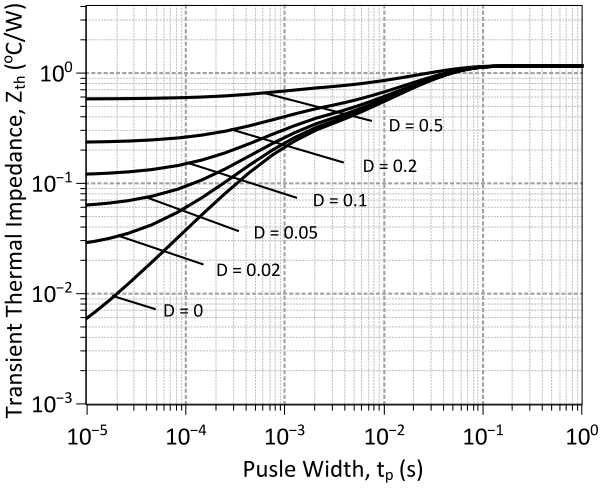


Figure 18: Transient Thermal Impedance

[2] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Section V: Driving the 2N7639-GA

The 2N7639-GA is a current controlled SiC transistor which requires a positive gate current for turn-on and to remain in on-state. It may be driven by different drive topologies depending on the intended application.

Table 1: Estimated Power Consumption and switching frequencies for various Gate Drive topologies.

Drive Topology	Gate Drive Power Consumption	Switching Frequency
Simple TTL	High	Low
Constant Current	Medium	Medium
High Speed – Boost Capacitor	Medium	High
High Speed – Boost Inductor	Low	High
Proportional	Lowest	Medium
Pulsed Power	Medium	N/A

A: Simple TTL Drive

The 2N7639-GA may be driven by 5 V TTL logic by using a simple current amplification stage. The current amplifier output current must meet or exceed the steady state gate current, $I_{G,steady,}$ required to operate the 2N7639-GA. An external gate resistor R_G, shown in the Figure 19 topology, sets $I_{G,steady}$ to the required level which is dependent on the SJT drain current I_D and DC current gain h_{FE}, R_G may be calculated from the equation below. The values of h_{FE} and $V_{GS,sat}$ may be read from Figure 5 and Figure 6, respectively. $V_{EC,sat}$ can be taken from the PNP datasheet, a partial list of high-temperature PNP and NPN transistors options is given below. High-temperature MOSFETs may also be used in the topology.

$$R_{G,max} = \frac{\left(5.0\ V - V_{EC,sat}(PNP) - V_{GS,sat}(SJT)\right) * h_{FE}(T, I_D)}{I_D * 1.5}$$

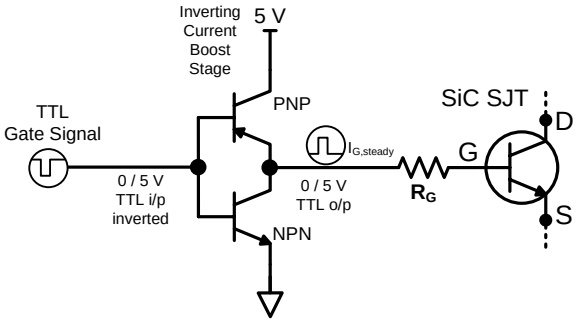


Figure 19: Simple TTL Gate Drive Topology

Table 2: Partial List of High-Temperature BJTs for TTL Gate Driving

BJT Part Number	Type	$T_{j,max}$ (°C)
PHPT60603PY	PNP	175
PHPT60603NY	NPN	175
2N2222	NPN	200
2N6730	PNP	200
2N2905	PNP	200
2N5883	PNP	200
2N5885	NPN	200

B: High Speed Driving

For ultra high speed 2N7639-GA switching (t_r, t_f < 20 ns) while maintaining low gate drive losses the supplied gate current should include a positive current peak during turn-on, a negative voltage peak during turn-off, and continuous gate current I_G to remain on.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge for turn-on, Q_G, is supplied by a burst of high gate current until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged. Ideally, the burst should terminate when the drain voltage has fallen to its on-state value in order to avoid unnecessary drive losses. A negative voltage peak is recommended for the turn-off transition in order to ensure that the gate current is not being supplied under high dV/dt due to the Miller effect. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative V_{GS} value may be used in order to speed up the turn-off transition.

B:1: High Speed, Low Loss Drive with Boost Capacitor

The 2N7639-GA may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide current peaks at turn-on and turn-off for fast switching and a continuous gate current while in on-state. As shown in Figure 20, in this topology two gate driver ICs are utilized. An external gate resistor R_G is driven by a low voltage driver to supply the continuous gate current throughout on-state.and a gate capacitor C_G is driven at a higher voltage level to supply a high current peak at turn-on and turn-off. A 3 kV isolated evaluation gate drive board (GA03IDDJT30-FR4) from GeneSiC Semiconductor utilizing this topology is commercially available for high and low-side driving, its datasheet provides additional details about this drive topology.

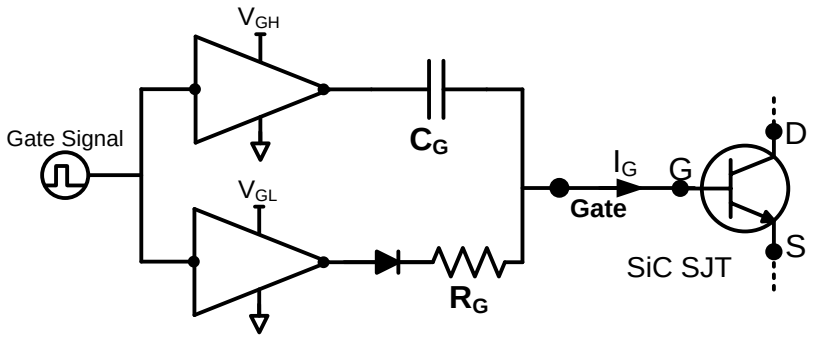


Figure 20: High Speed, Low Loss Drive with Boost Capacitor Topology

B:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the 2N7639-GA at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SJT gate pin using logic control of S_1, S_2, S_3, and S_4, as shown in Figure 21. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G. Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.[3]

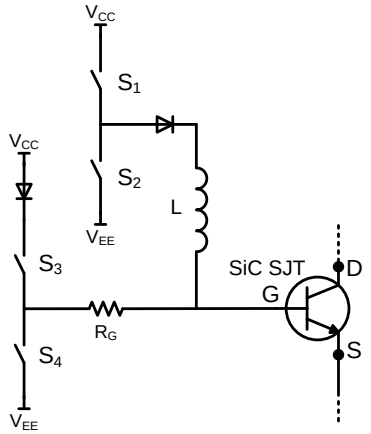


Figure 21: High Speed, Low-Loss Driver with Boost Inductor Topology

[3] – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/aee-2013-0026, June 2013

C: Proportional Gate Current Driving

A proportional gate drive topology may be beneficial for applications in which the 2N7639-GA will operate over a wide range of drain current conditions to lower the gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the 2N7639-GA.

C:1: Voltage Controlled Proportional Driver

A voltage controlled proportional driver relies on a gate drive integrated circuit to detect the 2N7639-GA drain-source voltage V_{DS} during on-state to sense I_D. The integrated circuit will then increase or decrease I_G in response to I_D. This allows I_G and gate drive power consumption to reduce while I_D is low or for I_G to increase when I_D increases. A high voltage diode connected between the drain and sense protects the integrated circuit from high-voltage when blocking. A simplified version of this topology is shown in Figure 22. Additional information will be available in the future at http://www.genesicsemi.com/references/product-notes/.

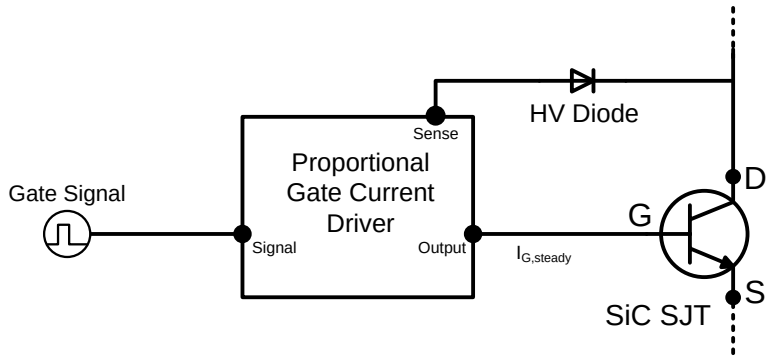


Figure 22: Simplified Voltage Controlled Proportional Driver

C:2: Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback of the 2N7639-GA drain current during on-state to supply $I_{G,steady}$ into the gate. $I_{G,steady}$ will increase or decrease in response to I_D at a fixed forced current gain which is set be the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. 2N7639-GA is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$ and the gate drive power consumption to reduce while I_D is relatively low or for $I_{G,steady}$ to increase when I_D increases. A simplified version of this topology is shown in Figure 23. Additional information will be available in the future at http://www.genesicsemi.com/references/product-notes/.

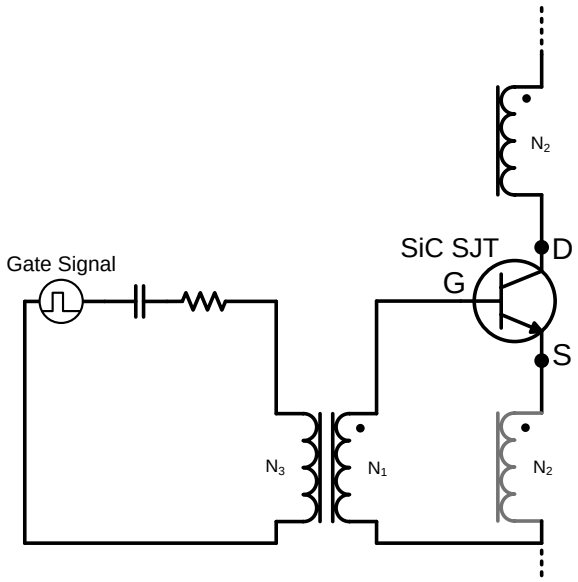
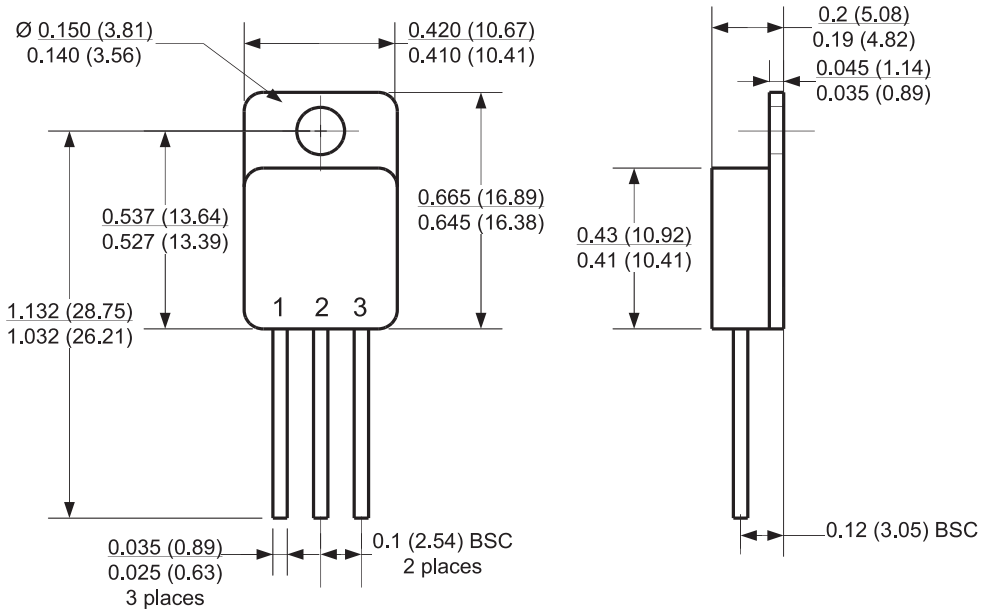


Figure 23: Simplified Current Controlled Proportional Driver

Section VI: Package Dimensions

TO-257 PACKAGE OUTLINE



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/12/12	5	Updated Electrical Characteristics	
2014/08/25	4	Updated Electrical Characteristics	
2014/03/18	3	Updated Gate Drive Section	
2013/12/19	2	Updated Gate Drive Section	
2013/11/18	1	Updated Electrical Characteristics	
2012/08/24	0	Initial release	

Published by
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43670 Trade Center Place Suite 155
Dulles, VA 20166

Section VII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/sjt/2N7639-GA_SPICE.pdf) into LTSPICE (version 4) software for simulation of the 2N7639-GA.

```
*       MODEL OF GeneSiC Semiconductor Inc.
*
*       $Revision:   1.3              $
*       $Date:   12-DEC-2014          $
*
*       GeneSiC Semiconductor Inc.
*       43670 Trade Center Place Ste. 155
*       Dulles, VA 20166
*
*       COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*       ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model 2N7639-GA NPN
+ IS           9.8338E-48
+ ISE          1.0733E-26
+ EG           3.23
+ BF           110
+ BR           0.55
+ IKF          200
+ NF           1.02
+ NE           2.0
+ RB           2.6
+ IRB          0.002
+ RBM          0.16
+ RE           0.01
+ RC           0.045
+ CJC          8.2281E-10
+ VJC          3.31126
+ MJC          0.48117
+ CJE          2.33957E-9
+ VJE          2.91486
+ MJE          0.48211
+ XTI          3
+ XTB          -1.2
+ TRC1         6.20E-03
+ VCEO         600
+ ICRATING     32
+ MFG          GeneSiC_Semiconductor
*
* End of 2N7639-GA SPICE Model
```