SQD50N03-06P

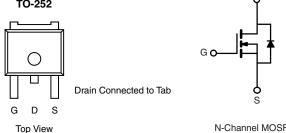


Vishay Siliconix

Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	30				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0060				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 V$	0.0085				
I _D (A)	50				
Configuration	Single				

TO-252



FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_q and UIS Tested
- AEC-Q101 Qualified
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



N-Channel MOSFET

D

ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50N03-06P-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20	V	
Continuous Drain Current ^a	T _C = 25 °C	- I _D	50		
	T _C = 125 °C		50		
Continuous Source Current (Diode Conduction) ^a		I _S	50	А	
Pulsed Drain Current ^b		I _{DM}	200		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	45		
Single Pulse Avalanche Energy	L = 0.1 MH	E _{AS}	101	mJ	
Mauinung Dauren Diagin atiant	T _C = 25 °C	D	83	W	
Maximum Power Dissipation ^b	T _C = 125 °C	P _D	27	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	50	°C/W
Junction-to-Case (Drain)		R _{thJC}	1.8	C/W

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR-4 material).

Document Number: 68634

SQD50N03-06P



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$		30	-	-	N	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	V _{DS} = V _{GS} , I _D = 250 μA		2.0	2.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 30 V	-	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 30 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 30 V, T _J = 175 °C	-	-	250		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α	
		V _{GS} = 10 V	I _D = 20 A	-	0.0047	0.0060	Ω	
Drain-Source On-State Resistance ^a	Р	V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0090		
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 20 A, T _J = 175 °C	-	-	0.0107		
		V _{GS} = 4.5 V	I _D = 20 A	-	0.0067	0.0085		
Forward Transconductanceb	9 _{fs}	V _{DS}	V _{DS} = 15 V, I _D = 20 A		74	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}			-	3222	4030		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$) V V _{DS} = 25 V, f = 1 MHz		563	705	pF	
Reverse Transfer Capacitance	C _{rss}]		-	241	300		
Total Gate Charge ^c	Qg			-	25.2	38		
Gate-Source Charge ^c	Q _{gs}	$V_{GS} = 4.5 V$	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 50 \text{ A}$	-	9.1	-	nC	
Gate-Drain Charge ^c	Q _{gd}]		-	9.4	-		
Gate Resistance	Rg	f = 1 MHz		0.5	1.6	2.8	Ω	
Turn-On Delay Time ^c	t _{d(on)}	$\begin{array}{l} V_{\text{DD}} = 15 \; V, \; R_{L} = 0.3 \; \Omega \\ I_{\text{D}} \cong 50 \; A, \; V_{\text{GEN}} = 10 \; V, \; R_{\text{g}} = 1 \; \Omega \end{array}$		-	10	15		
Rise Time ^c	t _r			-	10	15	ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	26	39		
Fall Time ^c	t _f			-	9	14		
Source-Drain Diode Ratings and Char	acteristics ^b				·			
Pulsed Current ^a	I _{SM}			-	-	200	Α	
Forward Voltage	V _{SD}	I _F = 85 A, V _{GS} = 0 V		-	1	1.5	V	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

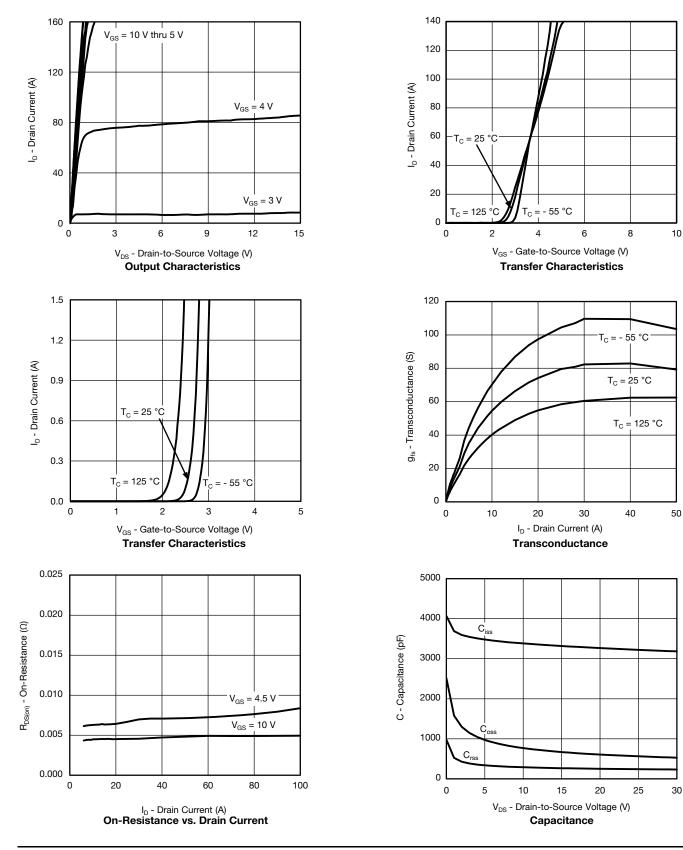
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SQD50N03-06P

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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



S12-2198-Rev. E, 24-Sep-12

3

For technical questions, contact: <u>automostechsupport@vishay.com</u> THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT <u>www.vishay.com/doc?91000</u> V_{DS} = 15 V

www.vishay.com

= 50 A

I_D

10

8

6

4

2

0

0

10

20

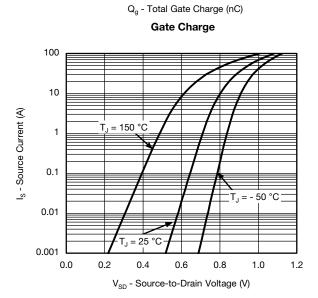
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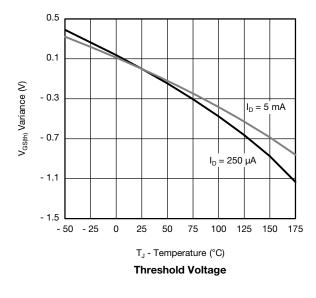
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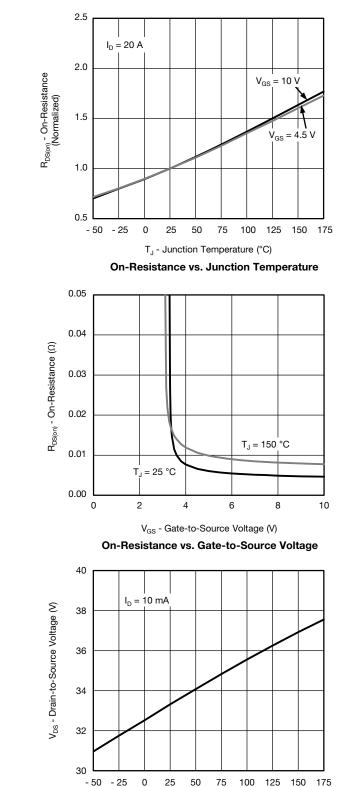
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V_{GS} - Gate-to-Source Voltage (V)



Source Drain Diode Forward Voltage





T_J - Junction Temperature (°C) Drain Source Breakdown vs. Junction Temperature

SQD50N03-06P Vishay Siliconix

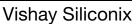
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

S12-2198-Rev. E, 24-Sep-12

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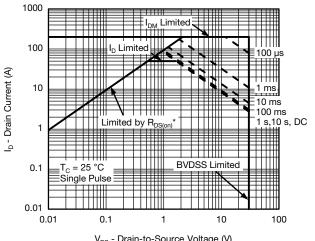
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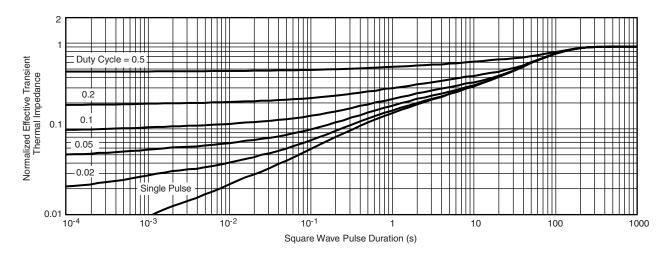




THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



 $\label{eq:V_S} \begin{array}{l} V_{DS} \mbox{-} Drain-to-Source Voltage (V) \\ * \, V_{GS} \mbox{-} minimum \, V_{GS} \mbox{ at which } R_{DS(on)} \mbox{ is specified} \\ \hline { { Safe Operating Area} } \end{array}$

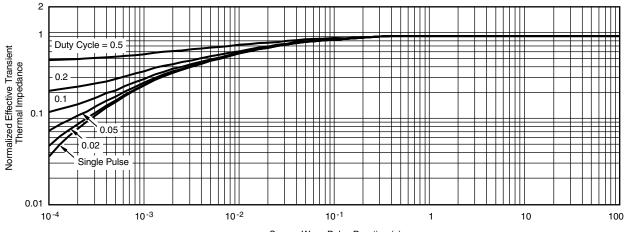


Normalized Thermal Transient Impedance, Junction-to-Ambient



Vishay Siliconix

THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Case

Note

The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68634.





Е b3 Ľ Δ ŝ b2 e1 Б E1

C2 т gage plane height (0.5 mm)

-C

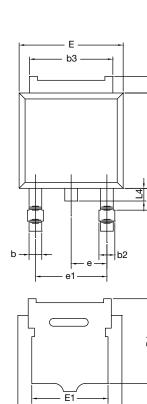
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TO-252AA Case Outline

	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019					

Note

• Dimension L3 is for reference only.





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RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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