CY3679 EVK

CY3679 Evaluation Kit User Guide

Doc. # 001-95978 Rev**

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): +1.408.943.2600
www.cypress.com

Copyrights

Source Code

Disclaimer

Trademarks

Flash Code Protection

Contents

Safety Information

The CY3679 Evaluation Kit is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure, so the board may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In such cases, the user may be required to take adequate preventive measures. Also, this board should not be used near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

	The CY3679 Evaluation Kit contains electrostatic discharge (ESD)-sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY3679 Evaluation Kit boards in the protective shipping package.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that the user perform procedures only at an ESD workstation. If ESD workstation is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to the chassis ground (any unpainted metal surface) on the board when handling parts.

Handling Boards

CY3679 Evaluation Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1 Introduction

Thank you for your interest in CY3679 Evaluation Kit (EVK). CY3679 EVK is designed to enable you to evaluate the programmable clock device CY27410, the latest addition to programmable devices in Cypress's timing product portfolio. The clock device CY27410 is a high-performance programmable clock generator with four independent fractional PLLs that generates any frequency with a zero-ppm synthesis error. The device offers eight differential and four single-ended outputs and comes in a 48-pin QFN package for industrial applications. The differential outputs can also be configured as single-ended. The differential I/O standards supported are LVDS (Low Voltage Differential Signaling), LVPECL (Low-Voltage Positive Emitter-Coupled Logic), HCSL (High-Speed Current steering logic) and CML (Current Mode Logic). The single–ended I/O standard supported is LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor). The device also supports features like voltage-controlled crystal oscillator (VCXO), I^2C, and Frequency Select options.

This kit allows you to evaluate both AC and DC parameters of the output signals by making required on-board termination settings.

This kit is available through the Cypress Online Store or through our distributors.

1.1 CY3679 EVK Contents

The CY3679 EVK includes the following:

- CY3679 Evaluation Board
- Power cables (banana to 2-pin housing cables) for external supply
- Jumper shunts
- USB Standard-A to Mini-B cable
- Quick Start Guide

Figure 1-1. Kit Contents

Inspect the contents of the kit. If you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/go/support

1.2 Getting Started

To learn the solution quickly and apply it to your design, see the Quick Start Guide inside the kit box or in the installation directory. The default location for the kit documents is:

```
<Install_Directory>\CY3679 EVALUATION KIT\<version>\Documentation
```

This guide will help you get acquainted with the CY3679 Evaluation Kit:

- The Software Installation chapter describes the installation of the kit software.
- The Kit Operation chapter describes the major feature of CY3679 Evaluation kit such as evaluating the clock device.
- The Hardware chapter describes the hardware content of the CY3679 Evaluation Kit and the hardware operation.
- The Sample Profiles chapter describes the multiple profiles that will help you understand how to evaluate different supported output standards on this kit. These profiles can be evaluated with the default termination settings on the board.
- The Appendix captures DC/AC Measurements of Clock Outputs, Schematics, Fab Drawing, and the bill of materials (BOM).

1.3 Additional Learning Resources

Visit www.cypress.com/go/CY3679 and www.cypress.com/go/CY27410 for additional learning resources including datasheets and application notes.

1.4 Technical Support

For assistance, go to our support: www.cypress.com/support web page, or contact our customer support at +1(800) 541-4736 Ext. 2 (in the USA), or +1 (408) 943-2600 Ext. 2 (International).

1.5 Document Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: C:\ ...cd\icc\
Italics	Displays file names and reference documentation.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

1.6 Acronyms

Table 1-2. List of Acronyms used in this document

Acronym	Definition
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVDS	Low Voltage Differential Signaling
HCSL	High speed Current Steering Logic
CML	Current Mirror Logic
SMA	Subminiature version A
DNP, DNM	Do Not Populate, Do Not Mount
SS	Spread Spectrum
ZDB	Zero Delay Buffer
NZDB	Non-Zero Delay Buffer
PCIe	PCI Express
I^2C	Inter-Integrated Circuit
LDO	Low-Dropout

2 Software Installation

This chapter describes the steps to install the software tools and packages on a PC for using the CY3679 Evaluation Kit.

2.1 Before You Begin

All Cypress software installations require administrator privileges. Ensure that you have the required privileges on the system for successful installation. Before you install the kit software, close any other Cypress software that is currently running.

2.2 Install Software

Follow these steps to install the CY3679 Evaluation Kit software:

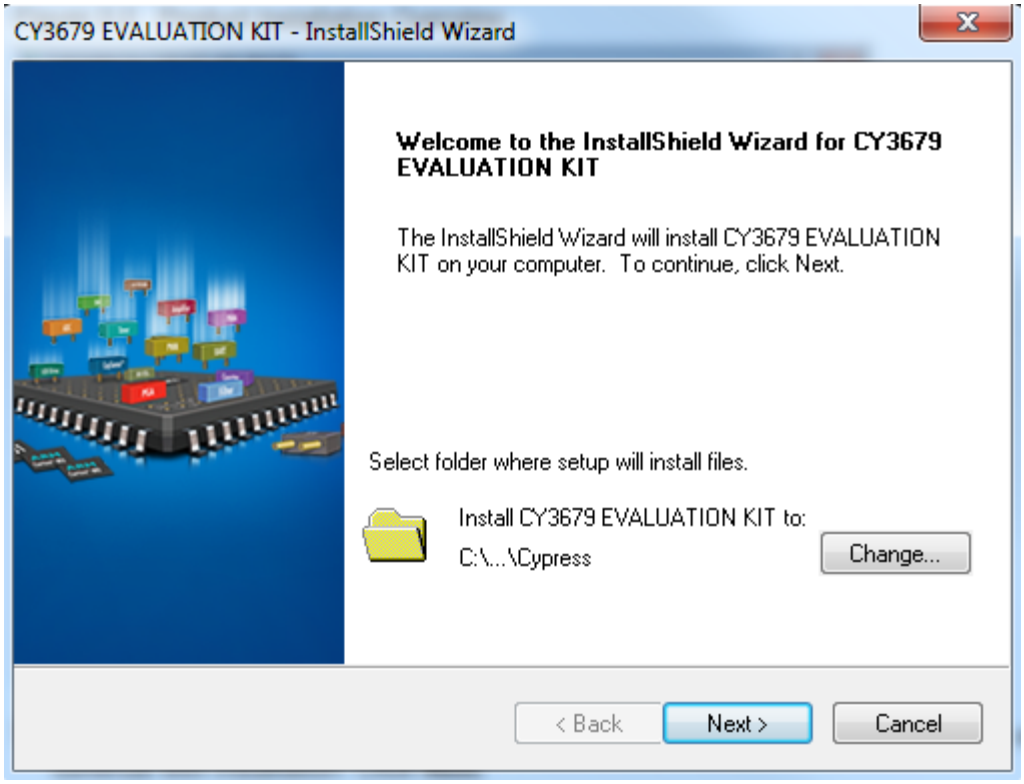
1. Download the CY3679 Evaluation Kit software from www.cypress.com/go/CY3679. The software is available in the following formats:
   a. **CY3679 Evaluation Kit Complete Setup:** This installation package contains the files related to the CY3679 Evaluation Kit. However, it does not include the Windows Installer or Microsoft .NET framework packages. If these packages are not available on your computer, the installer directs you to download and install them from the Internet.
   b. **CY3679 Evaluation Kit Only Package:** This executable file installs only the CY3679 Evaluation Kit contents, which include sample profiles, hardware files, and user documents. This package can be used if all the software prerequisites (listed in **step 5**) are installed on your PC.
   c. **CY3679 Evaluation Kit DVD ISO:** This file is a complete package, stored in a DVD-ROM image format that you can use to create a DVD or extract using an ISO extraction program such as WinZip or WinRAR. The file can also be mounted similar to a virtual CD/DVD using virtual drive programs such as Virtual CloneDrive and MagicISO. This file includes all the required software, utilities, drivers, hardware files, and user documents.
2. If you have downloaded the ISO file, mount it on a virtual drive. If you do not have a virtual drive to mount, extract the ISO contents using the appropriate ISO extractor (such as MagicISO or PowerISO). Double-click *cyautorun.exe* in the root directory of the extracted content or the mounted ISO if the “Autorun from CD/DVD” option is not enabled on the PC. The installation window will appear automatically.

   Note: If you are using the “Kit Complete Setup” or “Kit Only Package” file, then go to step 4 for installation
3. Click **Install CY3679 EVALUATION KIT** to start the installation, as shown in Figure 2-1..

Figure 2-1. Installer Screen

4. Select the folder in which you want to install the files related to CY3679 Evaluation Kit. Choose the directory and click **Next** as shown in Figure 2-2.

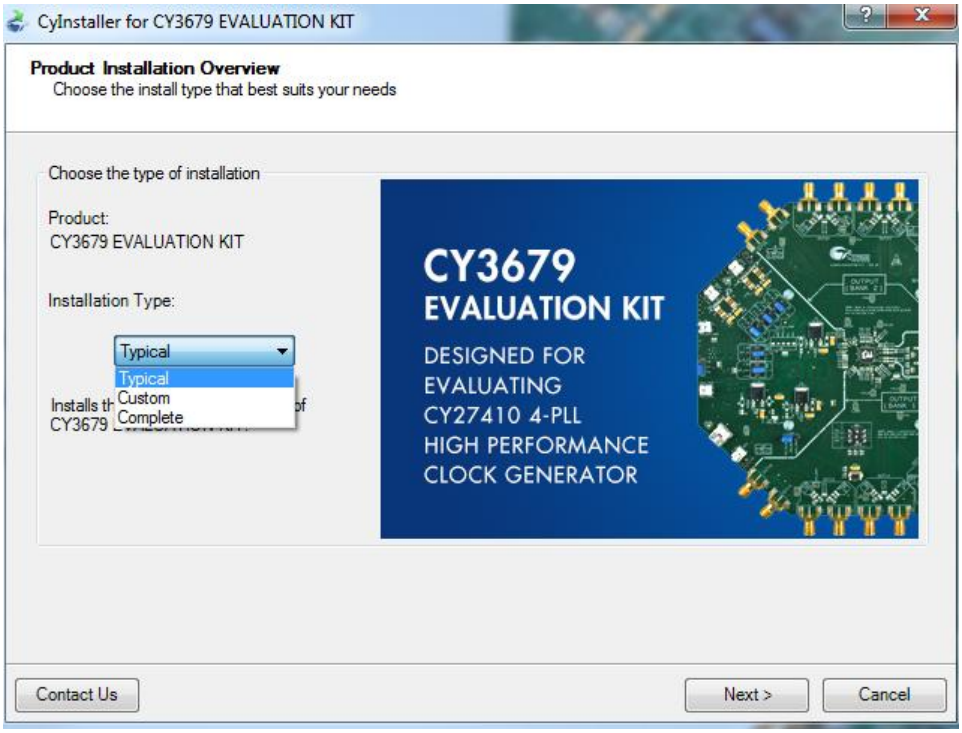
Figure 2-2. InstallShield Wizard



5. When you click **Next,** the CY3679 Evaluation Kit installer automatically installs the required software, if it is not present on your computer. The pre-requisite is PSoC Programmer 3.22.2 or later.

6. Choose the installation type in the Product Installation Overview window, as shown in Figure 2-3. Click **Next** after you select the installation type.

Figure 2-3. Product Installation Overview



7. Read the license agreement and select **I accept the terms in the license agreement** to continue with installation. Click **Next**.

   When the installation begins, a list of packages appears on the installation page. A green check mark appears next to each package after successful installation.

8. Click **Finish** to complete the CY3679 Evaluation Kit installation.
9. Enter your contact information or select the **Continue Without Contact Information** check box.
10. Click **Finish** to complete the CY3679 Evaluation Kit installation.

    After the installation is complete, the kit contents are available at:

    `<Install_Directory>\CY3679 EVALUATION KIT\<version>.`

    Default location:

    Windows 7 (64-bit): `C:\Program Files (x86)\Cypress\CY3679 EVALUATION KIT`

    Windows 7 (32-bit): `C:\Program Files\Cypress\CY3679 EVALUATION KIT`

2.3 Install Hardware

There is no additional hardware installation required for this kit.

2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**, and then click the **Uninstall** button for the appropriate software package.
- Go to **Start** > **Control Panel** > **Programs and Features**, and then click the **Uninstall/Change** button for the appropriate software package.

3 Kit Operation

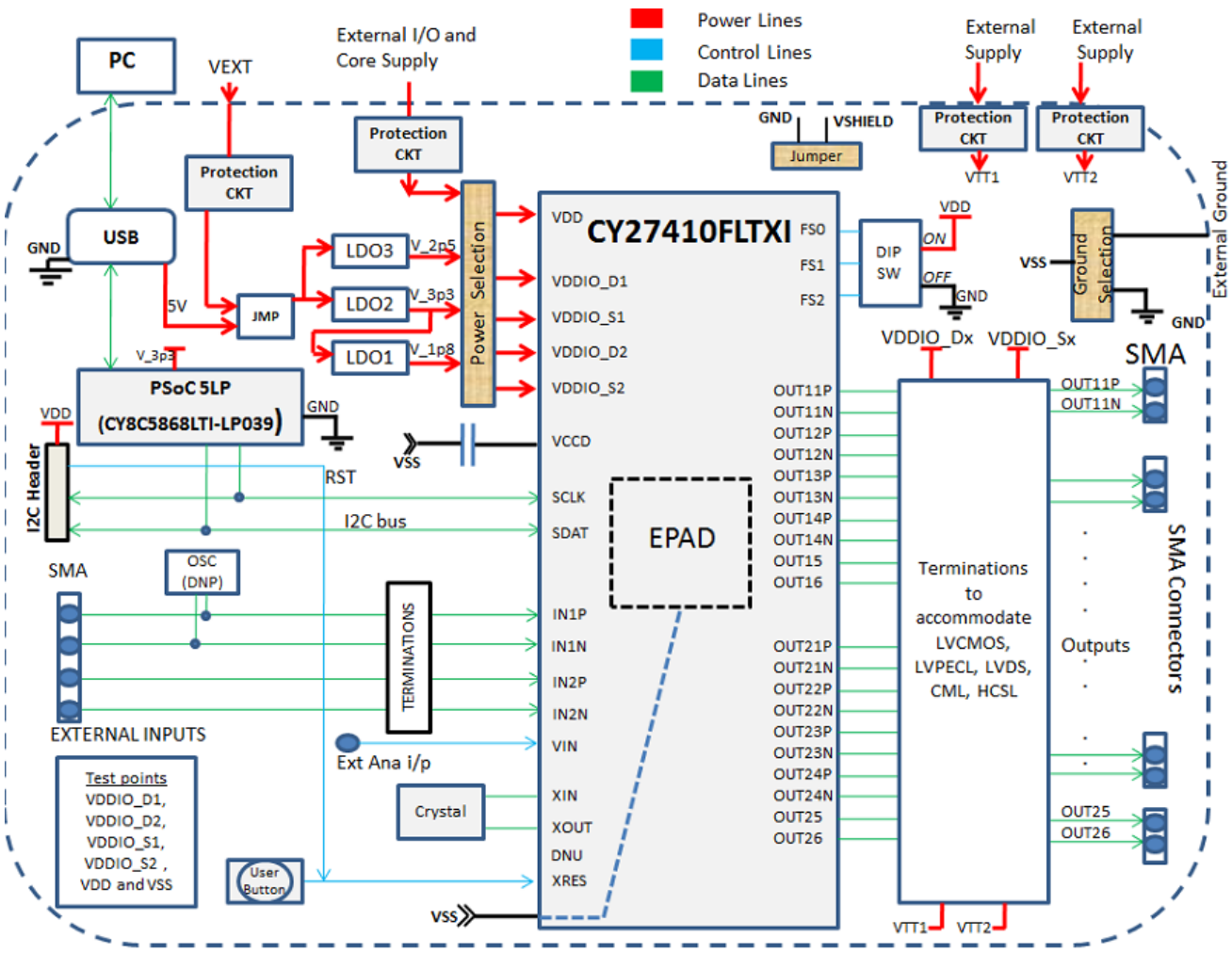
CY3679 Evaluation Kit (EVK) can be used to evaluate CY27410, a new-generation high-performance clock generator device. Connect CY3679 kit through USB to a PC running Cypress's Clock Programmer software. The clock device CY27410 can be configured and programmed to generate frequencies with best-in-class performances.

3.1 Theory of Operation

The CY3679 EVK offers twelve outputs: eight differential and four single-ended. The outputs are distributed among two banks, Bank1 and Bank2. Each bank has four differential and two single-ended outputs. Differential outputs can be configured as single-ended outputs also. The inputs to the CY27410 device on this kit can be provided either with an on-board crystal or with external clock references.

The kit is capable of generating fixed 3.3 V, 2.5 V, and 1.8 V voltages from a 5 V input (either USB or external power supply). The on-board PSoC 5LP (U7) performs the USB-to-I^2C conversion and controls one power LED and one status LED. The LDOs (U2, U3, and U4) generate fixed supply voltages of 3.3 V, 2.5 V, and 1.8 V. The block diagram of the kit is shown in Figure 3-1.

Figure 3-1. Block Diagram



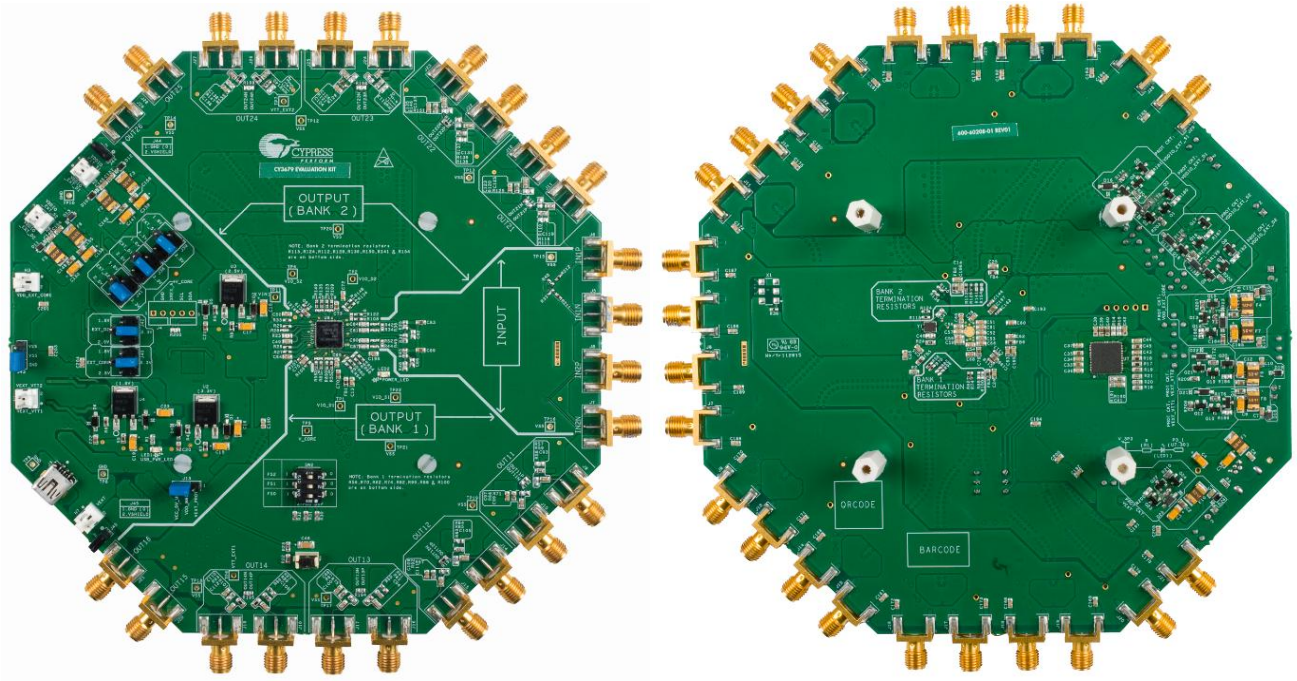
3.2 Functional Description

Each of the eight differential output drivers is AC-coupled to the SMA connectors, so the output signal will have no DC bias. If a signal with a DC bias is required or measurement is done using an active probe, the series AC-coupling capacitors can be replaced with a 0-Ω resistor. The EVK provides footprints for optional output terminations.

The termination options for differential outputs OUT11 – OUT14 and OUT21 – OUT24 in the evaluation board are listed in Evaluating Different I/O Standards Using CY3679 EVK. These termination circuits are designed to terminate the output clocks in LVPECL, LVDS, HCSL, CML, and LVCMOS signal types by populating (or by not populating) some resistors. DC or AC coupling of these outputs is also supported.

The top and bottom views of the kit are shown in Figure 3-2.

Figure 3-2. Top and Bottom Views of CY3679 Kit

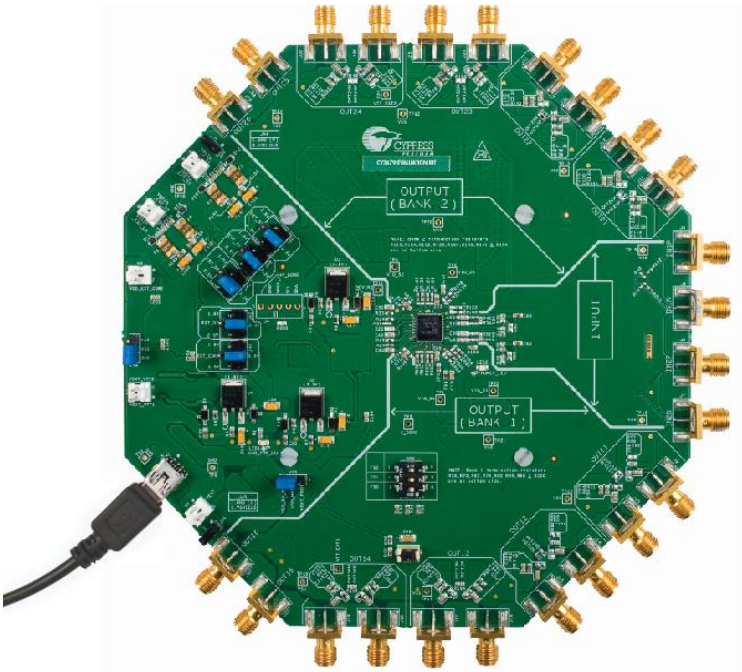


TOP View BOTTOM View

3.3 CY3679 Kit USB Connection

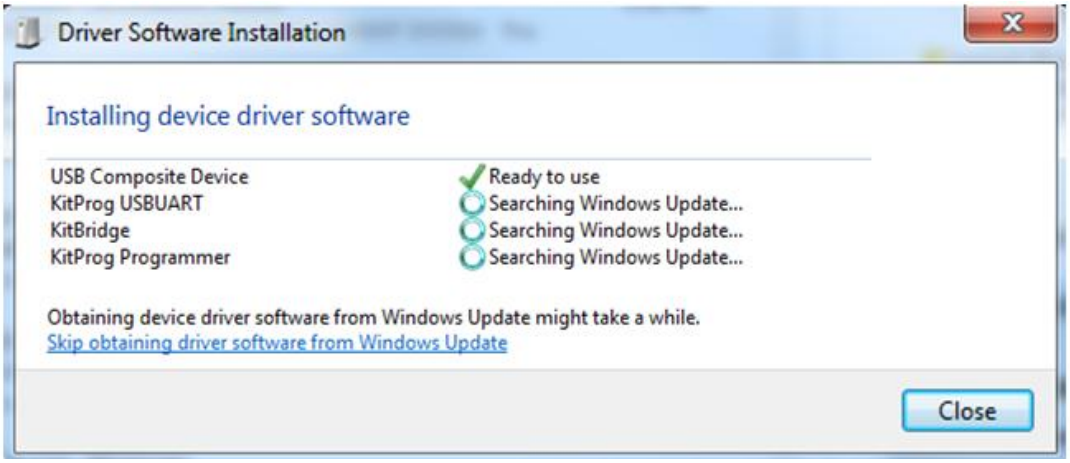
The clock device (CY27410) on the kit is loaded with a set of default profiles. For profiles other than the default profile, the clock device needs to be programmed with the desired profile. The Clock Programmer tool packaged with PSoC Programmer is required for programming any profile. Therefore, the kit should be connected (as shown in Figure 3-3) to the PC through the USB for programming.

Figure 3-3. Kit Connected through USB



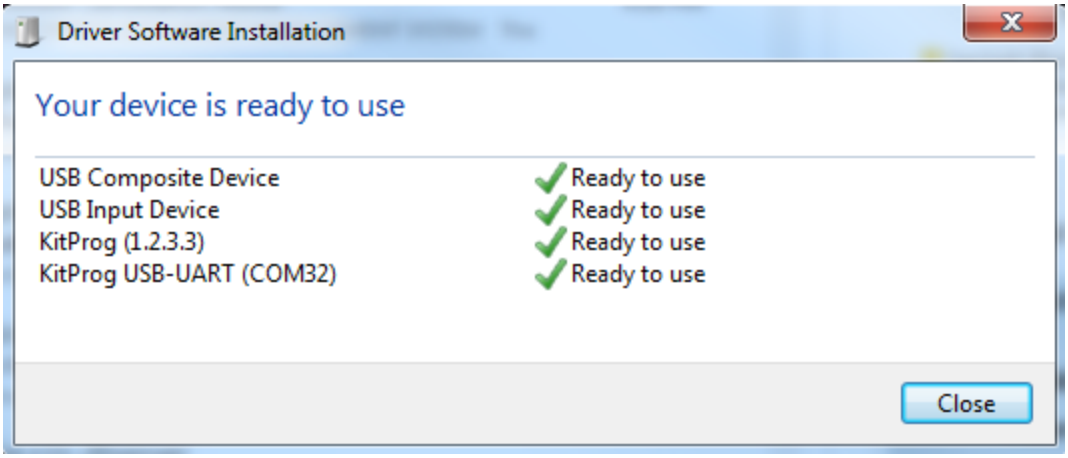
The kit enumerates as a USB Composite Device as part of the Driver Software Installation in Windows.

Figure 3-4. USB driver Installation



Once all the required drivers are installed, it shows that the device is ready to use.

Figure 3-5. USB Driver Installation Complete



3.4 Programming the Device CY27410

The sample profiles are jedec (.jed) files that contain the configuration data. They can be located at

`<Install_Directory>\CY3679 EVALUATION KIT\<version>\Firmware\Sample Profile`

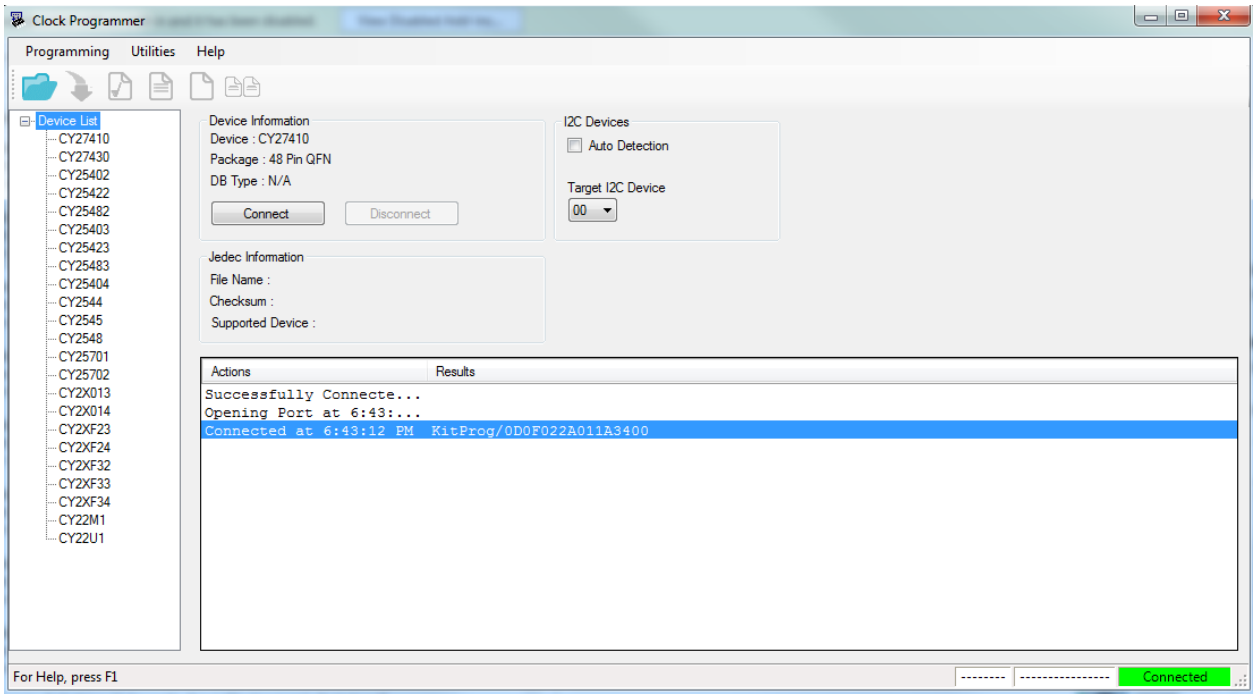
The sample profiles can also be downloaded from www.cypress.com/go/CY3679. These profiles can be used to evaluate different I/O standards supported by the CY27410 device. See Sample Profiles.

3.4.1 Programming the Sample Profile

The Clock Programmer tool comes along with the PSoC Programmer software. Clock Programmer can be located in installation folder at `<Install_Directory>\Programmer\ClockProgrammer.exe`.

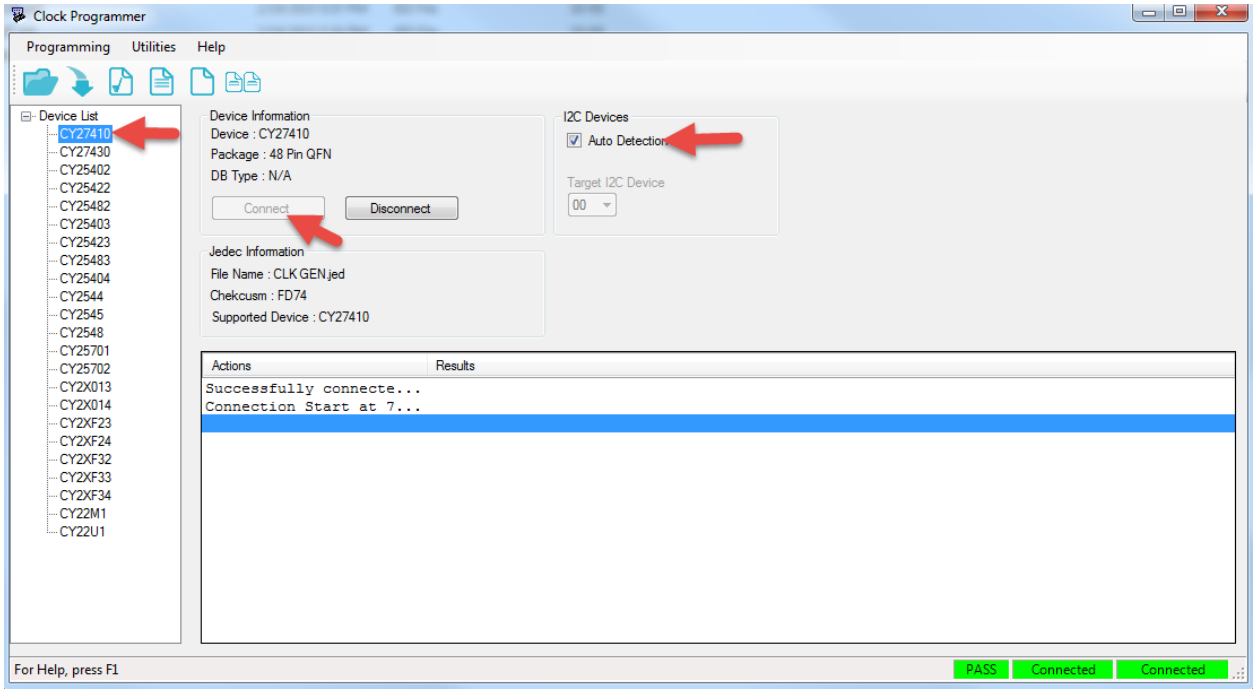
1. Connect CY3679 Evaluation Kit to your laptop through USB cable.
2. Double-click and open Clock Programmer.

Figure 3-6. Clock Programmer – Step 1



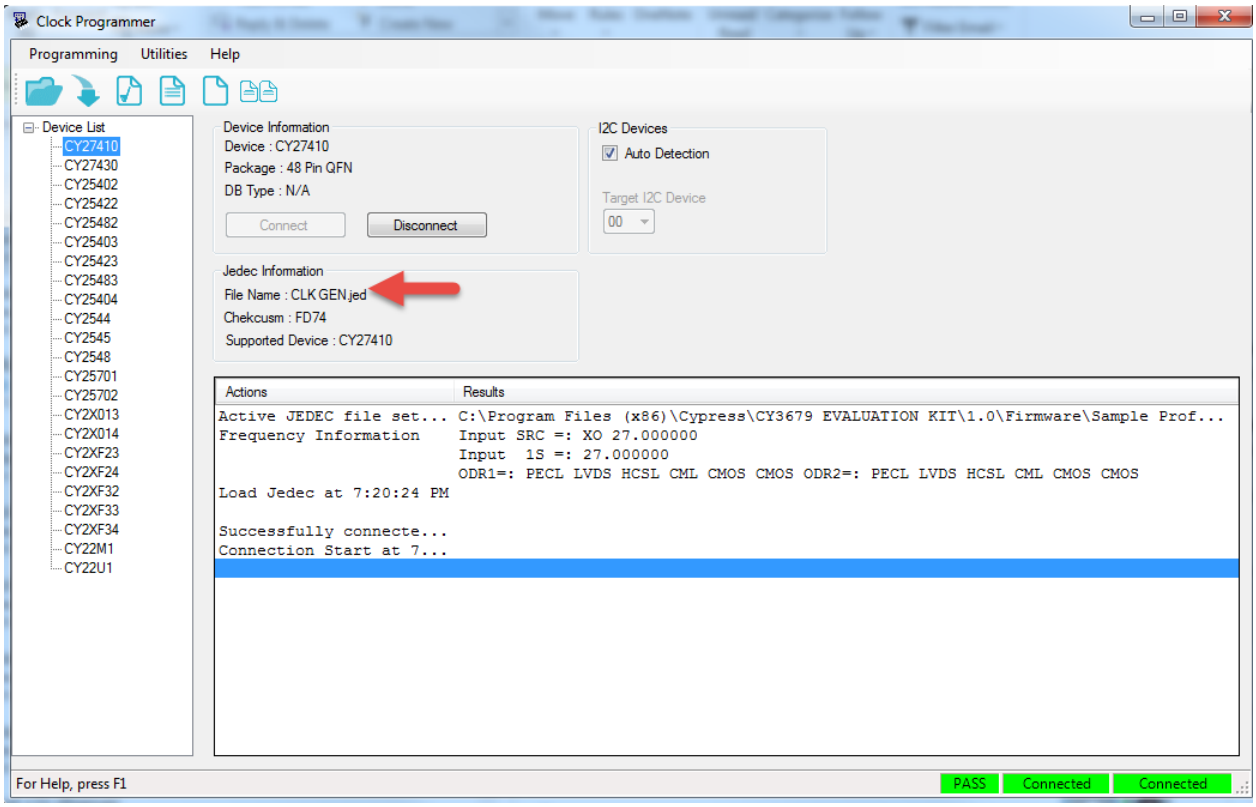
3. On the Device List window, do the following:
   - Expand the device list on the left and select **CY27410**.
   - Check the **Auto Detection** box and then click **Connect**. The command window shows the successful connection status.

Figure 3-7. Clock Programmer – Step 2



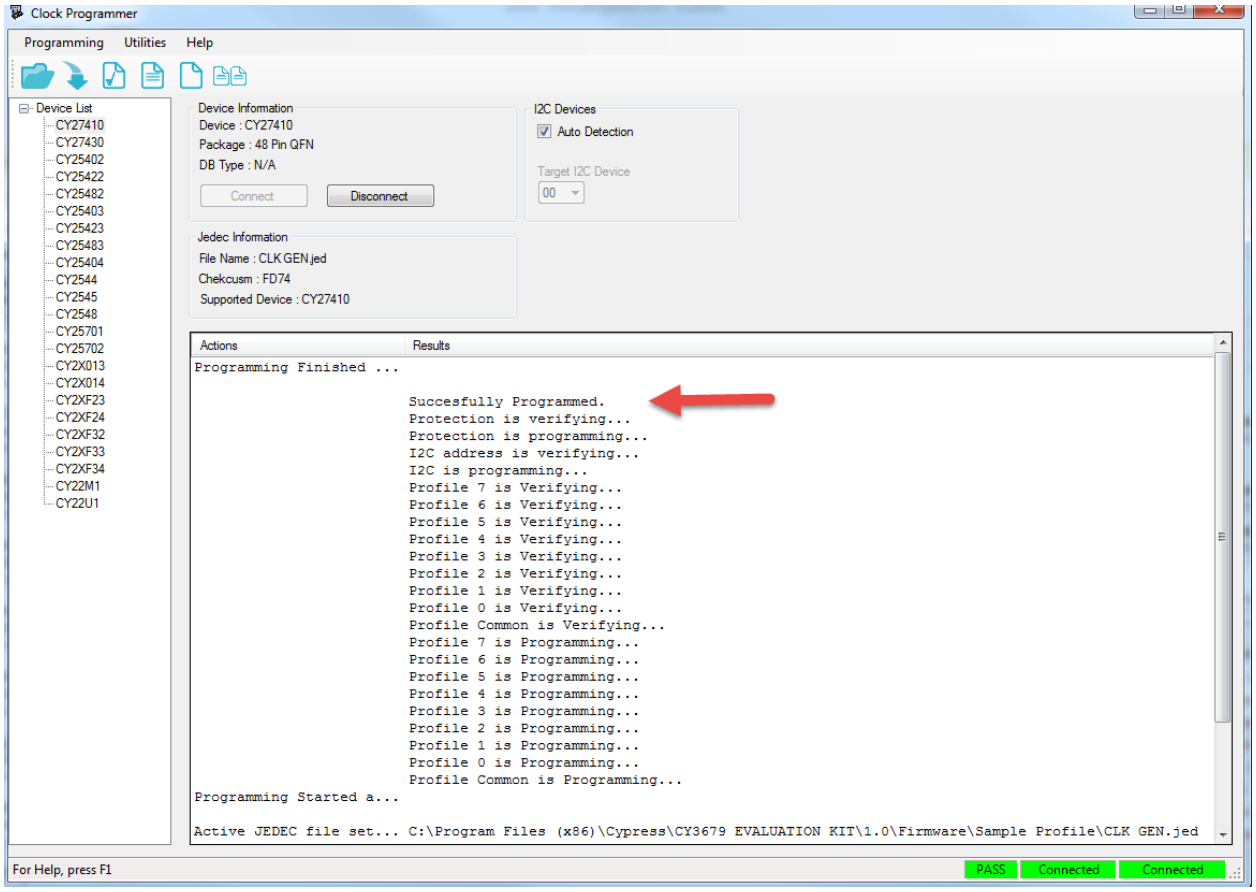
4. Go to **Programming** > **File Load** and select the configuration file *CLK GEN.jed* from the installation folder.

Figure 3-8. Clock Programmer – Step 3



5. Click on the Program button ( ).

Figure 3-9. Clock Programmer – Step 4



6. The device will be programmed. LED1 blinks to indicate that the device is being programmed.

   The sample profiles provided with this kit are configured to work with the default termination settings on different outputs. You can configure any output type, for example LVPECL, HCSL, or LVDS, on any output. See Section A.1. DC/AC Measurements of Clock Outputs for required termination settings for different I/O types.

3.5 Custom Profile Generation Support

If you require a custom profile, contact Cypress Customer Support at www.cypress.com/support. Cypress will provide you with the required profile as a jedec (.jed) file. Once you have obtained this profile file, follow the steps listed in the Programming the Sample Profile section to program the clock device (CY27410) with the custom profile.

4 Hardware

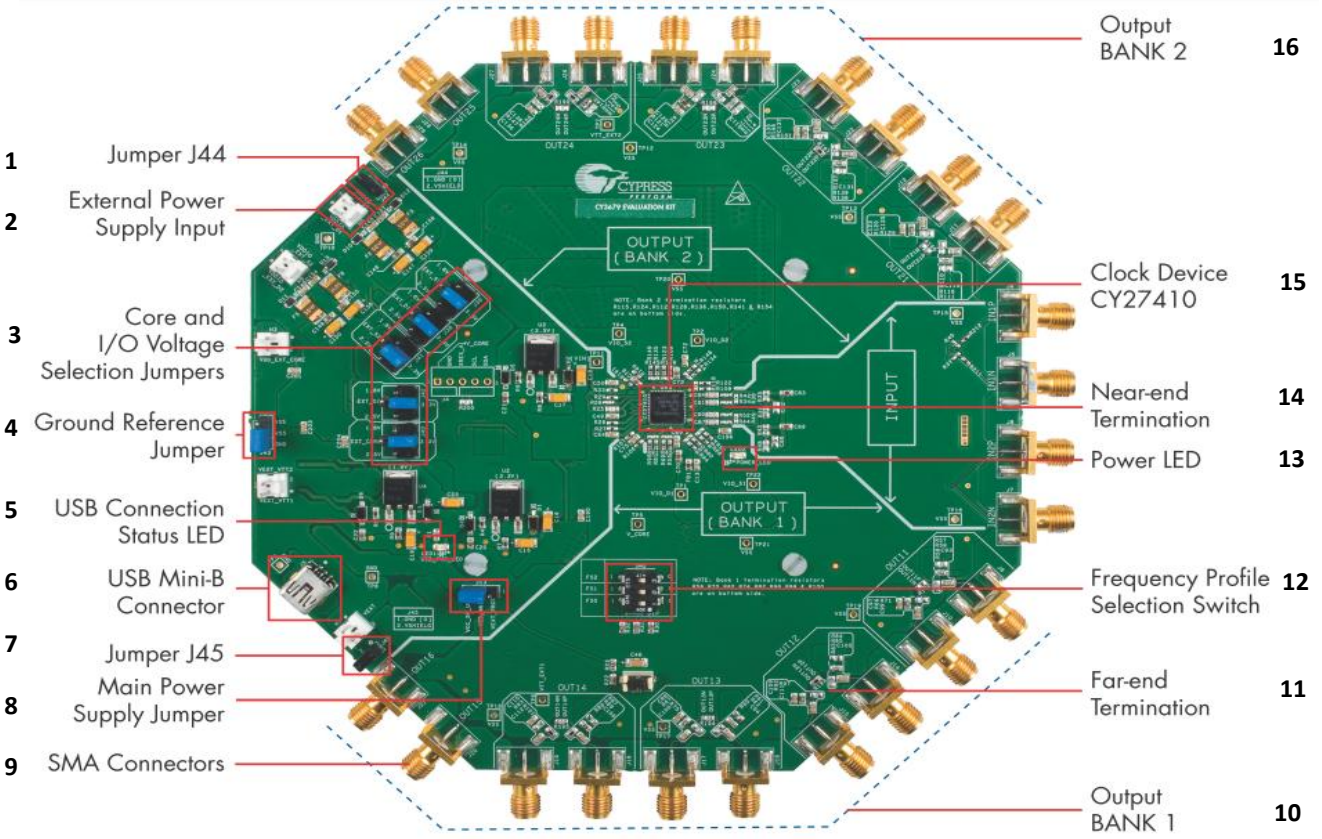
4.1 Board Overview

The CY3679 EVK is used for evaluating the CY27410 device. The following is a list of key features of the CY3679 Kit:

- Powered from either an USB port or external supply
- On-board 27-MHz crystal allows standalone operation
- Wide voltage range operation – both core (VDD) and I/O supplies (VDDIO_D1, VDDIO_D2, VDDIO_S1, and VDDIO_S2) can be independently set at 1.8 V, 2.5 V, 3.3 V, or external.
- Adjustable VDD and VSS provide flexibility to users for DC and AC measurements of signals using SMA connectors
- Jumper to short or isolate GND and VSS

Figure 4-1 shows the CY3679 board with a markup of the onboard components.

Figure 4-1. CY3679 Board with Onboard Components Labeled



1: Jumper J44

Jumper J44 is used to short GND (earth ground) and VSHIELD (SMA Ground). Refer to section 4.2.4 for more details on grounding scheme.

2: External Power Supply Input

The mark-up shows one of the five headers on the board (H1, H3, H5, H6, and H7) to which an external power supply can be connected.

3: Core and I/O Voltage Selection Jumpers

Use these to select the appropriate supply voltage from the on-board generated 3.3 V, 2.5 V, or 1.8 V, or direct external supply for Core and I/O supply voltages.

Figure 4-2. Power Select Jumpers Showing Default Selection of 3.3 V for Core and I/O Supply

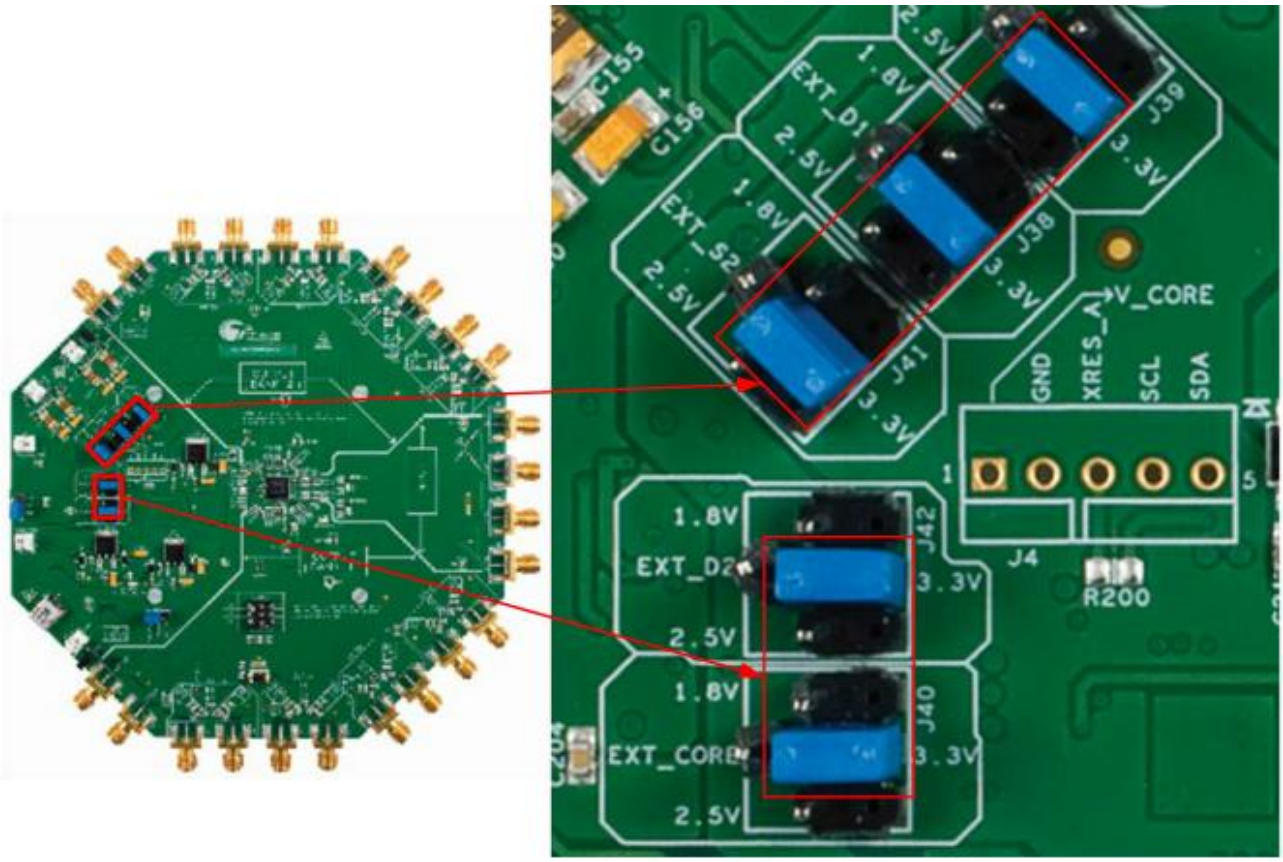
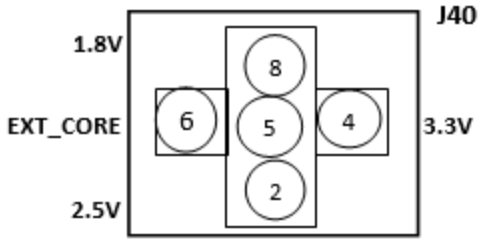


Figure 4-3 on next page shows the pin numbering of these Core and I/O voltage jumpers.

Figure 4-3. Pin Numbering of Core and I/O Voltage Jumpers



See Figure 4-4 through Figure 4-7 to check how the core power supply (VDD) is selected using jumper J40. See Power Section for more details.

Figure 4-4. J40 Setting to Select 1.8 V (Short Pins 5 and 8)

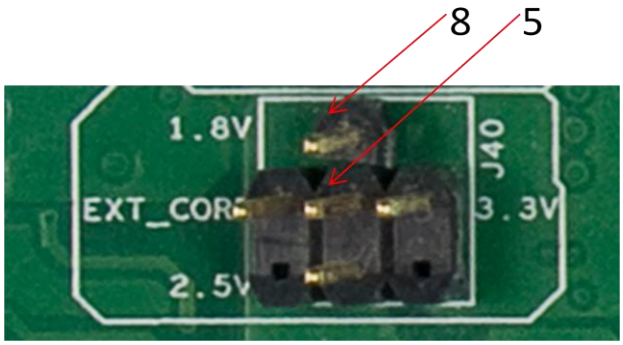


Figure 4-5. J40 Setting to Select 2.5 V (Short Pins 2 and 5)

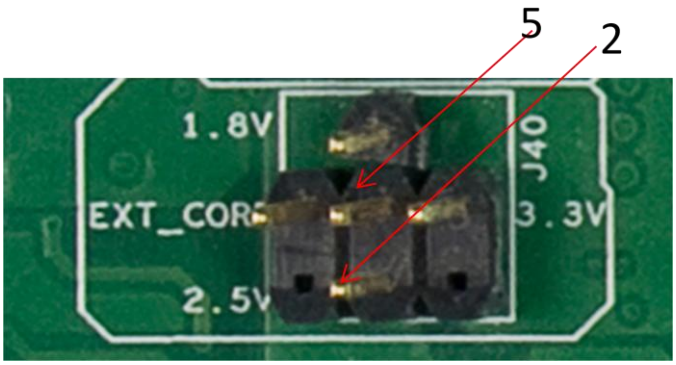


Figure 4-6. J40 Setting to Select 3.3 V (Short Pins 4 and 5)

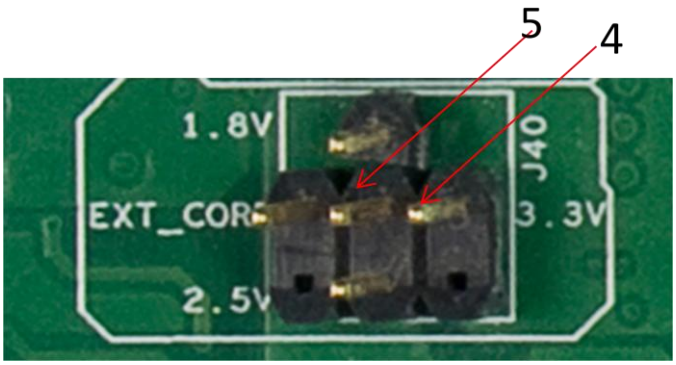
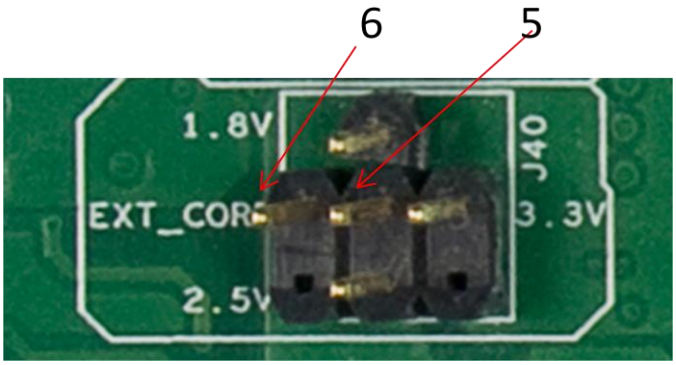


Figure 4-7. J40 Setting to Select External Supply (Short Pins 5 and 6)



Similarly, you can select the power for the I/O supplies VDDIO_D1 (on J38), VDDIO_S1 (on J39), VDDIO_D2 (on J42), and VDDIO_S2 (on J41).

4: Ground Reference Jumper

Proper jumper setting for J43 is important as it provides a ground reference to the device and the rest of the board (see Figure 4-8). See Grounding Scheme for more details.

Figure 4-8. Jumper Setting for Ground Reference

5: USB Connection Status LED

LED1 turns ON when the kit is connected to a PC through USB and blinks continuously when the device is being programmed.

6: USB Mini-B Connector

Connect the kit to a PC using the USB Standard-A to mini-B cable.

7: Jumper J45

Jumper J45 is used to short GND (earth ground) and VSHIELD (SMA Ground). Refer to section 4.2.4 for more details on grounding scheme.

8: Main Power Supply Jumper

Short pins **2** and **3** of jumper J13 to use the USB supply input to the kit. This is the default option. Otherwise, short pin **1** and **2** of J13 for external supply input to the kit through VEXT (header H7).

9: SMA Connectors

Connect SMA cables to the SMA connectors on one end and to an oscilloscope on the other end.

10: Output Bank 1

Bank 1 consists of four differential and two single-ended outputs. OUT11P-OUT11N, OUT12P-OUT12N, OUT13P-OUT13N and OUT14P-OUT14N are differential output pairs. Differential outputs can be configured as single ended outputs also. OUT15 and OUT16 are dedicated single-ended outputs.

11: Far-End Termination Options

Soldering or desoldering of resistors of an appropriate value may be required for proper terminations. See Appendix A.1 for details.

12: Frequency Profile Selection Switch

Up to eight profiles are stored by programming the flash inside the clock device CY27410. Use the Profile Selection switch to select the active profile. The profile selection can be done while the kit is in operation.

13: Power LED

This LED (LED2) stays ON when the CY27410 device is powered (that is, when the CY27410 core supply is connected by proper selection on jumper J40).

14: Near-End Termination Options

Soldering or desoldering of resistors of an appropriate value may be required for proper terminations. See Evaluating Different I/O Standards Using CY3679 for details.

15: Cypress's Clock Device CY27410

CY27410 is the Cypress clock chip that is evaluated with the CY3679 kit.

16: Output Bank 2

Bank 2 consists of four differential and two single-ended outputs. OUT21P-OUT21N, OUT22P-OUT22N, OUT23P-OUT23N, and OUT24P-OUT24N are differential output pairs. Differential outputs can be configured as single-ended outputs also. OUT25 and OUT26 are dedicated single-ended outputs.

4.2 Board Details

4.2.1 Default Jumper Settings

The CY3679 EVK comes with default jumper settings that select all I/O and core supply voltages as 3.3 V. Table 4-1 lists the default jumper settings.

Table 4-1. Default Jumper Settings on the Kit

Jumper	Default Settings	Selection
J13	Pin 2 and 3 are shorted	USB supply selected
J38	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_D1
J39	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_S1
J40	Pin 4 and 5 are shorted	3.3 V selected for VDD (core)
J41	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_S2
J42	Pin 4 and 5 are shorted	3.3 V selected for VDDIO_D2
J43	Pin 1 and 2 are shorted	GND and VSS are shorted
J44	Pin 1 and 2 are shorted	GND and VSHIELD* are shorted
J45	Pin 1 and 2 are shorted	GND and VSHIELD* are shorted

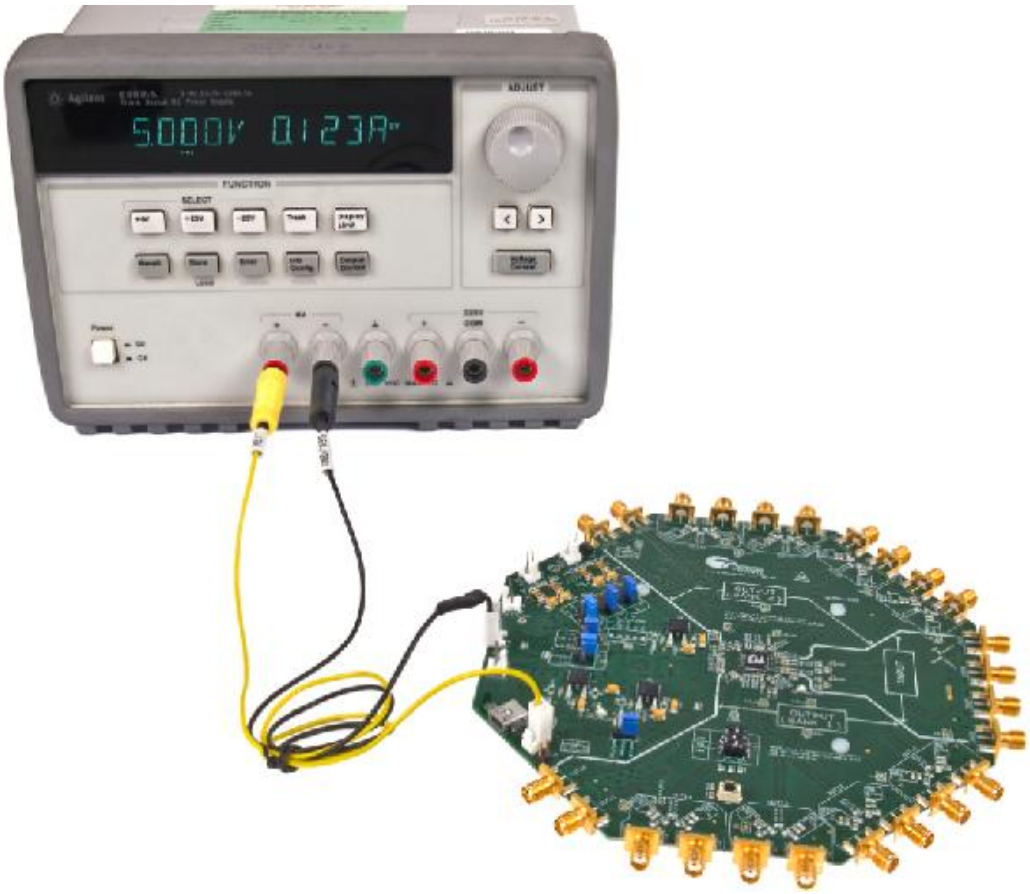
* Refer to section 4.2.4 for more details on grounding scheme

4.2.2 Power Section

You can choose either USB power supply or single external supply (VEXT) to power the kit by setting jumper J13. For using the USB supply option, short pins 2 and 3 of jumper J13.

If the external supply option is used, short pins 1 and 2 of jumper J13. Connect the external 5-V supply to header H7 (VEXT) and ground to VSS pin of J43. Use yellow and black colored wires to connect external supply as shown in Figure 4-9.

Figure 4-9. External 5-V Supply Connection



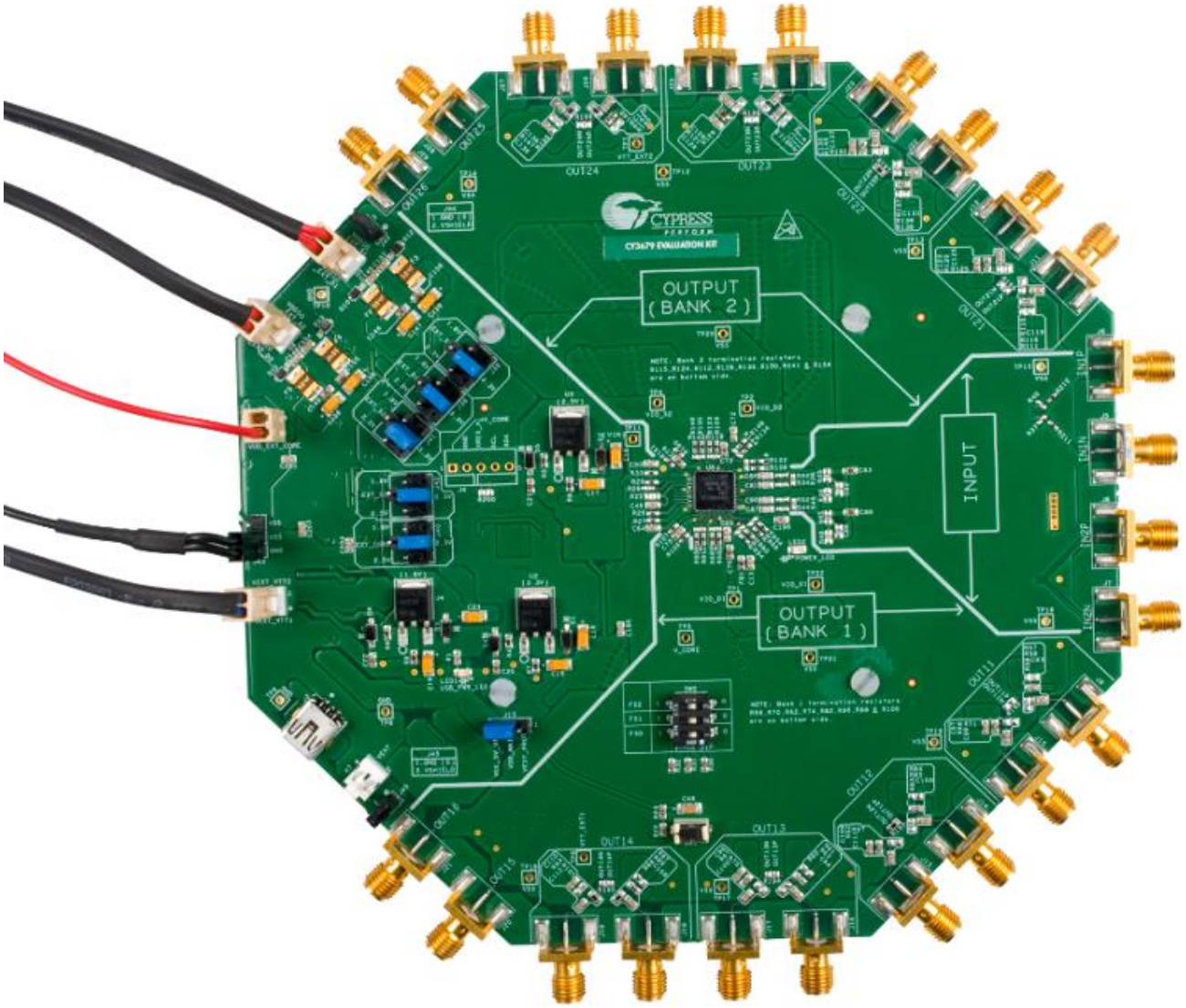
The device requires core and I/O supply voltages. The device has two banks of outputs, with each bank requiring a separate power supply for single-ended and differential outputs. The correct voltage must be selected for core and I/O supply for proper operation. Both core and I/O supplies can be independently selected from on-board generated supplies 1.8 V, 2.5 V, or 3.3 V or direct external supply on respective headers. Table 4-2 lists the hardware settings required for power selection. Figure 4-10 shows the different external supplies connected.

Table 4-2. Power Selection Guide

CY27410 Device Supply	Functionality	Jumper	Jumper Setting				Voltage Selected
			Short Pins 5 and 2	Short Pins 5 and 4	Short Pins 5 and 8	Short Pins 5 and 6	
VDD	Core supply	J40	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H3.1)
VDDIO_D1	Supply for differential outputs in Bank 1	J38	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H5.1)
VDDIO_S1	Supply for single ended outputs in Bank 1	J39	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H5.2)

CY27410 Device Supply	Functionality	Jumper	Jumper Setting				Voltage Selected
			Short Pins 5 and 2	Short Pins 5 and 4	Short Pins 5 and 8	Short Pins 5 and 6	
VDDIO_D2	Supply for differential outputs in Bank 2	J42	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H6.1)
VDDIO_S2	Supply for single ended outputs in Bank 2	J41	Yes	No	No	No	2.5 V
			No	Yes	No	No	3.3 V
			No	No	Yes	No	1.8 V
			No	No	No	Yes	EXT (H6.2)

Figure 4-10. External Supply Connected to VDDIOs, Core, and Termination Voltages



4.2.3 Caution for 1.8-V Operation

If the profile (.jed) file is generated to configure the device for 1.8-V operation, before loading the profile into the clock device, ensure that the core and I/O jumpers are set properly to select 1.8 V as the supply voltage. See Table 4-2 for correct 1.8-V jumper settings.

4.2.4 Grounding Scheme

The board contains three ground references: earth ground (GND), CY27410 device ground (VSS), and SMA ground (VSHIELD). These three ground references have been isolated in this kit to provide the advanced feature of enabling DC measurement of the different output standards supported by the device using SMA connectors.

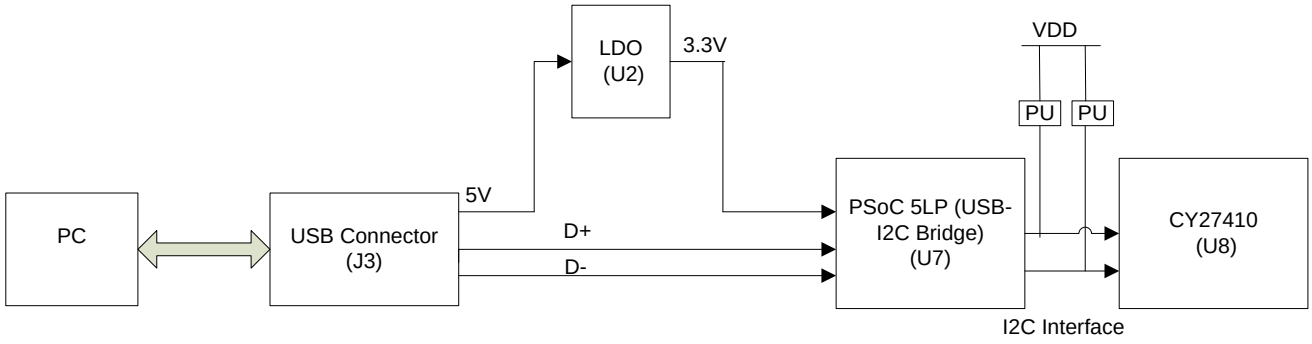
The device ground (VSS) is measured with respect to the earth ground (GND). You can use jumper J43 to short or isolate these two grounds on the board. When the board is powered using USB, GND is provided from the USB ground connection. Ensure that the jumper is placed to short Pin 1 and 2 so that GND and VSS are shorted on the board.

The ground reference of all SMA connectors are shorted on the board, designated as VSHIELD. When the board is connected to any instrument (such as an oscilloscope or a Modulation Domain Analyzer) through an SMA cable, the ground reference of the instrument is shorted to VSHIELD. This is enabled by default, wherein VSHIELD and GND are shorted (pins 1 and 2 of jumpers J44 and J45 are shorted). However, for advanced measurement of clock parameters, the jumper settings of J43, J44, and J45 should be set as listed in Table A-1, Table A-2, and Table A-3.

4.2.5 Programming Section

The board should be connected to a PC through a USB connector to configure and program the device. See CY3679 Kit USB Connection to learn how to connect the kit to a PC. Figure 4-11 illustrates the programming section of the kit.

Figure 4-11. Programming the CY27410 Device



The USB interface can generate a 5-V power supply. The on-board LDO generates a 3.3-V supply to power the on-board PSoC 5LP device. The PSoC 5LP converts the JEDEC profiles into an I^2C-compatible format, which is then loaded into the CY27410 clock device. Up to eight profiles can be programmed and saved in the CY27410 device memory at one time. The active profile selection can be made when the kit is in operation using the switch SW2.

During programming, you must keep the core power supply of CY27410 device at 1.8 V. See Table 4-3 for details. Other I/O supplies can be left floating or powered to a maximum of 1.8 V.

Table 4-3. Hardware Setting for Programming

Board Component	Hardware Setting
J3 (USB Connector)	Connect J3 to the PC that has the required software installed
J13	Short Pin 2 and 3 to use USB power
J43	Short GND and VSS
J40	Short Pin 5 with pin 8 to power the device core with on-board 1.8 V power supply option

The sample profiles are jedec (.jed) files that contain the configuration data. See Sample Profiles.

Table 4-4. Sample Profiles

Profile	Profile Name	Configuration	Hardware Settings
1	CLK GEN.jed	All output types with different frequencies	Default. See Sample Profile #1 for more details.
2	PCIE.jed	HCSL – 2 outputs; OUT13 and OUT23	See Sample Profile #2 for more details.
3	NZDB.jed	All output types with different frequencies. External input required for reference clock.	See Sample Profile #3 for more details.
4	ZDB.jed	All differential outputs of Bank2 show a 50-MHz output	See Sample Profile #4 for more details.

4.2.6 LED Indicators

Table 4-5. LED Indicators

LED	Label	Indicator	Description
LED1	USB_PWR_LED	Power and Signal indicator	This LED turns ON when the kit is connected to the USB port on a PC using the cable provided. If this LED does not turn ON, check if J13 is properly selected (pin 2 and 3 are shorted). This LED blinks continuously when the device is being programmed through the PSoC 5LP device. **Note**: This LED may glow with low intensity under the following condition: The PSoC 5LP device is powered through VEXT, while the USB cable is disconnected, and the CY27410 core is not powered. This low-intensity LED glow may be misleading to the user on the status of the USB connection to the board. It is, therefore, recommended to avoid this condition during usage of the kit.
LED2	POWER_LED	Power	This LED turns ON when the core of the CY27410 device is powered. Ensure that J40 is connected to the 3.3 V, 2.5 V, or 1.8 V board supply, or to an external power supply. The intensity of LED glow for 1.8 V is lower compared to 2.5 V and 3.3 V.

4.2.7 On-Board Crystal

The on-board 27-MHz crystal serves as a clock source for the CY27410 device.

4.2.8 Footprint for On-Board Oscillator

You can also mount a 5 mm × 7 mm oscillator as a clock source for the CY27410 clock device. The oscillator is not mounted by default. The reference designator of oscillator is X1 and can be found on the bottom side of the board.

4.3 Absolute Maximum Ratings

The CY3679 EVK provides flexibility to the user to directly connect an external voltage supply to the CY27410 core, I/O power pins and termination voltages. The maximum allowable external supply voltage to the VEXT line is 8 V. When the core, I/O and termination voltages are individually connected to the external supply, the maximum allowed voltage on these power pins is 5 V. Therefore, care should be taken while connecting the external supply.

The I^2C header J4 is DNP in this kit. It is not recommended to use these pins. Inputs to the pins in this header must not exceed 4.6 V.

Table 4-6. Power Cable Selection for External Supply Option

Header	External Supply	Cable Color	Label	Operating Power supply	Absolute Maximum Rating
H7.1	5 V, single external supply to power the kit	Yellow	VEXT	5 V	8 V
H5.1	Bank1, differential output	Red	VDDIO_EXT_D1	3.3 V, 2.5 V, or 1.8 V	5 V
H5.2	Bank1, Single ended output	Red	VDDIO_EXT_S1	3.3 V, 2.5 V, or 1.8 V	5 V
H6.1	Bank2, differential output	Red	VDDIO_EXT_D2	3.3 V, 2.5 V, or 1.8 V	5 V

Header	External Supply	Cable Color	Label	Operating Power supply	Absolute Maximum Rating
H6.2	Bank2, single ended output	Red	VDDIO_EXT_S2	3.3 V, 2.5 V, or 1.8 V	5 V
H3.2	CORE	Red	VDD_EXT_CORE	3.3 V, 2.5 V, or 1.8 V	5 V
H1.1	Bank1, termination voltage	Blue	VEXT_VTT1	3.3 V, 2.5 V, or 1.8 V	5 V
H1.2	Bank2, termination voltage	Blue	VEXT_VTT2	3.3 V, 2.5 V, or 1.8 V	5 V
J43	Ground	Black	GND/VSS	0 V	-3.3 V

Note: The maximum ratings for the supplies listed in Table 4-6 are to maintain a maximum allowable potential difference between the respective supplies and ground (GND/VSS). Also, it is strongly recommended not to use any of the test points on the board to power the device.

4.4 Evaluating Different I/O Standards Using CY3679 EVK

The CY27410 device supports LVPECL, LVDS, HCSL, and CML differential output types and LVCMOS single-ended output type. A sample output termination circuit for bank 1 LVPECL output type is shown in Figure 4-12 and a sample picture is shown in Figure 4-13.

Figure 4-12. LVPECL Output Termination Circuit

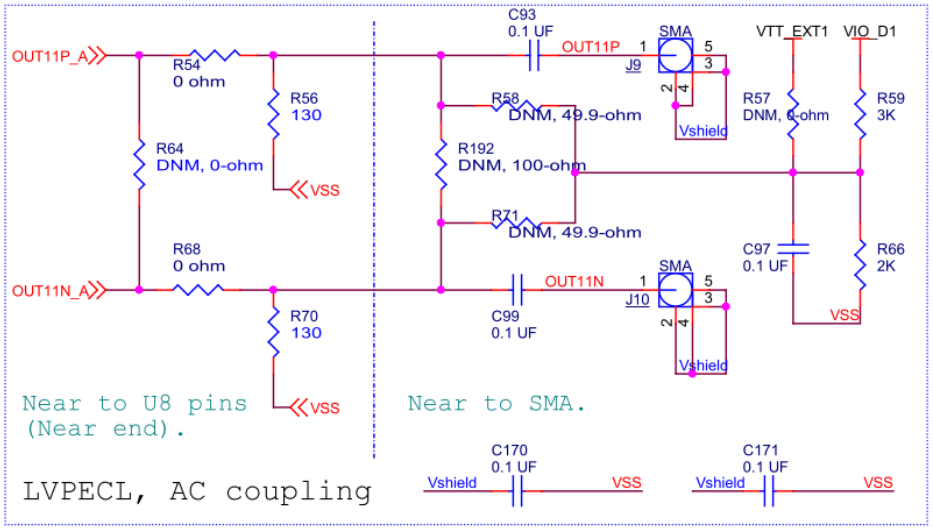
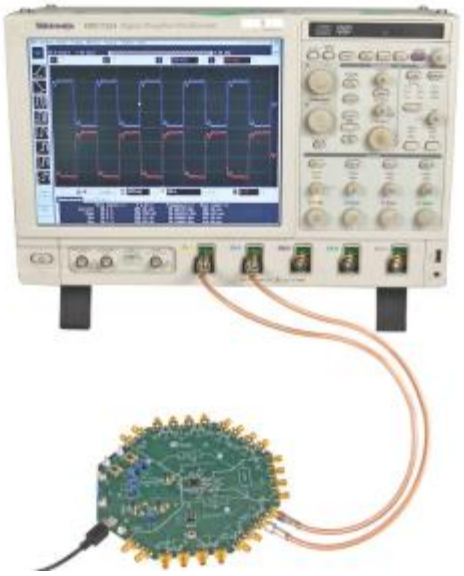


Figure 4-13. EVK Connected to an Oscilloscope



The default output connections to the SMA connectors for the different output types is as shown in Table 4-7.

Table 4-7. Default Output Options on the CY3679 EVK

Bank	Output Number	SMA Number	Default Output Type
BANK 1	OUT11P	J9	LVPECL
	OUT11N	J10	
	OUT12P	J14	LVDS
	OUT12N	J15	
	OUT13P	J16	HCSL
	OUT13N	J17	
	OUT14P	J18	CML
	OUT14N	J19	
	OUT15	J20	LVCMOS
	OUT16	J21	LVCMOS
BANK 2	OUT21P	J11	LVPECL
	OUT21N	J12	
	OUT22P	J22	LVDS
	OUT22N	J23	
	OUT23P	J24	HCSL
	OUT23N	J25	
	OUT24P	J26	CML
	OUT24N	J27	
	OUT25	J28	LVCMOS
	OUT26	J29	LVCMOS

To evaluate the CY27410 device for DC/AC measurements using the CY3679 EVK, see the A.1. DC/AC Measurements of Clock Outputs section.

5 Sample Profiles

This kit can be evaluated with sample profiles that configure the device with different output types and frequencies. This section provides the details of each profile. The sample profiles can be used with default terminations. All the profiles are located at:

`<Install_Directory>\CY3679 EVALUATION KIT\<version>\Firmware\Sample Profile`

One out of the four sample profiles (CLK GEN.jed) is preloaded on the CY27410 device and can be evaluated with the SW2 frequency select (FS) switch on the kit. For all the sample profiles, the I/O output types are matched to the different outputs as in Table 4-7.

5.1 Sample Profile #1 – *CLK GEN.jed*

This sample profile is designed for 3.3V crystal reference input and is pre-loaded on the CY27410 device.

Table 5-1. Sample Profile #1 – *CLK GEN.jed*

Output	I/O Type	Profile Selection(SW2) FS[2:0]							
		000	001	010	011	100	101	110	111
OUT11	LVPECL[1]	50 MHz	100 MHz	25 MHz	33.33 MHz	X	X	X	X
OUT12	LVDS[2]	50 MHz	100 MHz	25 MHz	66.66 MHz	X	X	X	X
OUT13	HCSL[1]	100 MHz	50 MHz	25 MHz	133.33 MHz	X	X	X	X
OUT14	CML[2]	100 MHz	50 MHz	25 MHz	133.33 MHz	X	X	X	X
OUT15	LVCMOS[1]	32.768 kHz	25 MHz	24 MHz	24 MHz	X	X	X	X
OUT16	LVCMOS[1]	33.33 MHz	33.33 MHz	48 MHz	48 MHz	X	X	X	X
OUT21	LVPECL[1]	156.25 MHz	155.52 MHz	77.76 MHz	38.88 MHz	X	X	X	X
OUT22	LVDS[2]	156.25 MHz	155.52 MHz	77.76 MHz	38.88 MHz	X	X	X	X
OUT23	HCSL[1]	156.25 MHz	77.76 MHz	77.76 MHz	24 MHz	X	X	X	X
OUT24	CML[2]	156.25 MHz	77.76 MHz	77.76 MHz	24 MHz	X	X	X	X
OUT25	LVCMOS[1]	133.33 MHz	25 MHz	10 MHz	48 MHz	X	X	X	X
OUT26	LVCMOS[1]	33.33 MHz	10 MHz	25 MHz	48 MHz	X	X	X	X

[1] For LVPECL, HCSL and LVCMOS outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be shorted.

[2] While evaluating LVDS and CML outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be open.

The 'x' indicates the FS profile is not programmed, and therefore, invalid.

Note: When switching from an invalid profile (in the above example, 100, 101, 110, or 111) to a valid profile (in the above example, 000, 001, 010 or 011), you must press the RESET button (SW1) after changing the SW2 switch settings.

5.2 Sample Profile #2 – *PCIE.jed*

The sample profile 2 – *PCIE.jed* is specifically designed for the PCIe standard that works at 100-MHz frequency. The on-board crystal (27 MHz) is used for the input reference frequency. This profile also exhibits the Spread Spectrum (SS) feature. Outputs OUT13 and OUT23 are, by default, set for HCSL standard, so they should be used to observe the PCIe-100-MHz clock outputs. You can check the outputs with the profile selection FS [2:0] = 000 and 001. The profile (FS [2:0] = 001) with 0.5% down spectrum is configured with a center frequency of 99.75 MHz.

Table 5-2. Sample Profile #2 – *PCIE.jed*

Output	I/O type	Profile Selection(SW2) FS[2:0]							
		000	001	010	011	100	101	110	111
OUT11	LVPECL[1]	X	X	X	X	X	X	X	X
OUT12	LVDS[2]	X	X	X	X	X	X	X	X
OUT13	HCSL[1]	100 MHz (0% spread)	100 MHz (0.5% down spread)	X	X	X	X	X	X
OUT14	CML[2]	X	X	X	X	X	X	X	X
OUT15	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT16	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT21	LVPECL[1]	X	X	X	X	X	X	X	X
OUT22	LVDS[2]	X	X	X	X	X	X	X	X
OUT23	HCSL[1]	100 MHz (0% spread)	100 MHz (0.5% down spread))	X	X	X	X	X	X
OUT24	CML[2]	X	X	X	X	X	X	X	X
OUT25	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT26	LVCMOS[1]	X	X	X	X	X	X	X	X

[1] For LVPECL, HCSL and LVCMOS outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be shorted.

[2] While evaluating LVDS and CML outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be open.

The 'x' indicates the FS profile is not programmed, and hence invalid.

Note: When switching from an invalid profile to a valid profile, you must press the RESET button (SW1) after changing the SW2 switch settings.

5.3 Sample Profile #3 – *NZDB.jed*

The sample profile 3 – *NZDB.jed* is designed for illustrating the Non-Zero Delay Buffer (NZDB) mode feature. This profile is configured such that it requires a 50-MHz reference input connected externally on IN1P (800-mV peak-to-peak). Bank 1 differential outputs are configured to provide a 50-MHz output, while the LVCMOS outputs are programmed to 25 MHz. Bank 2 differential outputs are configured to provide a 50-MHz output, while the LVCMOS outputs are programmed to 12.5 MHz. Check the outputs with the profile selection FS [2:0] = 000.

Table 5-3. Sample Profile #3 – *NZDB.jed*

Profile Selection(SW2) FS[2:0]		000	001	010	011	100	101	110	111
OUT11	LVPECL[1]	50 MHz	X	X	X	X	X	X	X
OUT12	LVDS[2]	50 MHz	X	X	X	X	X	X	X
OUT13	HCSL[1]	50 MHz	X	X	X	X	X	X	X
OUT14	CML[2]	50 MHz	X	X	X	X	X	X	X
OUT15	LVCMOS[1]	25 MHz	X	X	X	X	X	X	X
OUT16	LVCMOS[1]	25 MHz	X	X	X	X	X	X	X
OUT21	LVPECL[1]	50 MHz	X	X	X	X	X	X	X

Profile Selection(SW2) FS[2:0]		000	001	010	011	100	101	110	111
OUT22	LVDS[2]	50 MHz	X	X	X	X	X	X	X
OUT23	HCSL[1]	50 MHz	X	X	X	X	X	X	X
OUT24	CML[2]	50 MHz	X	X	X	X	X	X	X
OUT25	LVCMOS[1]	12.5 MHz	X	X	X	X	X	X	X
OUT26	LVCMOS[1]	12.5 MHz	X	X	X	X	X	X	X

[1] For LVPECL, HCSL and LVCMOS outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be shorted.

[2] While evaluating LVDS and CML outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be open.

The 'x' indicates the FS profile is not programmed, and hence invalid.

5.4 Sample Profile #4 – *ZDB.jed*

The sample profile # 4 – *ZDB.jed* is designed for illustrating Zero Delay Buffer (ZDB) mode operation. This profile is configured such that it requires a 50-MHz reference input connected externally on IN1P (800-mV peak-to-peak) . OUT21 should be fed back to IN2. All differential outputs of Bank 2 show a 50-MHz output. You can check the outputs with profile selection FS [2:0] = 000.

Table 5-4. Sample Profile #4 – *ZDB.jed*

Profile Selection(SW2) FS[2:0]		000	001	010	011	100	101	110	111
OUT11	LVPECL[1]	X	X	X	X	X	X	X	X
OUT12	LVDS[2]	X	X	X	X	X	X	X	X
OUT13	HCSL[1]	X	X	X	X	X	X	X	X
OUT14	CML[2]	X	X	X	X	X	X	X	X
OUT15	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT16	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT21	LVPECL[1]	50 MHz	X	X	X	X	X	X	X
OUT22	LVDS[2]	50 MHz	X	X	X	X	X	X	X
OUT23	HCSL[1]	50 MHz	X	X	X	X	X	X	X
OUT24	CML[2]	50 MHz	X	X	X	X	X	X	X
OUT25	LVCMOS[1]	X	X	X	X	X	X	X	X
OUT26	LVCMOS[1]	X	X	X	X	X	X	X	X

[1] For LVPECL, HCSL and LVCMOS outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be shorted.

[2] While evaluating LVDS and CML outputs, (J44.1 & J44.2) and (J45.1 & J45.2) MUST be open.

The 'x' indicates this FS profile is not programmed, and hence invalid.

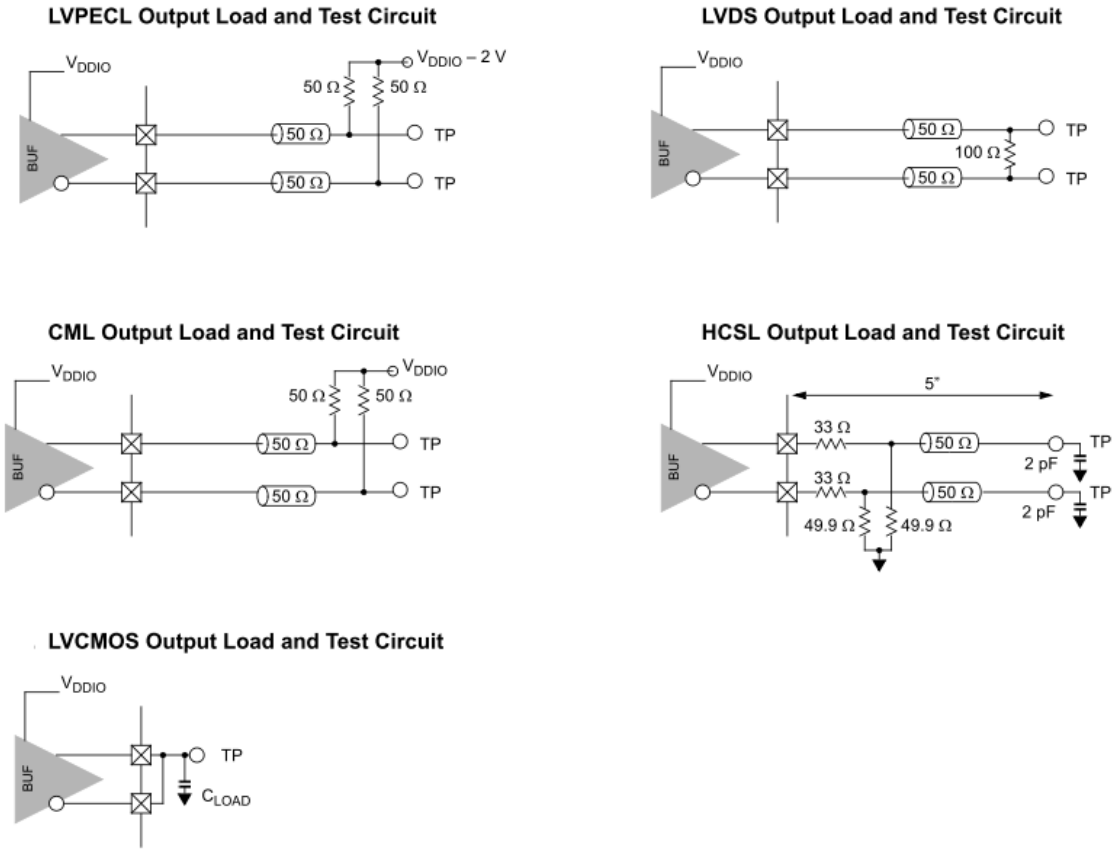
Note: When switching from an invalid profile to a valid profile, you must press the RESET button (SW1) after changing the SW2 switch settings.

A. Appendix

A.1. DC/AC Measurements of Clock Outputs

To evaluate the CY27410 device for DC/AC measurements, see Figure A-1 and Table A-1, Table A-2, and Table A-3 for custom output settings.

Figure A-1. Recommended Termination Scheme for DC/AC Measurements



The desired output measurement can be done using an SMA cable connected to an oscilloscope as shown in Figure 4-13. SMA offers an extra 50 ohms to the oscilloscope ground, which should be taken into account while doing measurements. Follow the termination scheme listed in Table A-1, Table A-2, and Table A-3 while using SMA probes.

Table A-1. Settings to Evaluate DC/AC Parameters for VDD=3.3 V Using SMA (50-ohm Scope Termination)

Signal Type	Near-End Termination			Far-End Terminations			VDD (V)	VSS (V)	J43 VSS-GND Connection	J44, J45 GND-VSHIELD Connection
	Differential Resistor (R64)	Series Resistor (R54, R68)	Pull-Down Resistor (R56, R70)	Series DC Block Capacitor (C93, C99)	Differential Resistor (R192)	Pull-Up Resistor (R58, R71)				
LVPECL	DNM	0 ohm	DNM	0 ohm	DNM	DNM	2.0	-1.3	Open	Open
HCSL	DNM	0 ohm	DNM	0 ohm	DNM	DNM	3.3	0	Short	Short
CML	DNM	0 ohm	DNM	0 ohm	DNM	DNM	0	-3.3	Open	Open
LVDS	DNM	0 ohm	DNM	0 ohm	DNM	DNM	3.3	0	Open	Open
LVCMOS *	0 ohm	0 ohm	Replace R56 with 15-pF cap. R70 - DNM	0 ohm	DNM	DNM	3.3	0	Short	Short

Table A-2. Settings to Evaluate DC/AC Parameters for VDD=2.5 V Using SMA (50-ohm Scope Termination)

Signal Type	Near-End Termination			Far-End Terminations			VDD (V)	VSS (V)	J43 VSS-GND Connection	J44, J45 GND-VSHIELD Connection
	Differential Resistor (R64)	Series Resistor (R54, R68)	Pull-Down Resistor (R56, R70)	Series DC Block Capacitor (C93, C99)*	Differential Resistor (R192)	Pull-Up Resistor (R58, R71)				
LVPECL	DNM	0 ohm	DNM	0 ohm	DNM	DNM	2.0	-0.5	Open	Open
HCSL	DNM	0 ohm	DNM	0 ohm	DNM	DNM	2.5	0	Short	Short
CML	DNM	0 ohm	DNM	0 ohm	DNM	DNM	0	-2.5	Open	Open
LVDS	DNM	0 ohm	DNM	0 ohm	DNM	DNM	2.5	0	Open	Open
LVCMOS*	0 ohm	0 ohm	Replace R56 with 15-pF cap. R70 - DNM	0 ohm	DNM	DNM	2.5	0	Short	Short

Table A-3. Settings to Evaluate DC/AC Parameters for VDD=1.8 V Using SMA (50-ohm Scope Termination)

Signal Type	Near-End Termination			Far-End Terminations			VDD (V)	VSS (V)	J43 VSS-GND Connection	J44, J45 GND-VSHIELD Connection
	Differential Resistor (R64)	Series Resistor (R54, R68)	Pull-Down Resistor (R56, R70)	Series DC Block Capacitor (C93, C99)*	Differential Resistor (R192)	Pull-Up Resistor (R58, R71)				
HCSL	DNM	0 ohm	DNM	0 ohm	DNM	DNM	1.8	0	Short	Short
CML	DNM	0 ohm	DNM	0 ohm	DNM	DNM	0	-1.8	Open	Open
LVDS	DNM	0 ohm	DNM	0 ohm	DNM	DNM	1.8	0	Open	Open
LVCMOS*	0 ohm	0 ohm	Replace R56 with 15-pF cap. R70 - DNM	0 ohm	DNM	DNM	1.8	0	Short	Short

*For precise LVCMOS measurements, it is recommended to populate 450 ohm at C93 and C99. The VOH and VOL levels observed on the oscilloscope must be multiplied by a factor of 10 to arrive at the actual VOH and VOL levels.

A.2. Schematics

Figure A-2. Sheet 1 – Block Diagram

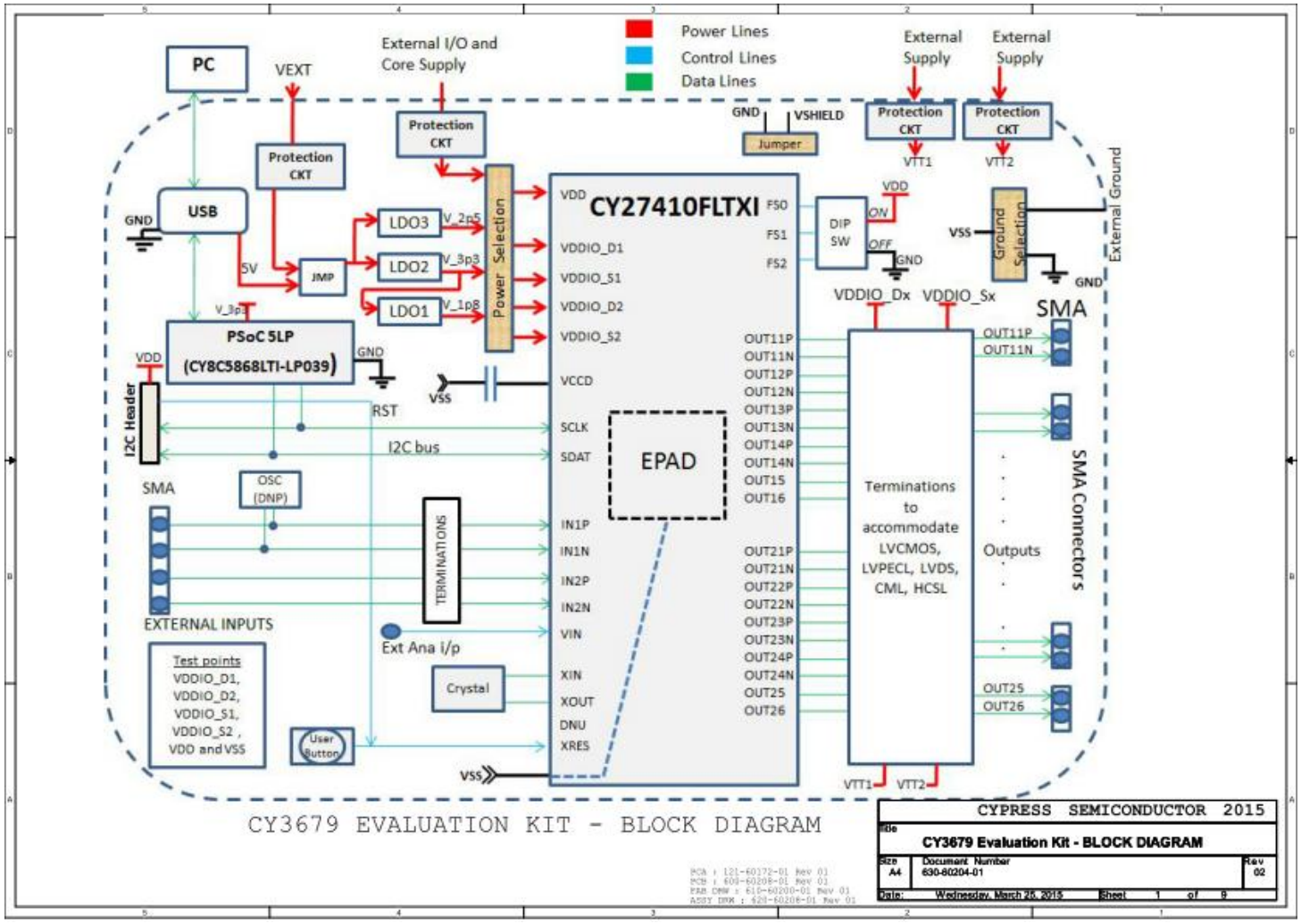


Figure A-3 Sheet 2 – Power Supply Scheme – I

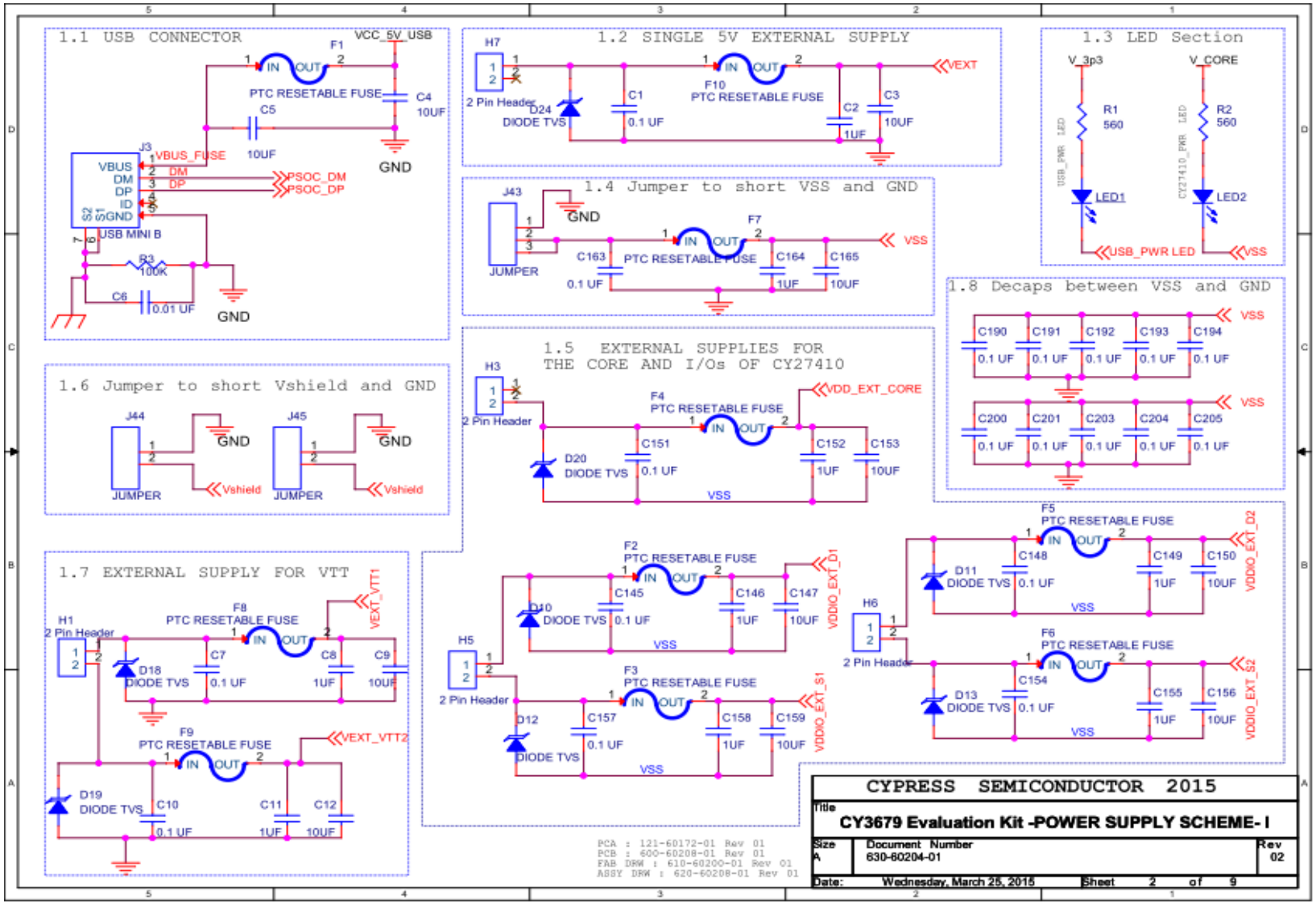


Figure A-4 Sheet 2 – Power Supply Scheme – II

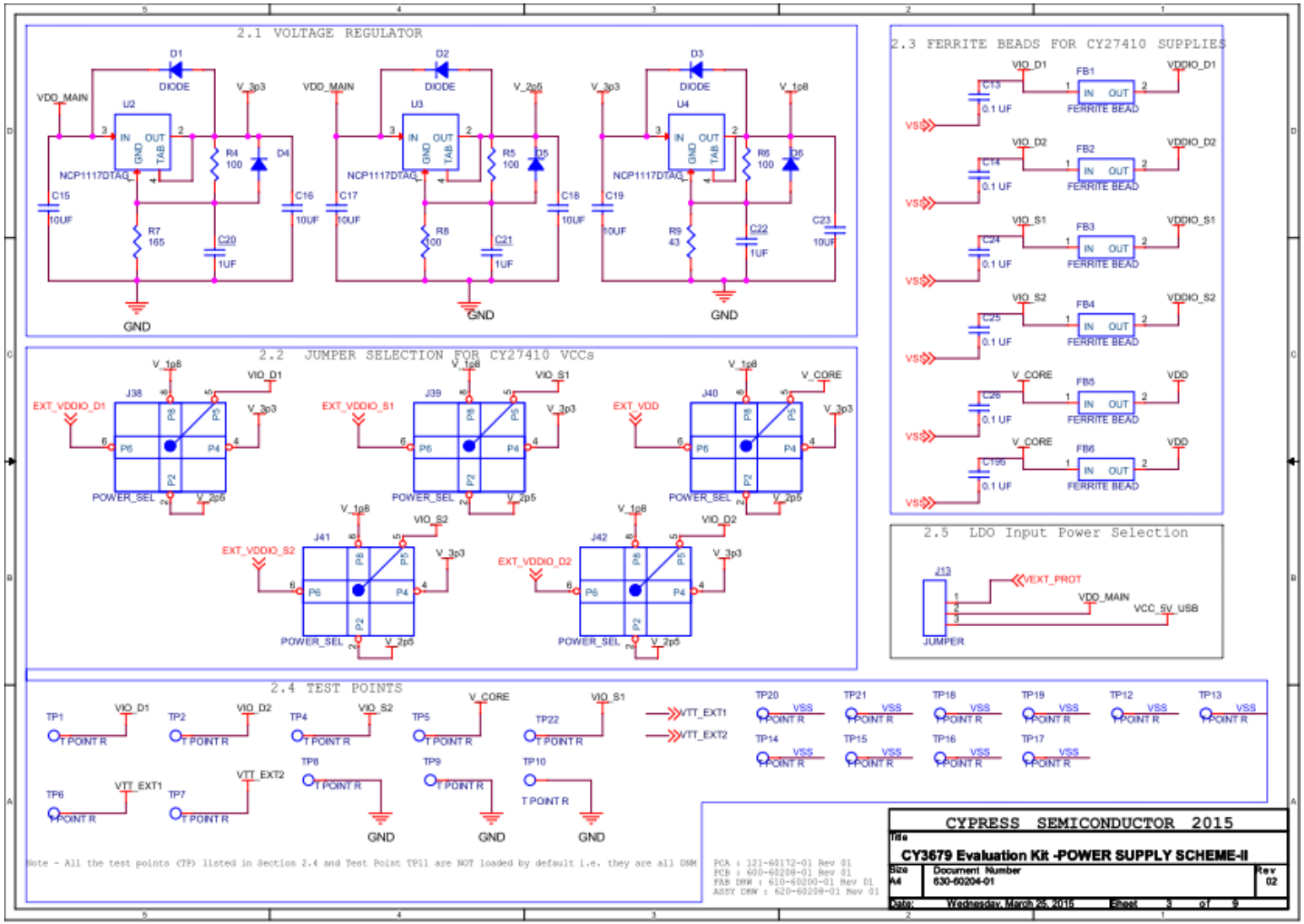


Figure A-5. Protection Circuit

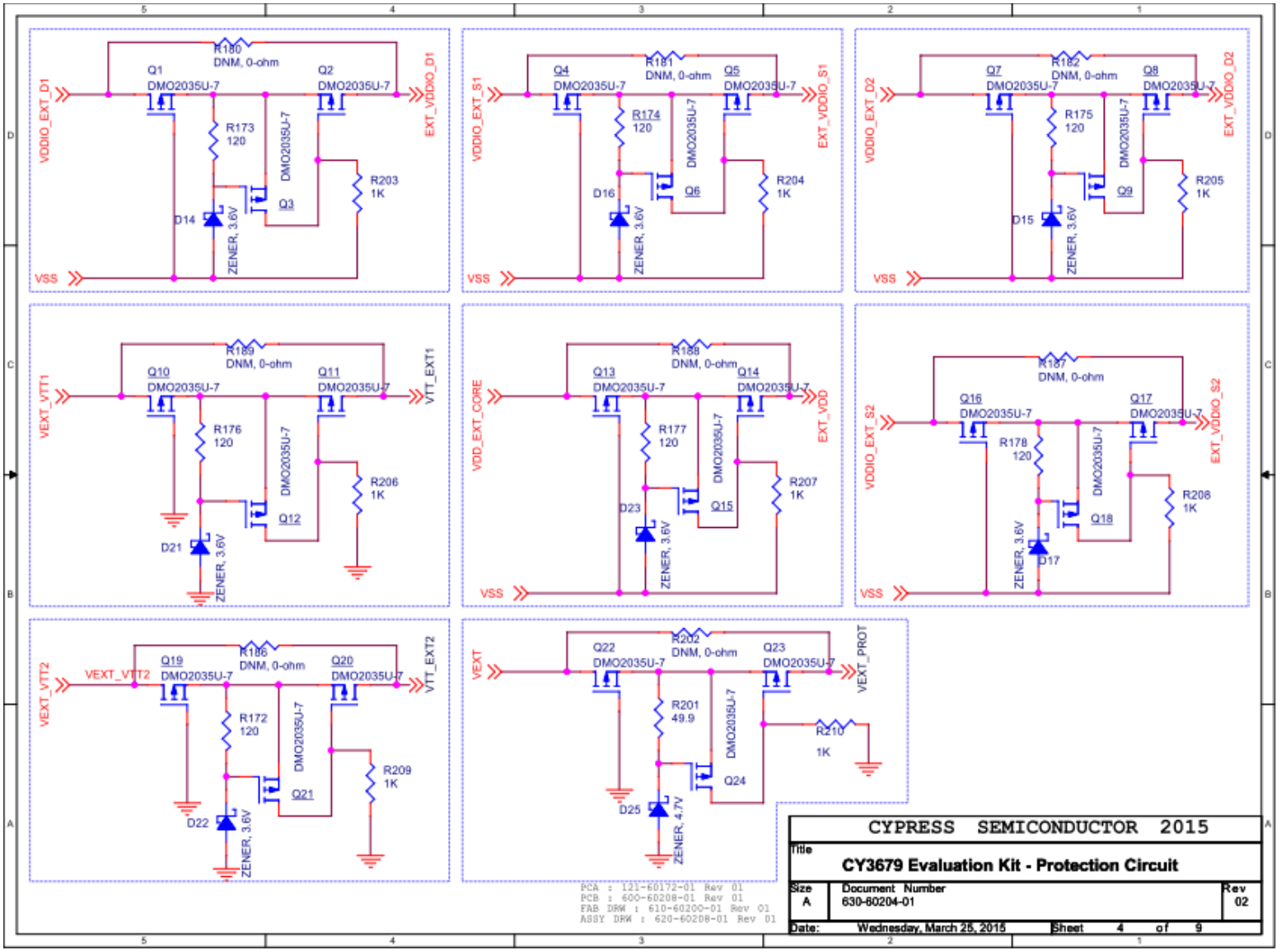


Figure A-6. Controller Schematics

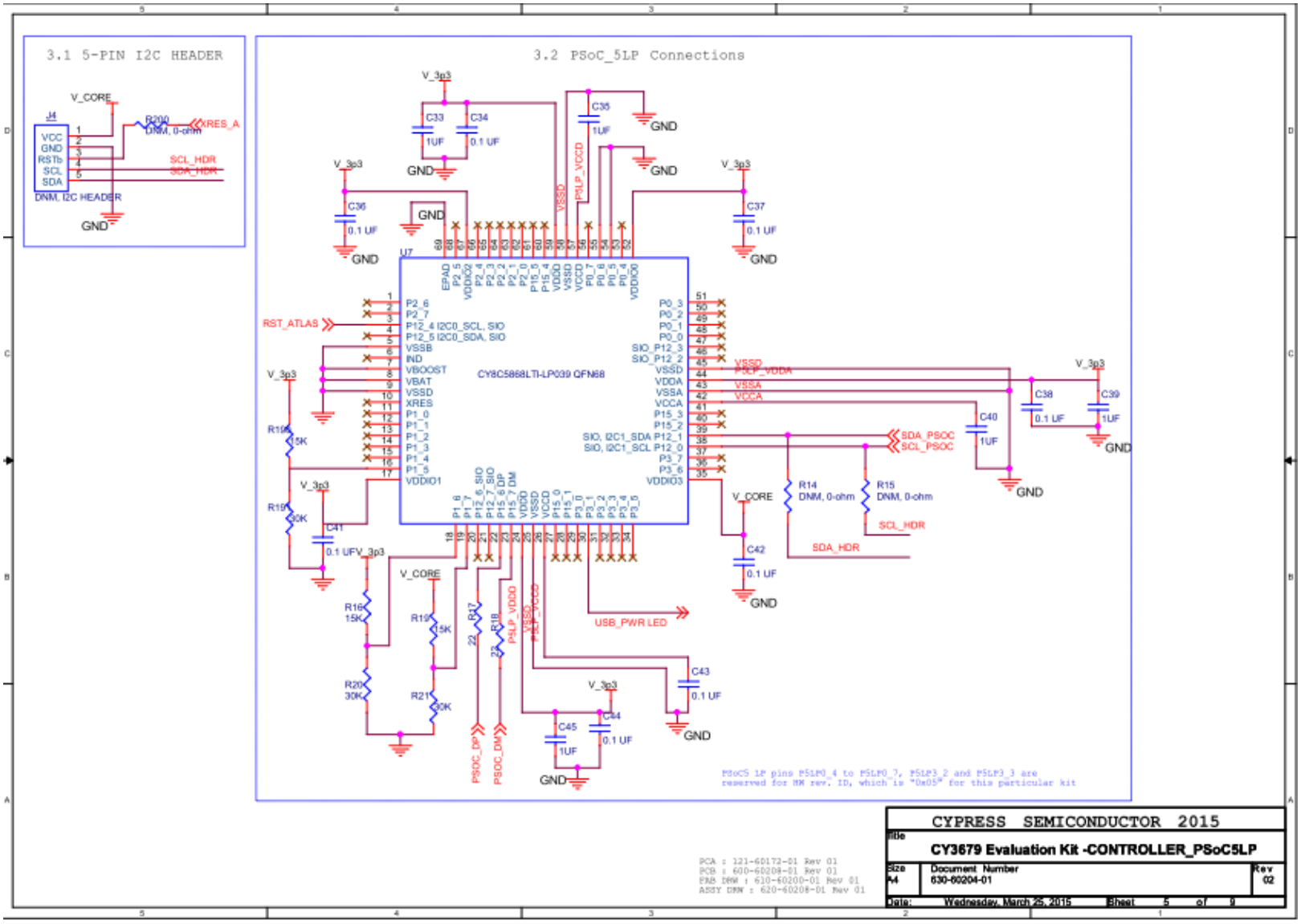


Figure A-7. Schematics – CY27410

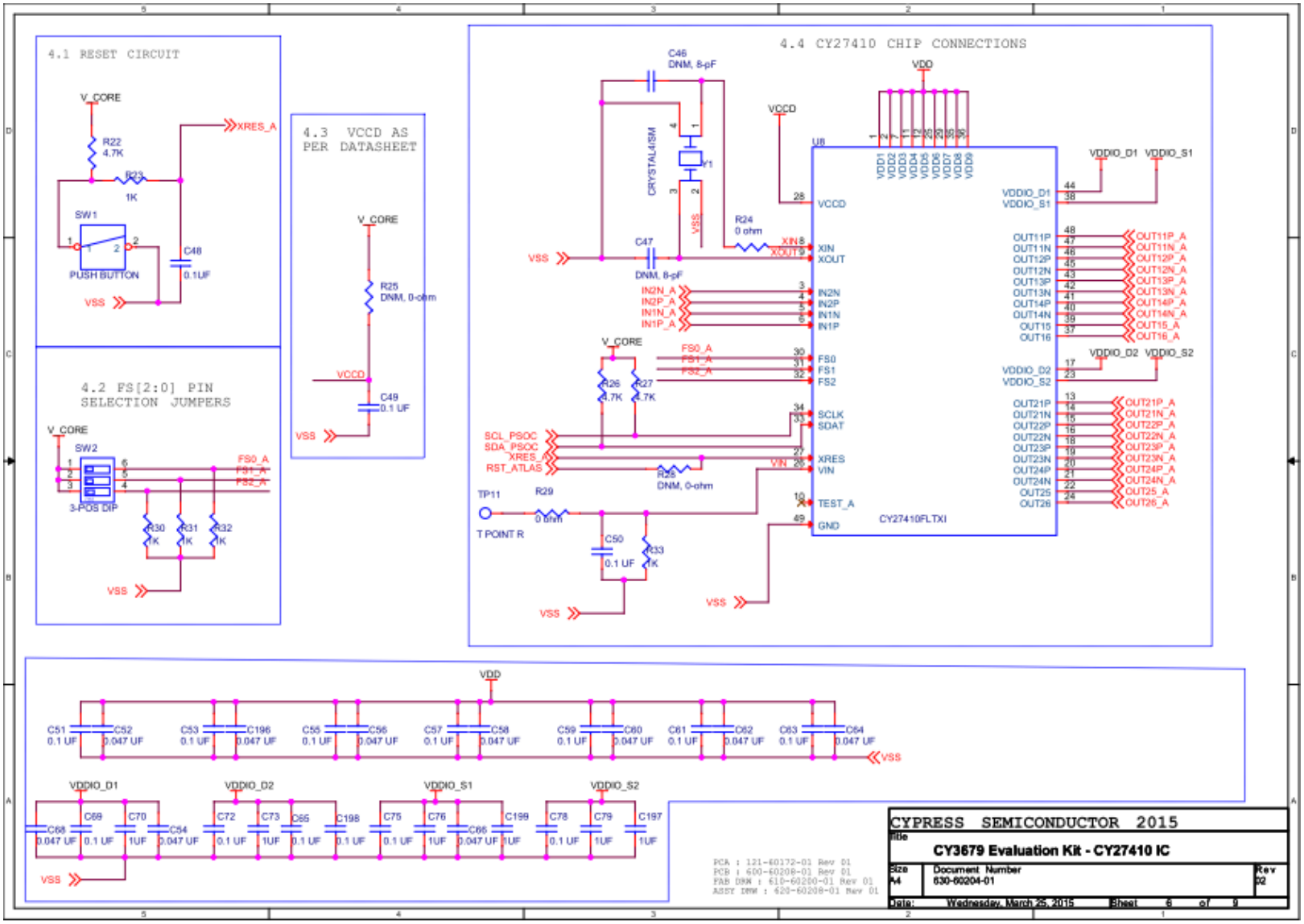


Figure A-8. Input Termination

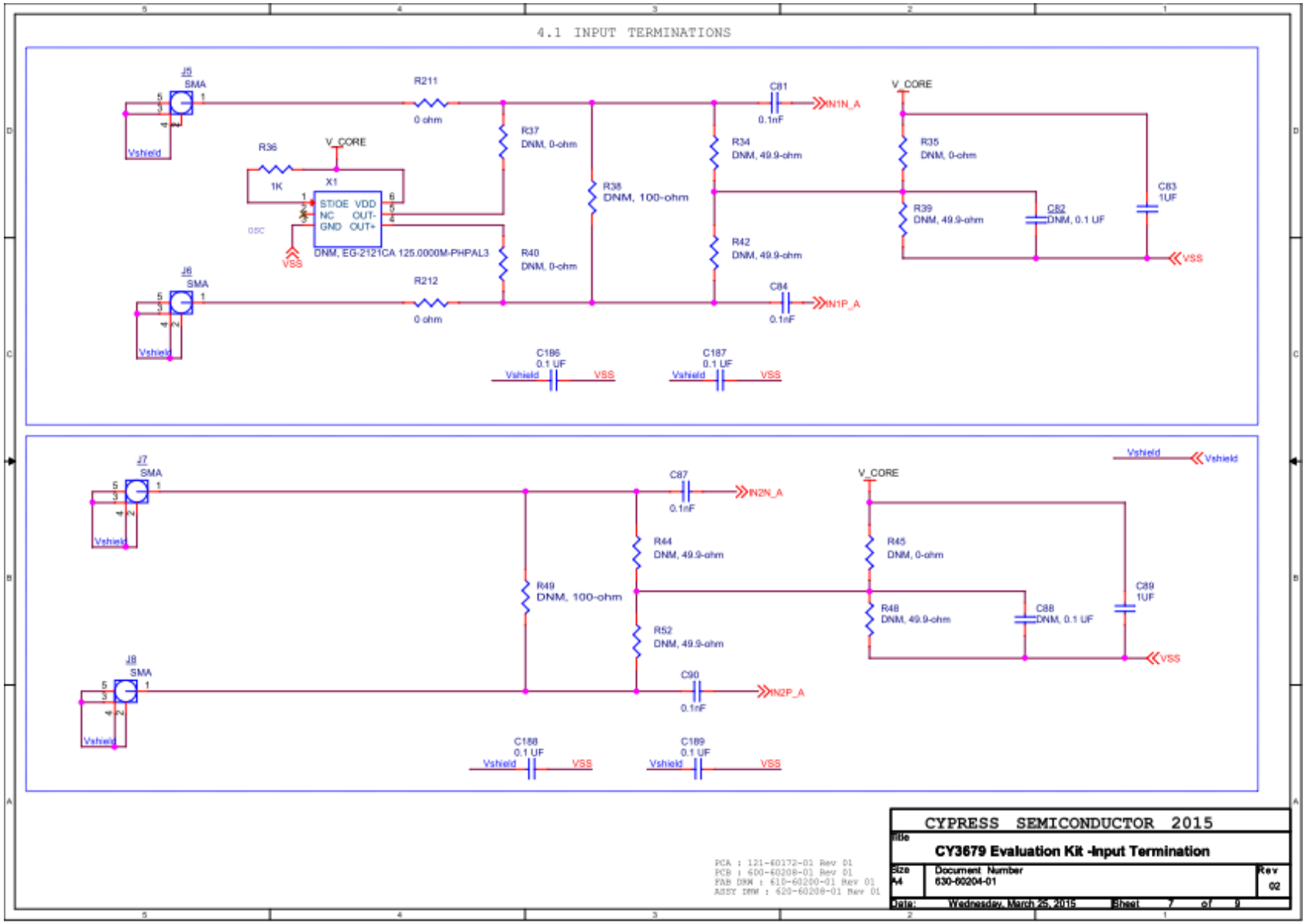


Figure A-9. Output Terminations: BANK 1

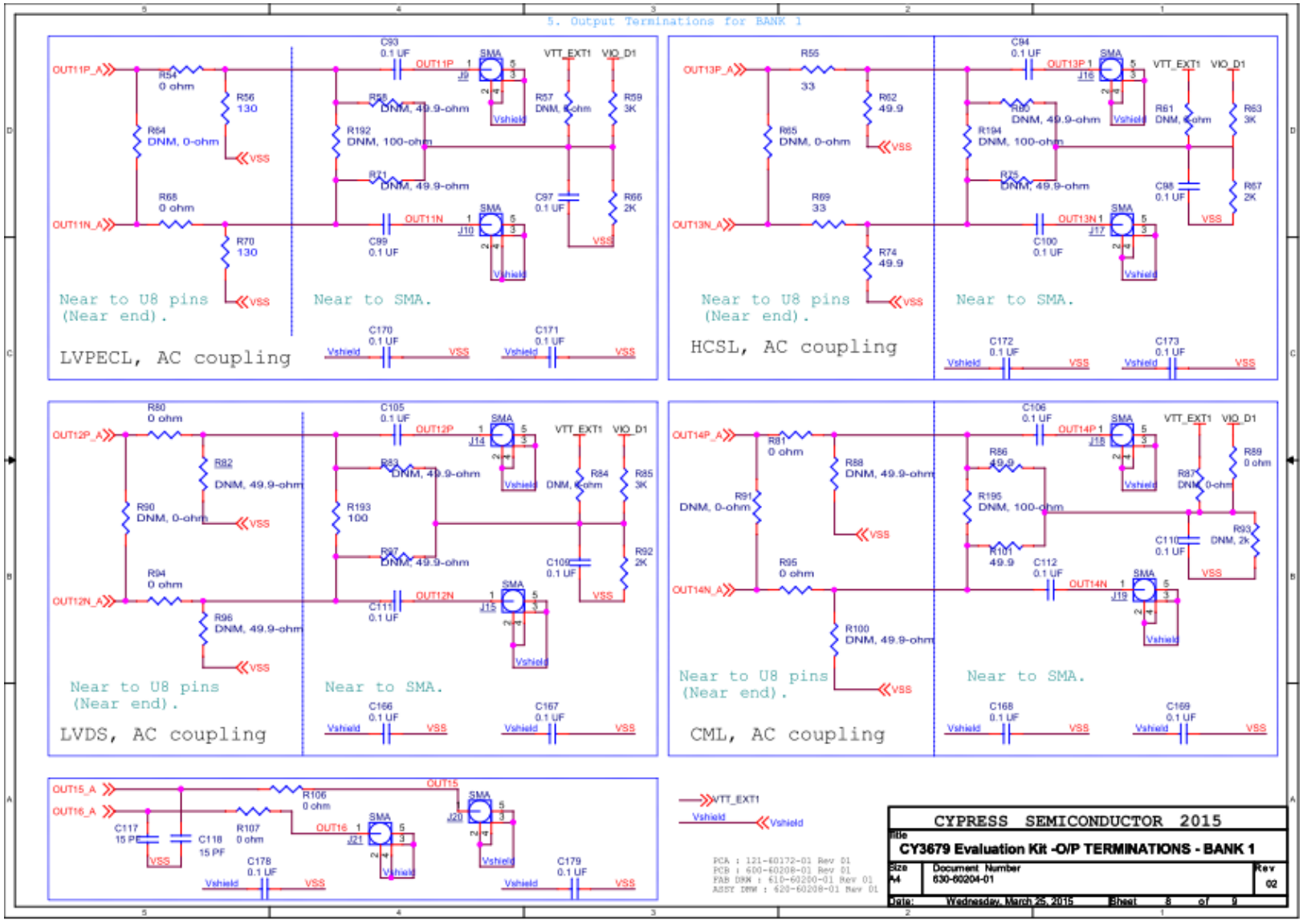
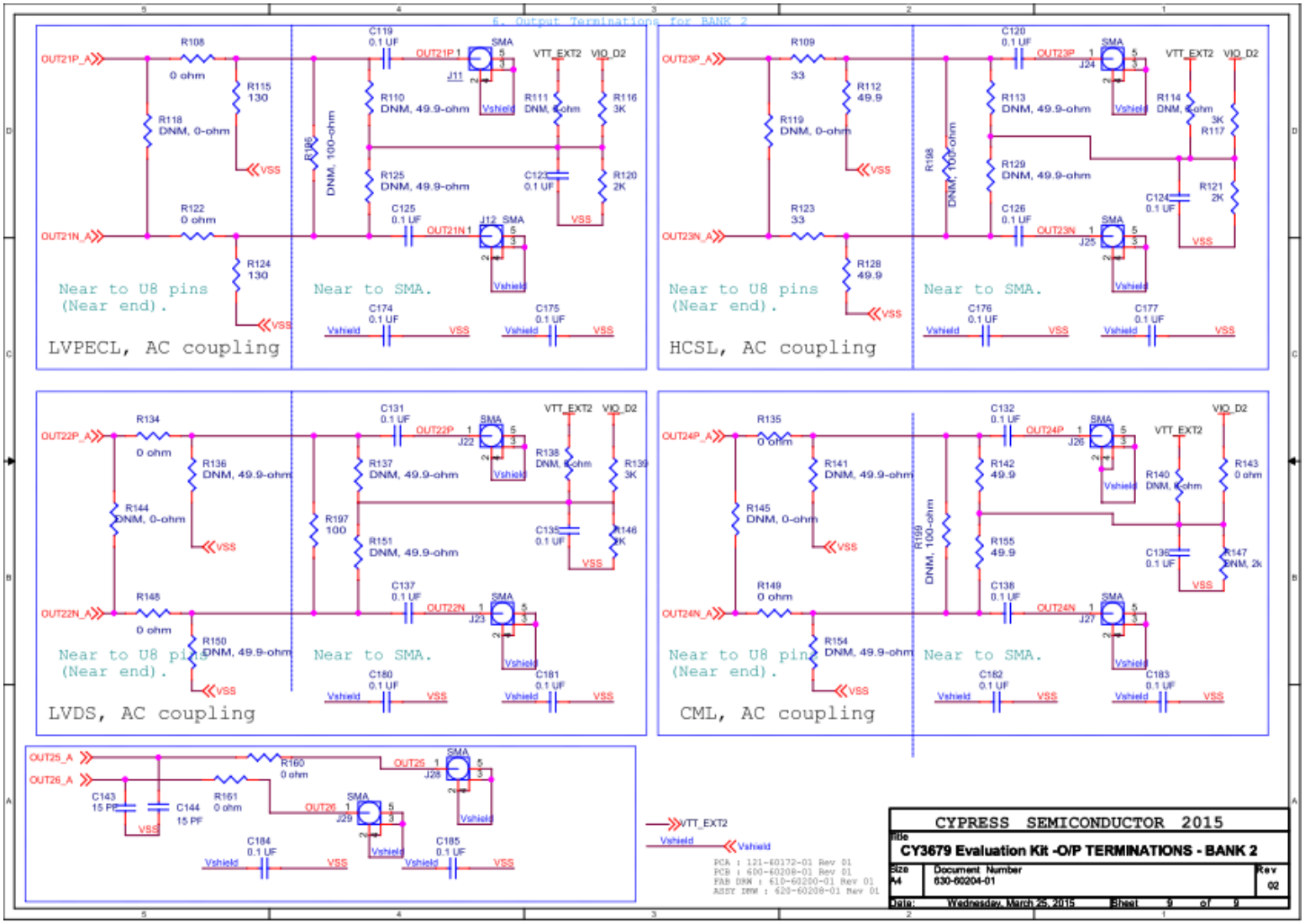
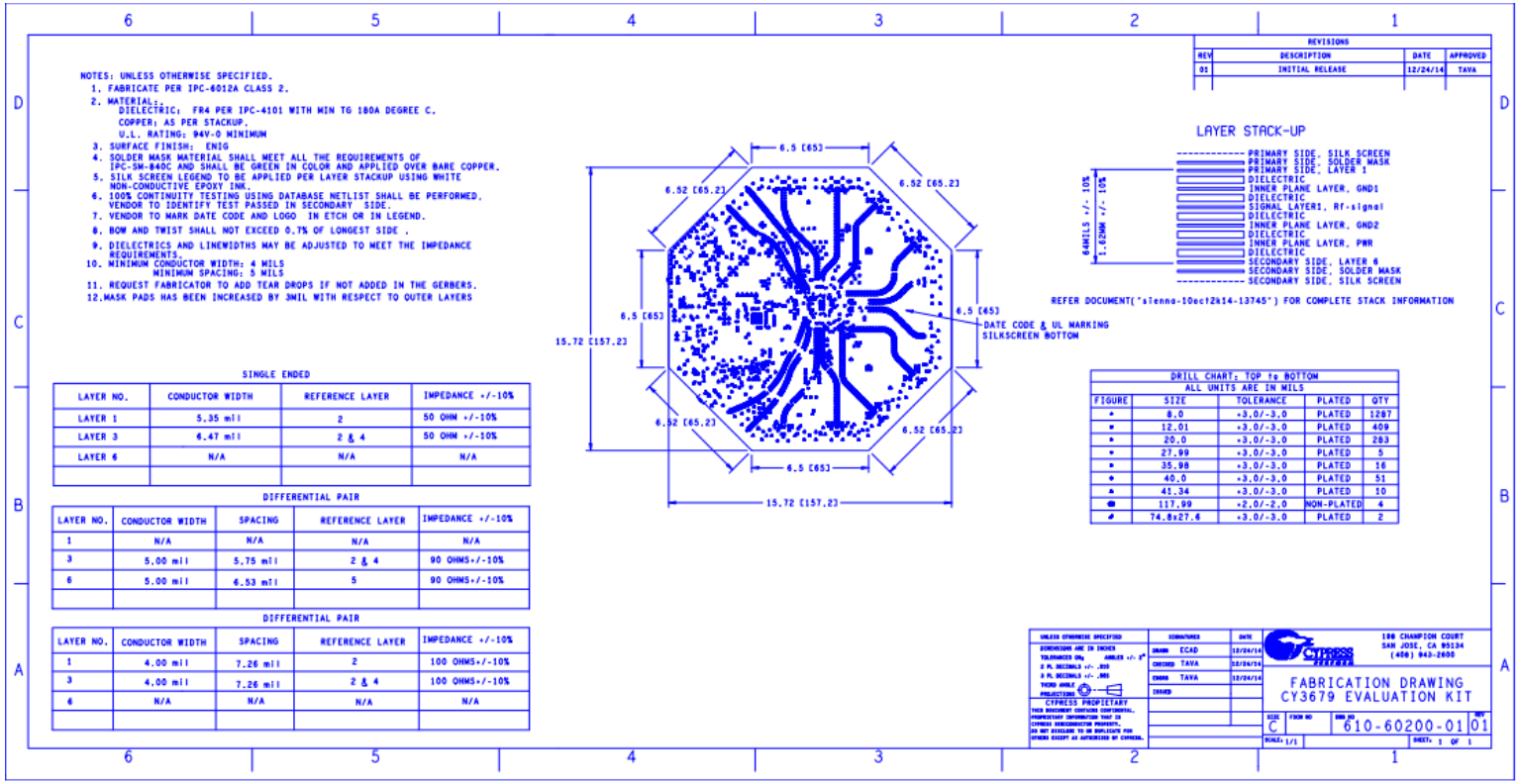


Figure A-10. Output Terminations: BANK 2



A.3. Fabrication Drawing

Figure A-11. Fabrication Drawing



A.4. Bill of Materials

Table A-4. Bill of Materials

Item	Qty	Reference	Part	MPN\PCB Footprint	Part Description	Manufacturer
1	96	C1, C7, C10, C13, C14, C24, C25, C26, C34, C36, C37, C38, C41, C42, C43, C44, C49, C50, C51, C53, C55, C57, C59, C61, C63, C65, C69, C72, C75, C78, C97, C98, C109, C110, C123, C124, C135, C136, C145, C148, C151, C154, C157, C163, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C198, C200, C201, C203, C204, C205, C93, C94, C99, C100, C105, C106, C111, C112, C119, C120, C125, C126, C131, C132, C137, C138	0.1 µF	CC0603ZRY5V9BB104	CAP CER 0.1UF 50V Y5V 0603	Yageo
2	25	C2, C8, C11, C20, C21, C22, C33, C35, C39, C40, C45, C70, C73, C76, C79, C83, C89, C146, C149, C152, C155, C158, C164, C197, C199	1 µF	TMK107BJ105KA-T	CAP CER 1UF 25V 10% X5R 0603	Taiyo Yuden
3	17	C3, C4, C5, C9, C12, C15, C16, C17, C18, C19, C23, C147 ,C150, C153, C156, C159, C165	10 µF	TAJA106K016R	CAP TANT 10UF 16V 10% 1206	AVX Corporation
4	1	C6	0.01 µF	GRM188R71H103KA01D	CAP CER 10000PF 50V 10% X7R 0603	Murata Electronics North America
5	1	C48	0.1 µF	C1206C104K5RAC7867	CAP CER 0.1UF 50V 10% X7R 1206	Kemet
6	10	C52, C54, C56, C58, C60, C62, C64, C66, C68, C196	0.047 µF	C0603C473J5RACTU	CAP CER 0.047UF 50V 5% X7R 0603	Kemet
7	4	C81, C84, C87, C90	0.1 nF	GRM1885C1H101JA01D	CAP CER 100PF 50V 5% NP0 0603	Murata Electronics North America
8	4	C117, C118, C143, C144	15 pF	500R07S150GV4T	CAP CER 15PF 50V 2% NP0 0402	Johanson Technology Inc
9	6	D1, D2, D3, D4, D5, D6	DIODE	MBRX120LF-TP	DIODE SCHOTTKY 20V 1A SOD123	Micro Commercial Co
10	8	D10, D11, D12, D13, D18, D19, D20, D24	DIODE TVS	CDSOD323-T18	TVS DIODE 18VWM 29VC SMD	Bourns Inc.
11	7	D14, D15, D16, D17, D21, D22, D23	ZENER, 3.6 V	MMSZ5227B-7-F	DIODE ZENER 3.6V 500MW SOD123	Diodes Incorporate
12	1	D25	ZENER, 4.7 V	MMSZ5230B-7-F	DIODE ZENER 4.7V 500MW SOD123	Diodes Incorporate
13	6	FB1, FB2, FB3, FB4, FB5, FB6	FERRITE BEAD	BLM18BB221SN1D	FERRITE CHIP 220 OHM 450MA 0603	Murata Electronics North America
14	10	F1, F2, F3, F4, F5, F6, F7, F8, F9, F10	PTC RESETABLE FUSE	MF-MSMF050-2	PTC RESETTABLE .50A 15V 1812	Bourns Inc.
15	5	H1, H3, H5, H6, H7	2-Pin Header	640456-2	CONN HEADER VERT 2POS .100 TIN	TE Connectivity
16	1	J3	USB MINI B	1734510-1	MINI USB RCPT R/A DIP	TE Connectivity
17	24	J5,J6,J7,J8,J10,J11,J12,J13,J14,J15,J16,J17,J18,J19,J20,J21,J22,J23,J24,J25,J26,J27,J28,J29	SMA	142-0701-801	CONN SMA JACK 50 OHM EDGE MNT	Cinch Connectivity Solutions Johnson
18	2	J30,J43	3-PIN JUMPER	9-146280-0-03	CONN HEADR BRKWAY .100 03POS STR	TE Connectivity
19	5	J38,J39,J40,J41,J42	POWER_SEL	9-146280-0-03	CONN HEADR BRKWAY .100 03POS STR	TE Connectivity
20	2	J44,J45	2-PIN JUMPER	9-146280-0-02	CONN HEADR BRKWAY .100 02POS STR	TE Connectivity
21	2	LED1,LED2	LED	CMD17-21VGC/TR8	LED GREEN CLEAR 0805 SMD	Visual Communications Company - VCC

Item	Qty	Reference	Part	MPN\PCB Footprint	Part Description	Manufacturer
22	24	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10,Q11,Q12,Q13,Q14,Q15,Q16,Q17,Q18,Q19,Q20,Q21,Q22,Q23,Q24	DMO2035U-7	DMP2035U-7	MOSFET P-CH 20V 3.6A SOT-23	Diodes Incorporated
23	2	R1,R2	560	ERJ-3GEYJ561V	RES SMD 560 OHM 5% 1/10W 0603	Panasonic Electronic Components
24	1	R3	100K	ERJ-3GEYJ104V	RES SMD 100K OHM 5% 1/10W 0603	Panasonic Electronic Components
25	6	R4,R5,R6,R8,R193,R197	100	ERJ-3EKF1000V	RES SMD 100 OHM 1% 1/10W 0603	Panasonic Electronic Components
26	1	R7	165	ERJ-3EKF1650V	RES SMD 165 OHM 1% 1/10W 0603	Panasonic Electronic Components
27	1	R9	43	ERJ-3EKF43R0V	RES SMD 43 OHM 1% 1/10W 0603	Panasonic Electronic Components
28	3	R16,R19,R190	15K	ERJ-3GEYJ153V	RES SMD 15K OHM 5% 1/10W 0603	Panasonic Electronic Components
29	2	R17,R18	22	ERJ-3EKF22R0V	RES SMD 22 OHM 1% 1/10W 0603	Panasonic Electronic Components
30	3	R20,R21,R191	30K	ERJ-3GEYJ303V	RES SMD 30K OHM 5% 1/10W 0603	Panasonic Electronic Components
31	1	R22	4.7K	ERJ-3GEYJ472V	RES SMD 4.7K OHM 5% 1/10W 0603	Panasonic Electronic Components
32	12	R23,R30,R31,R32,R203,R204,R205,R206,R207,R208,R209,R210	1K	RC0603JR-071KL	RES SMD 1K OHM 5% 1/10W 0603	Yageo
33	3	R24,R89,R143	0	ERJ-3GEY0R00V	RES SMD 0.0 OHM JUMPER 1/10W	Panasonic Electronic Components
34	2	R26,R27	4.7K	ERJ-2GEJ472X	RES SMD 4.7K OHM 5% 1/10W 0402	Panasonic Electronic Components
35	19	R29,R54,R68,R80,R81,R94,R95,R106,R107,R108,R122,R134,R135,R148,R149,R160,R161,R211,R212	0	ERJ-2GE0R00X	RES SMD 0.0 OHM JUMPER 1/10W ; (0402 package)	Panasonic Electronic Components
36	2	R33,R36	1K	ERJ-2GEJ102X	RES SMD 1K OHM 5% 1/10W 0402	Panasonic Electronic Components
37	4	R55,R69,R109,R123	33	1-1879208-3	RES SMD 33 OHM 0.1% 1/16W 0402	TE Connectivity
38	4	R56,R70,R115,R124	130	ERA-2AEB131X	RES SMD 130 OHM 0.1% 1/16W 0402	Panasonic Electronic Components
39	6	R59,R63,R85,R116,R117,R139	3K	ERJ-3GEYJ302V	RES SMD 3K OHM 5% 1/10W 0603	Panasonic Electronic Components
40	4	R62,R74,R112,R128	49.9	ERA-2AEB49R9X	RES SMD 49.9 OHM 0.1% 1/16W 0402	Panasonic Electronic Components
41	6	R66,R67,R92,R120,R121,R146	2K	RC0603FR-072KL	RES SMD 2K OHM 1% 1/10W 0603	Yageo
42	5	R86,R101,R142,R155,R201	49.9	ERA-3AEB49R9V	RES SMD 49.9 OHM 0.1% 1/10W 0603	Panasonic Electronic Components
43	1	SW1	PUSH BUTTON	EVQ-PE105K	SWITCH TACTILE SPST-NO 0.05A 12V	Panasonic Electronic Components

Item	Qty	Reference	Part	MPN\PCB Footprint	Part Description	Manufacturer
44	1	SW2	3-POS DIP	209-3MS	SWITCH RAISED ACTUATOR 3 SEC 50V	CTS Electrocomponents
45	3	U2,U3,U4	NCP1117DTAG	NCP1117DTAG	IC REG LDO ADJ 1A DPAK	ON Semiconductor
46	1	U7	CY8C5868LTI-LP039 QFN68	CY8C5868LTI-LP039	IC MCU 32BIT 256KB FLASH 68QFN	Cypress Semiconductor
47	1	U8	CY27410FLTXI	CY27410FLTXI	4-PLL High Performance Clock Generator	Cypress Semiconductor
48	1	Y1	CRYSTAL4/SM	NX3225GA-27.000M-STD-CRG-1	CRYSTAL 27MHZ 8PF SMD	NDK
49	7	R172,R173,R174,R175,R176,R177,R178	120	CR0603-FX-1200ELF	RES SMD 120 OHM 1% 1/10W 0603	Bourns Inc.
Labels						
50	1	N/A	N/A	N/A	N/A	LBL, PCA Identification Label, Vendor Code, Datecode, Serial Number(YYWWVVXXXX)
51	1	N/A	N/A	N/A	N/A	LBL, QR Code, CY3679
Stickers						
52	1	N/A	N/A	N/A	N/A	LBL, KIT Sticker 'CY3679 EVALUATION KIT' , 25mm x 2mm
53	1	N/A	N/A	N/A	N/A	LBL, KIT Sticker '600-60208-01 REV01' , 17mm x 2mm
No Load Comments						
54	2	C46,C47	DNM, 8-pF	C1608C0G1H080D080AA	r-cr0603	CAP CER 8PF 50V C0G 0603
55	2	C82,C88	DNM, 0.1 UF	CC0603ZRY5V9BB104	r-cr0603	CAP CER 0.1UF 50V Y5V 0603
56	22	R14,R15,R180,R181,R182,R186,R187,R188,R189,R200,R202,R25,R57,R61,R84,R87,R111,R114,R138,R140,R35,R45	DNM, 0-ohm	ERJ-3GEY0R00V	r-cr0603	RES SMD 0.0 OHM JUMPER 1/10W
57	12	R34,R42,R44,R52,R82,R88,R96,R100,R136,R141,R150,R154	DNM, 49.9-ohm	ERA-2AEB49R9X	r-cr0402	RES SMD 49.9 OHM 0.1% 1/16W 0402
58	11	R28,R37,R40,R64,R65,R90,R91,R118,R119,R144,R145	DNM, 0-ohm	ERJ-2GE0R00X	r-cr0402	RES SMD 0.0 OHM JUMPER 1/10W
59	2	R38,R49	DNM, 100-ohm	ERJ-2RKF1000X	r-cr0402	RES SMD 100 OHM 1% 1/10W 0402
60	14	R39,R48,R58,R60,R71,R75,R83,R97,R110,R113,R125,R129,R137,R151	DNM, 49.9-ohm	ERA-3AEB49R9V	r-cr0603	RES SMD 49.9 OHM 0.1% 1/10W 0603
61	2	R93,R147	2k, DNM	RC0603FR-072KL	r-cr0603	RES SMD 2K OHM 1% 1/10W 0603
62	6	R192,R194,R195,R196,R198,R199	DNM, 100-ohm	ERJ-3EKF1000V	r-cr0603	RES SMD 100 OHM 1% 1/10W 0603
63	1	J4	I2C HEADER	22-23-2051	hdr5_keyed_m	CONN HEADER 5POS .100 VERT TIN

Item	Qty	Reference	Part	MPN\PCB Footprint	Part Description	Manufacturer
64	1	X1	OSC, DNM	EG-2121CA 125.0000M-PHPAL3	osc_eg_2102ca	OSC SO 125.000MHZ LVPECL SMD
65	21	TP1,TP2,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22	T POINT R		tp_60c40dp	

Revision History

Document Revision History

Document Title: CY3679 Evaluation Kit User Guide Document Number: 001-95978			
Revision	**Issue Date**	**Origin of Change**	**Description of Change**
**	03/31/2015	MEMJ	Initial version of the kit guide.