SDLS008

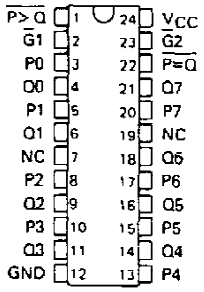
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

D2617, JANUARY 1981 – REVISED MARCH 1988

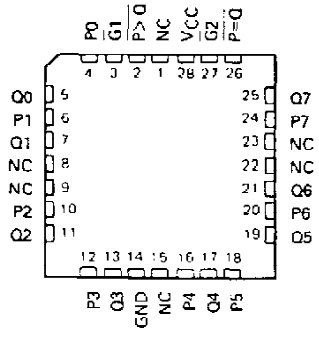
- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-kΩ Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

TYPE	$\overline{P = Q}$	$\overline{P > Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no

SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE
(TOP VIEW)

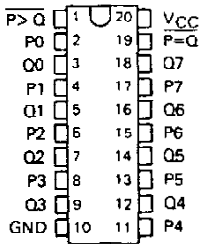


SN54LS687 . . . FK PACKAGE
(TOP VIEW)

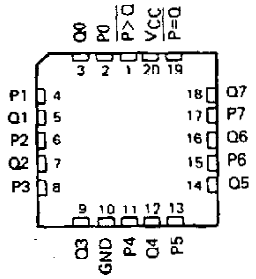


NC – No internal connection

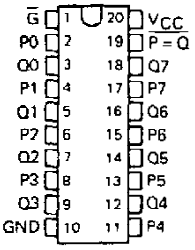
SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE
(TOP VIEW)



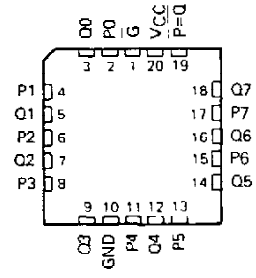
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE
(TOP VIEW)



SN54LS688 . . . J PACKAGE
SN74LS688 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS688 . . . FK PACKAGE
(TOP VIEW)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P = Q}$ outputs and all except 'LS688 provide $\overline{P > Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

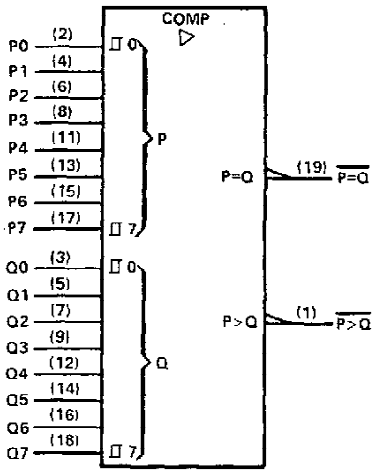
FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}$, $\overline{G1}$	$\overline{G2}$		
P = Q	L	X	L	H
P > Q	X	L	H	L
P < Q	X	X	H	H
P = Q	H	X	H	H
P > Q	X	H	H	H
X	H	H	H	H

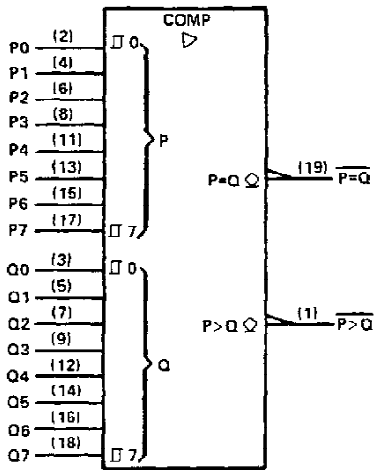
NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687, $\overline{G}1$ enables $\overline{P=Q}$ and $\overline{G}2$ enables $\overline{P>Q}$.

logic symbols†

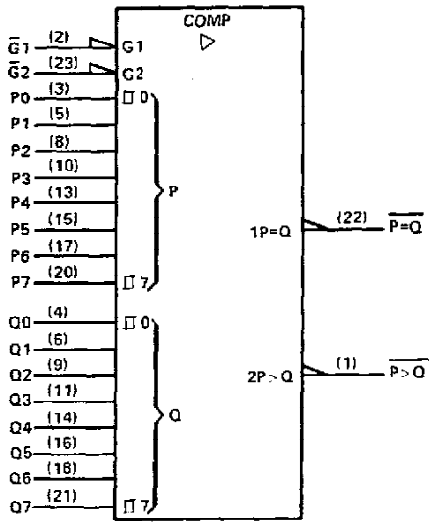
'LS682, 'LS684



'LS685



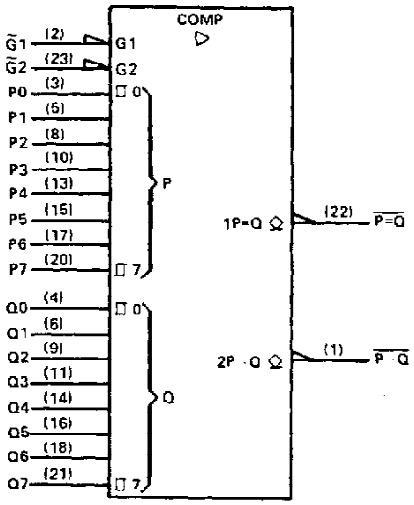
'LS686



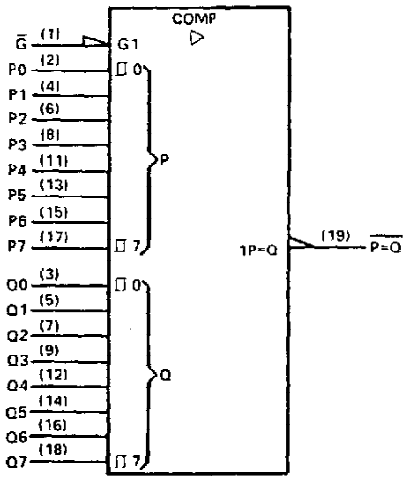
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, JT, N, and NT packages.

logic symbols† (continued)

'LS687

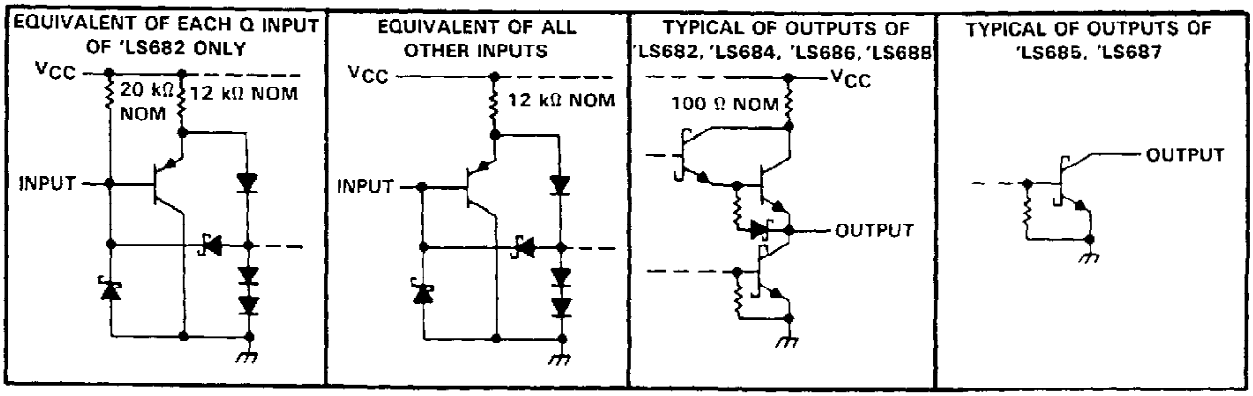


'LS688

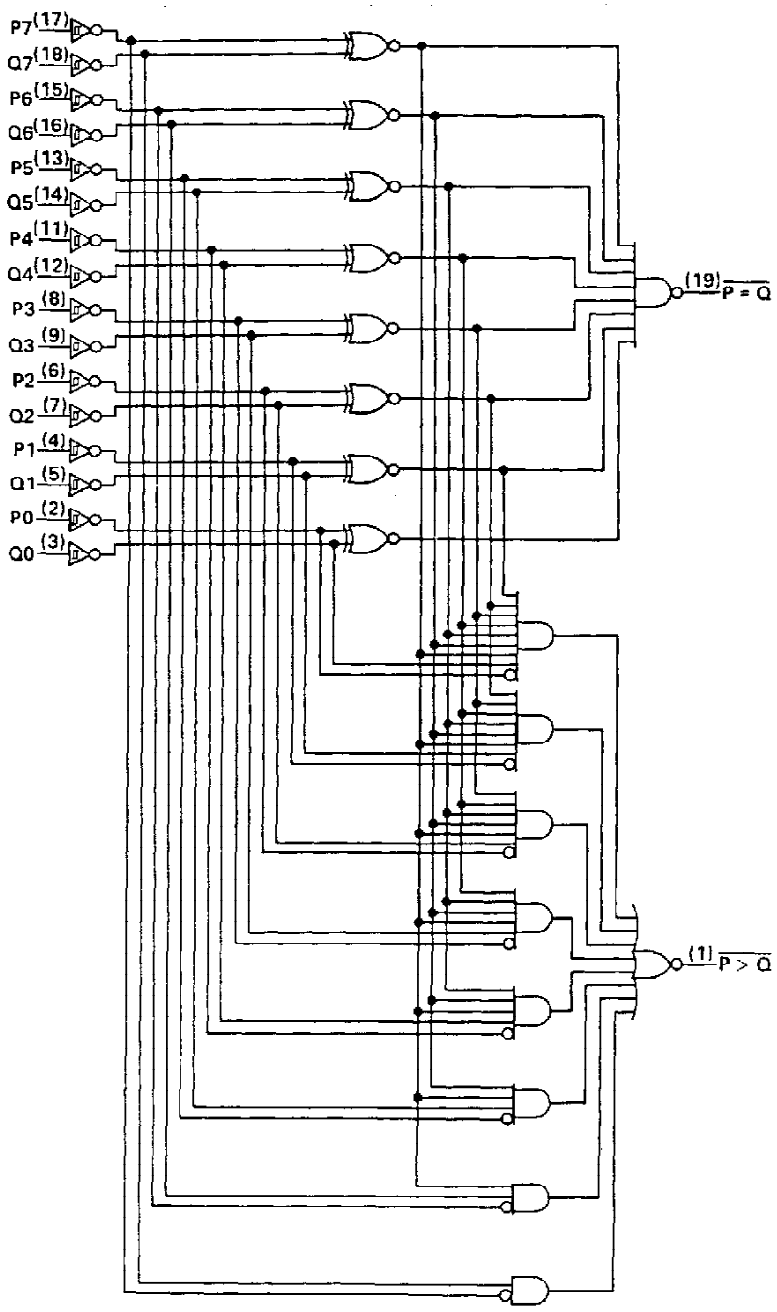


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, JT, N, and NT packages.

schematics of inputs and outputs

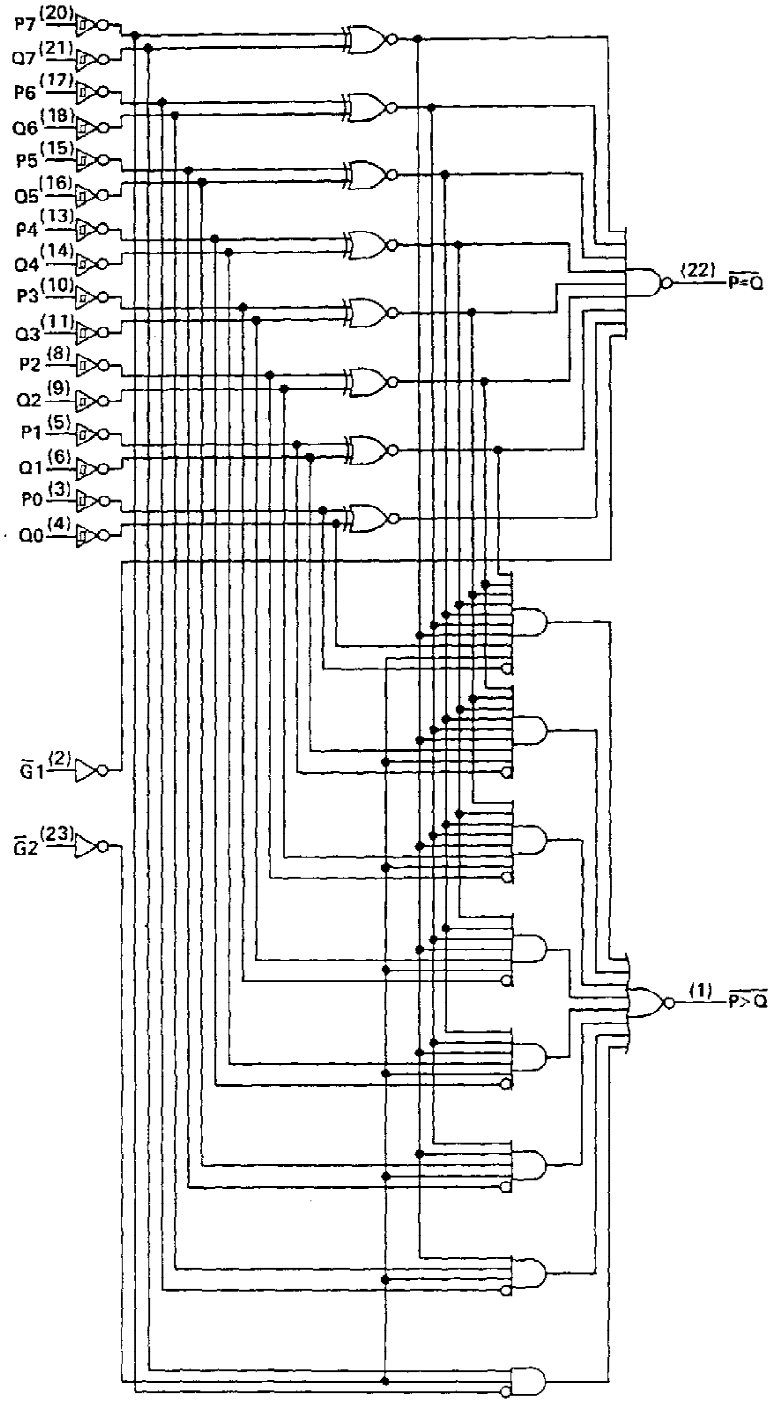


'LS682, 'LS684, 'LS685 logic diagram (positive logic)



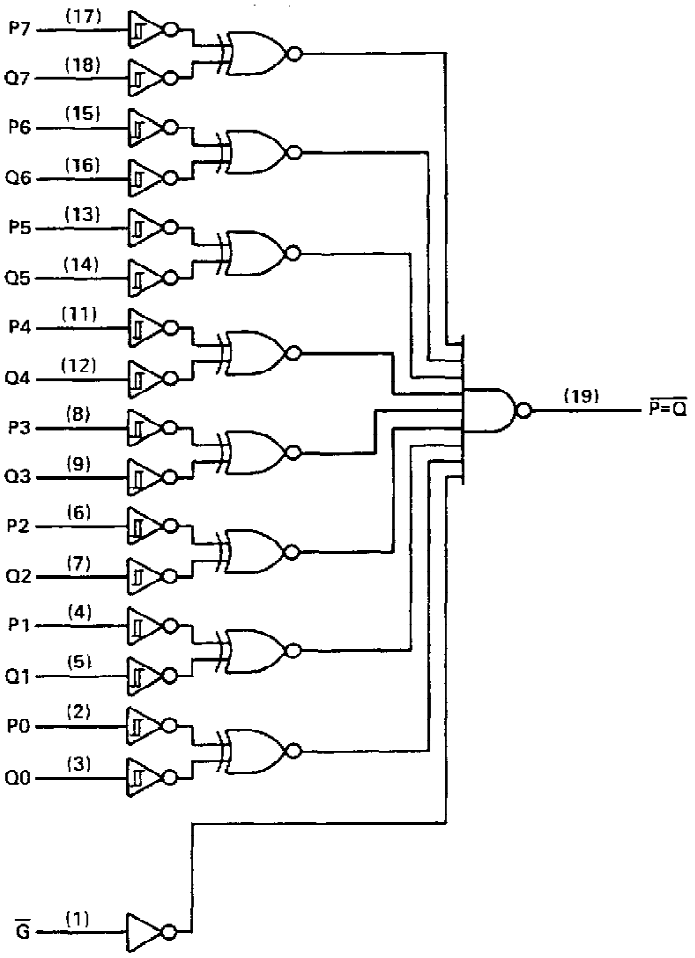
Pin numbers shown are for DW, J, and N packages.

'LS686, 'LS687 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: Q inputs of 'LS682 . . . . . 5.5 V
All other inputs . . . . . 7 V
Off-state output voltage: 'LS685, 'LS687 . . . . . 7 V
Operating free-air temperature range:
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 . . . . . −55°C to 125°C
SN74LS682, SN74LS684 thru SN74LS688 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+}-V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{OS}§	Short-circuit output current		V_{CC} = MAX,	V_O = 0	−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS682	V_{CC} = MAX,	See Note 1		42	70		42	70	mA
		'LS684				40	65		40	65	
		'LS686				44	75		44	75	
		'LS688				40	65		40	65	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 1: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 2		13	25		15	25		13	25		12	18	ns
t_{PHL}					15	25		17	25		20	30		17	23	
t_{PLH}	Q	$\overline{P=Q}$			14	25		16	25		13	25		12	18	ns
t_{PHL}					15	25		15	25		21	30		17	23	
t_{PLH}	$\overline{G}$, $\overline{G}1$	$\overline{P=Q}$									11	20		12	18	ns
t_{PHL}											19	30		13	20	
t_{PLH}	P	$\overline{P>Q}$			20	30		22	30		19	30				ns
t_{PHL}					15	30		17	30		15	30				
t_{PLH}	Q	$\overline{P>Q}$			21	30		24	30		18	30				ns
t_{PHL}					19	30		20	30		19	30				
t_{PLH}	$\overline{G}2$	$\overline{P>Q}$									21	30				ns
t_{PHL}											16	25				

†t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I			V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{CC}	Supply current	'LS685	V_{CC} = MAX,	See Note 1		40	65		40	65	mA
		'LS687				44	75		44	75	

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: I_{CC} is measure with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS685			'LS687			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 2		30	45		24	35	ns
t_{PHL}					19	35		20	30	
t_{PLH}	Q	$\overline{P=Q}$			24	45		24	35	ns
t_{PHL}					23	35		20	30	
t_{PLH}	$\overline{G}$, $\overline{G}1$	$\overline{P=Q}$						21	35	ns
t_{PHL}								18	30	
t_{PLH}	P	$\overline{P>Q}$			32	45		24	35	ns
t_{PHL}					16	35		16	30	
t_{PLH}	Q	$\overline{P>Q}$			30	45		24	35	ns
t_{PHL}					20	35		16	30	
t_{PLH}	$\overline{G}2$	$\overline{P>Q}$						24	35	ns
t_{PHL}								15	30	

†t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84151012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84151012A SNJ54LS 682FK	Samples
84151012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84151012A SNJ54LS 682FK	Samples
8415101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	Samples
8415101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	Samples
8415101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	Samples
8415101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	Samples
84152012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK	Samples
8415201RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J	Samples
8415201SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201SA SNJ54LS684W	Samples
84153012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK	Samples
8415301RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J	Samples
8415301SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W	Samples
SN54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS682J	Samples
SN54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS682J	Samples
SN54LS684J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS684J	Samples
SN54LS688J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS688J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS682DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682	Samples
SN74LS682N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS682N	Samples
SN74LS682N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS682N	Samples
SN74LS682NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS682	Samples
SN74LS682NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS682	Samples
SN74LS684DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684	Samples
SN74LS684DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684	Samples
SN74LS684N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS684N	Samples
SN74LS684NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS684N	Samples
SN74LS684NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS684	Samples
SN74LS686DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74LS686NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS687NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS687NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74LS688DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS688DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	Samples
SN74LS688DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688	Samples
SN74LS688N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS688N	Samples
SN74LS688N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS688NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS688N	Samples
SN74LS688NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS688	Samples
SNJ54LS682FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84151012A SNJ54LS 682FK	Samples
SNJ54LS682FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84151012A SNJ54LS 682FK	Samples
SNJ54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	Samples
SNJ54LS682J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J	Samples
SNJ54LS682W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	Samples
SNJ54LS682W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W	Samples
SNJ54LS684FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK	Samples
SNJ54LS684J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J	Samples
SNJ54LS684W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415201SA SNJ54LS684W	Samples
SNJ54LS688FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK	Samples
SNJ54LS688J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS688W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS682, SN54LS684, SN54LS688, SN54LS688-SP, SN74LS682, SN74LS684, SN74LS688 :

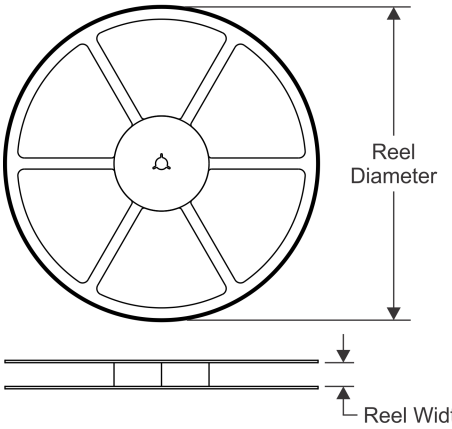
- Catalog: SN74LS682, SN74LS684, SN74LS688, SN54LS688
- Military: SN54LS682, SN54LS684, SN54LS688
- Space: SN54LS688-SP

NOTE: Qualified Version Definitions:

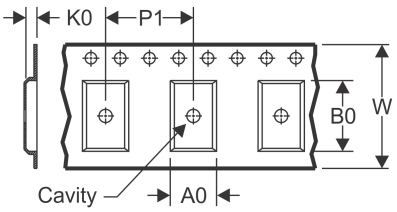
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

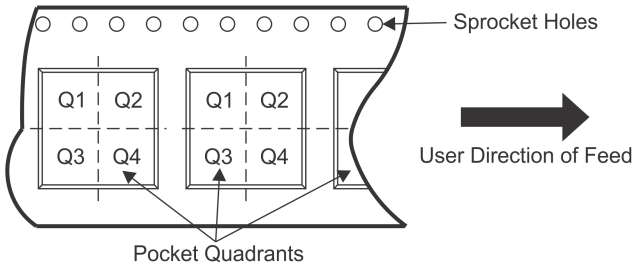


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

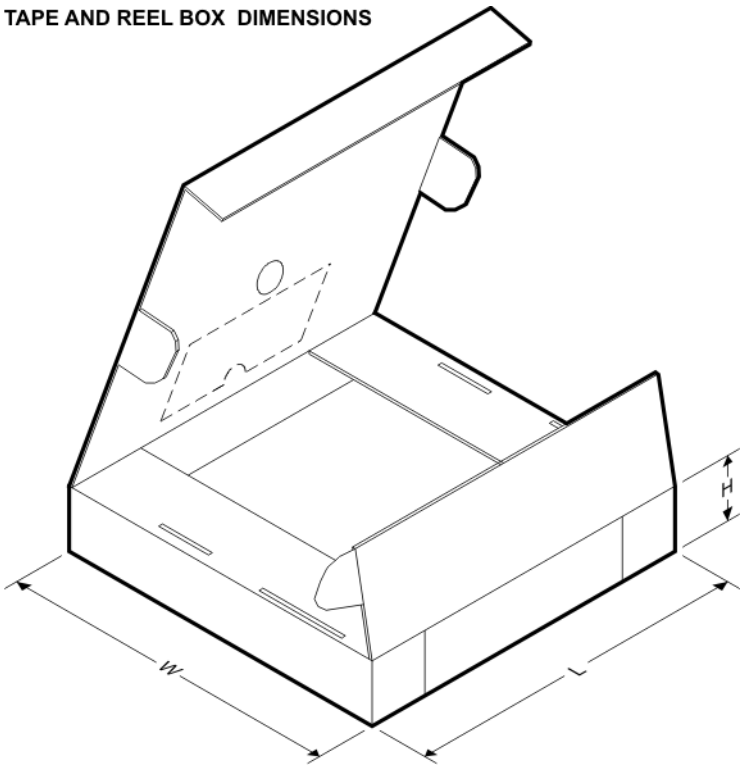
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS682DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS682NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74LS684DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS684NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1
SN74LS688DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS688NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	4.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



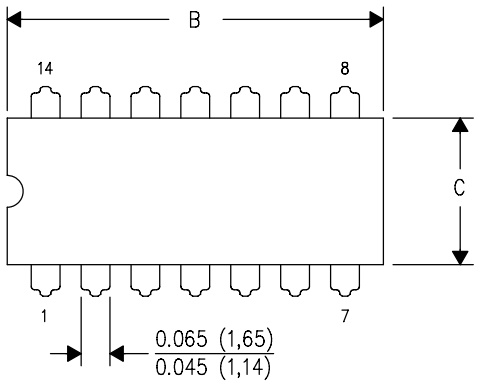
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS682DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS682NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS684DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS684NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS688DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS688NSR	SO	NS	20	2000	367.0	367.0	45.0

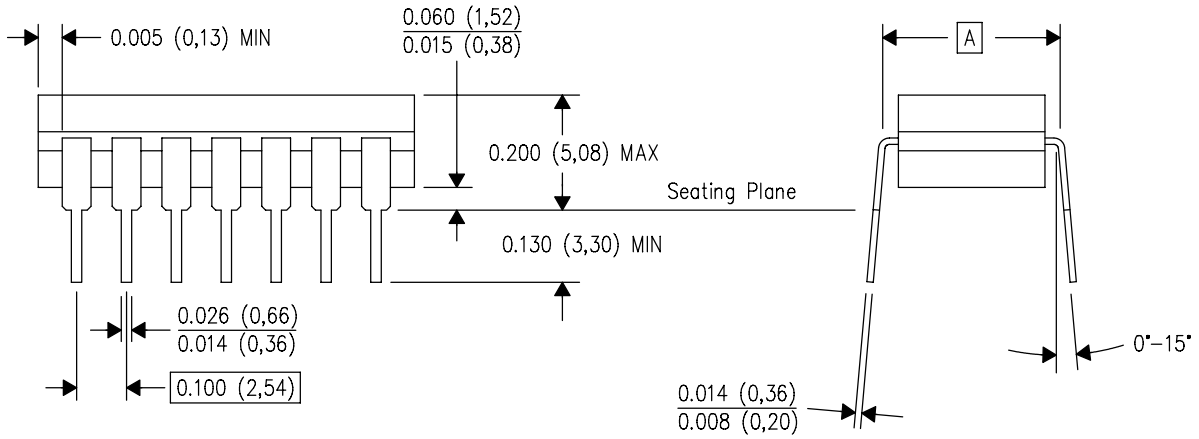
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



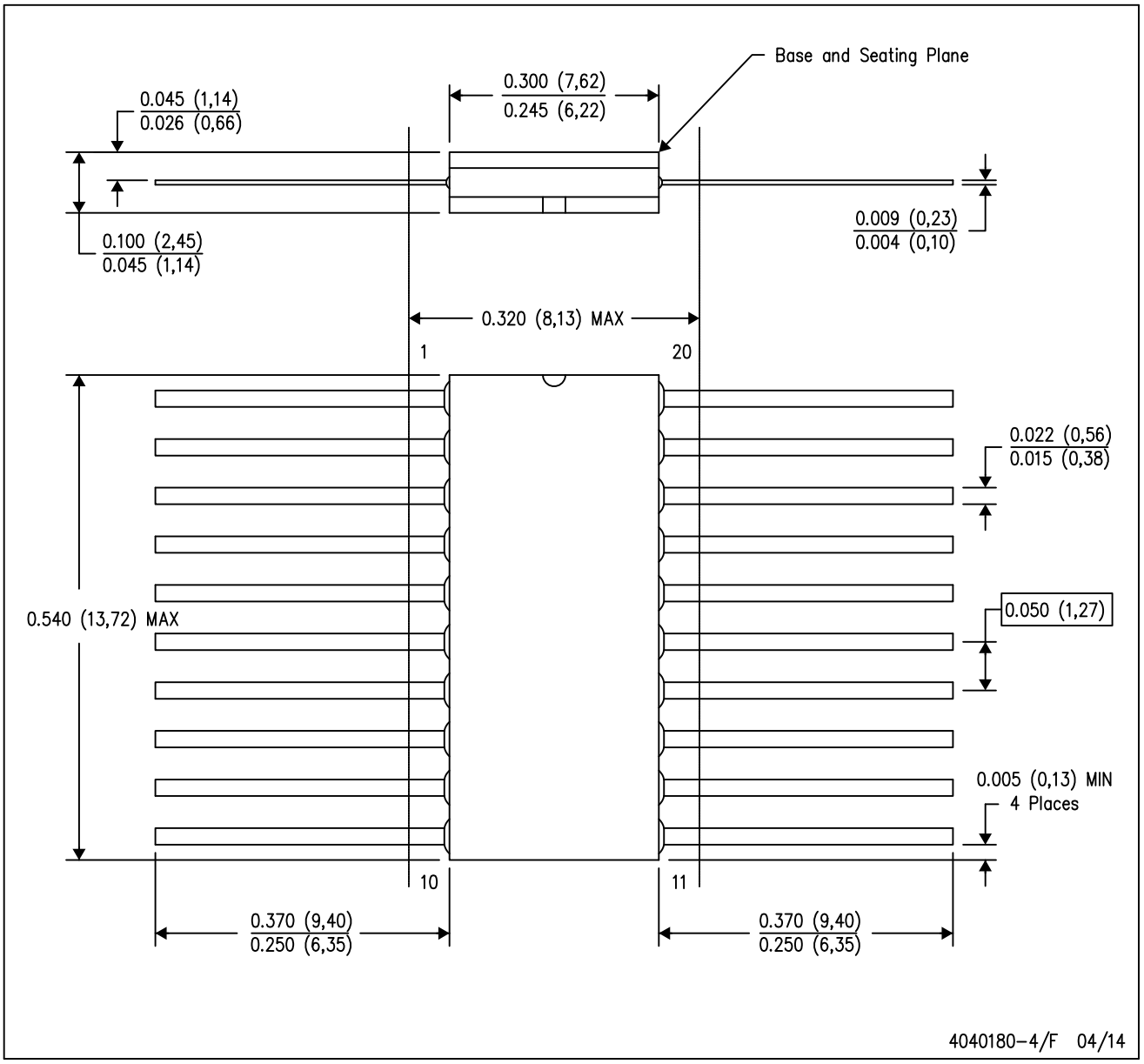
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

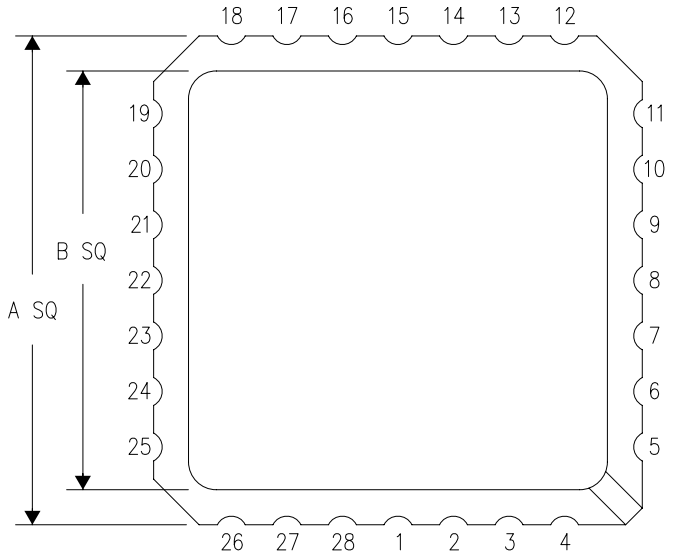
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



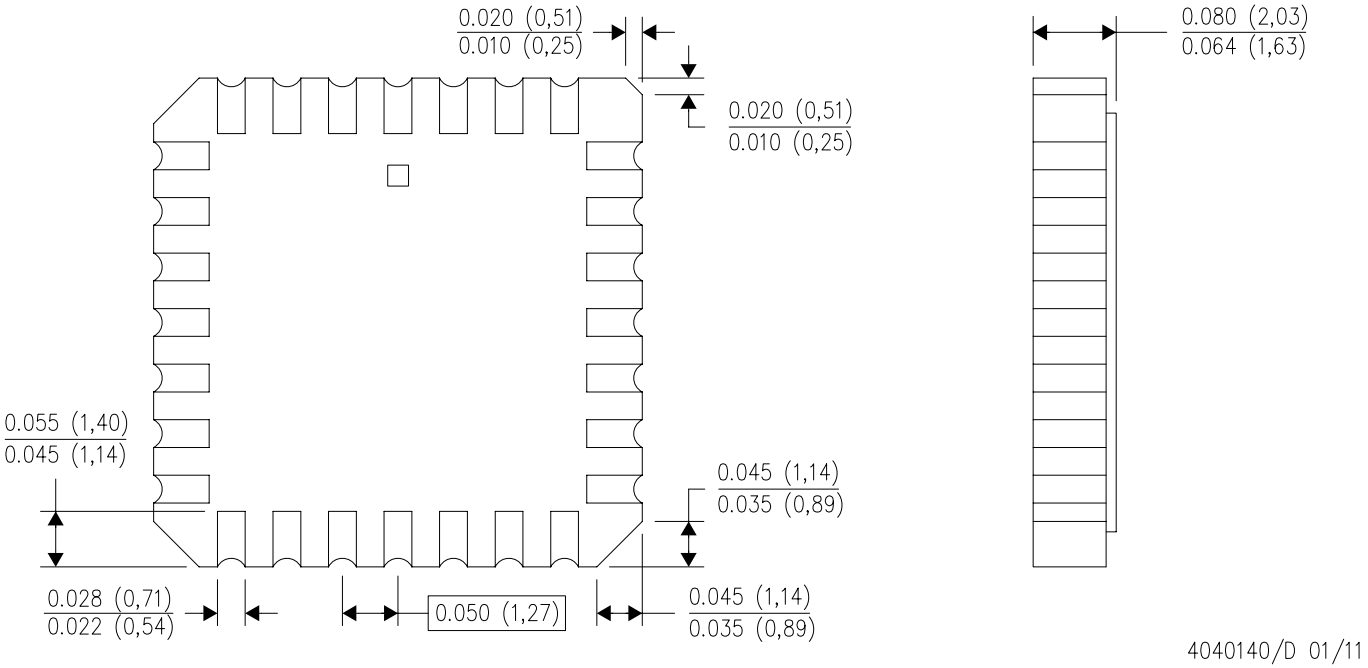
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



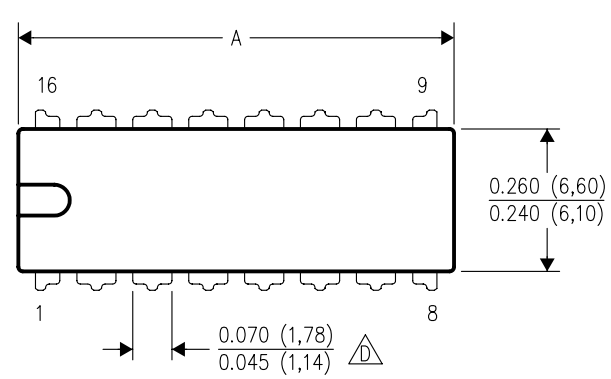
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

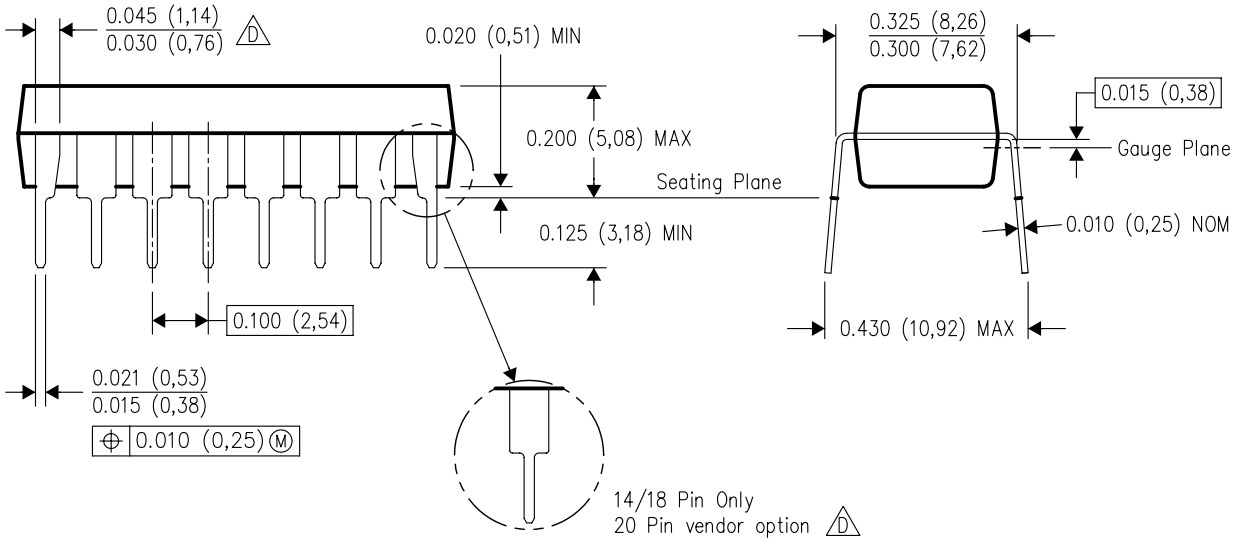
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

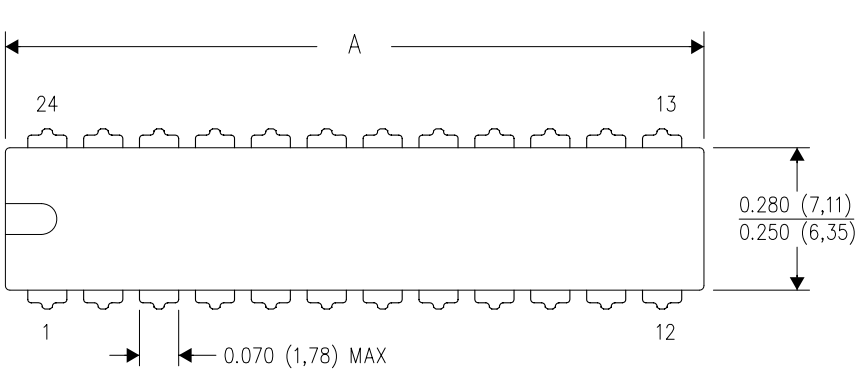


4040049/E 12/2002

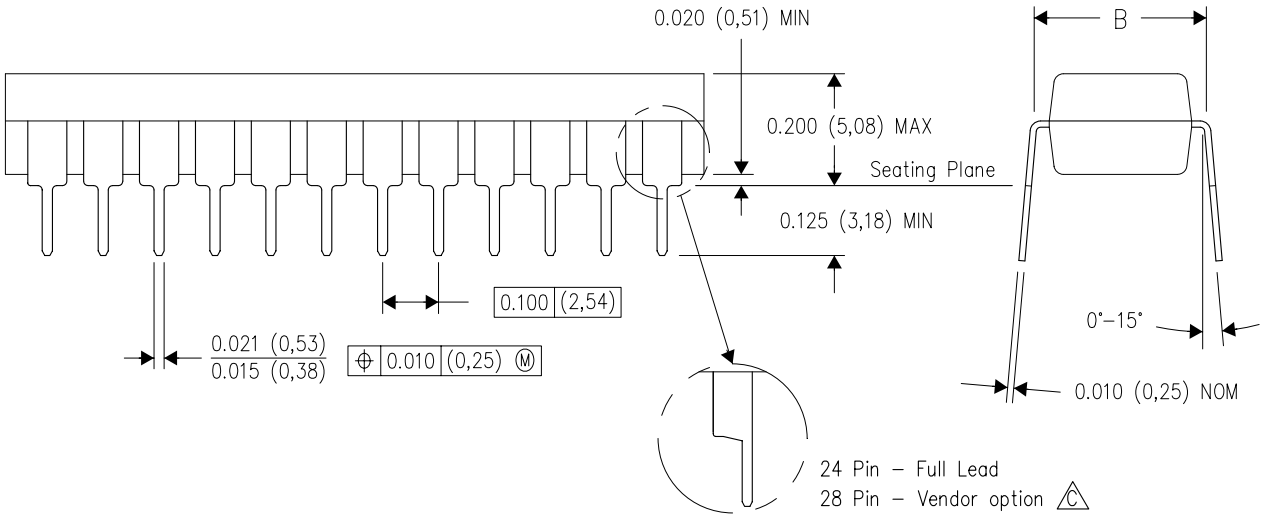
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



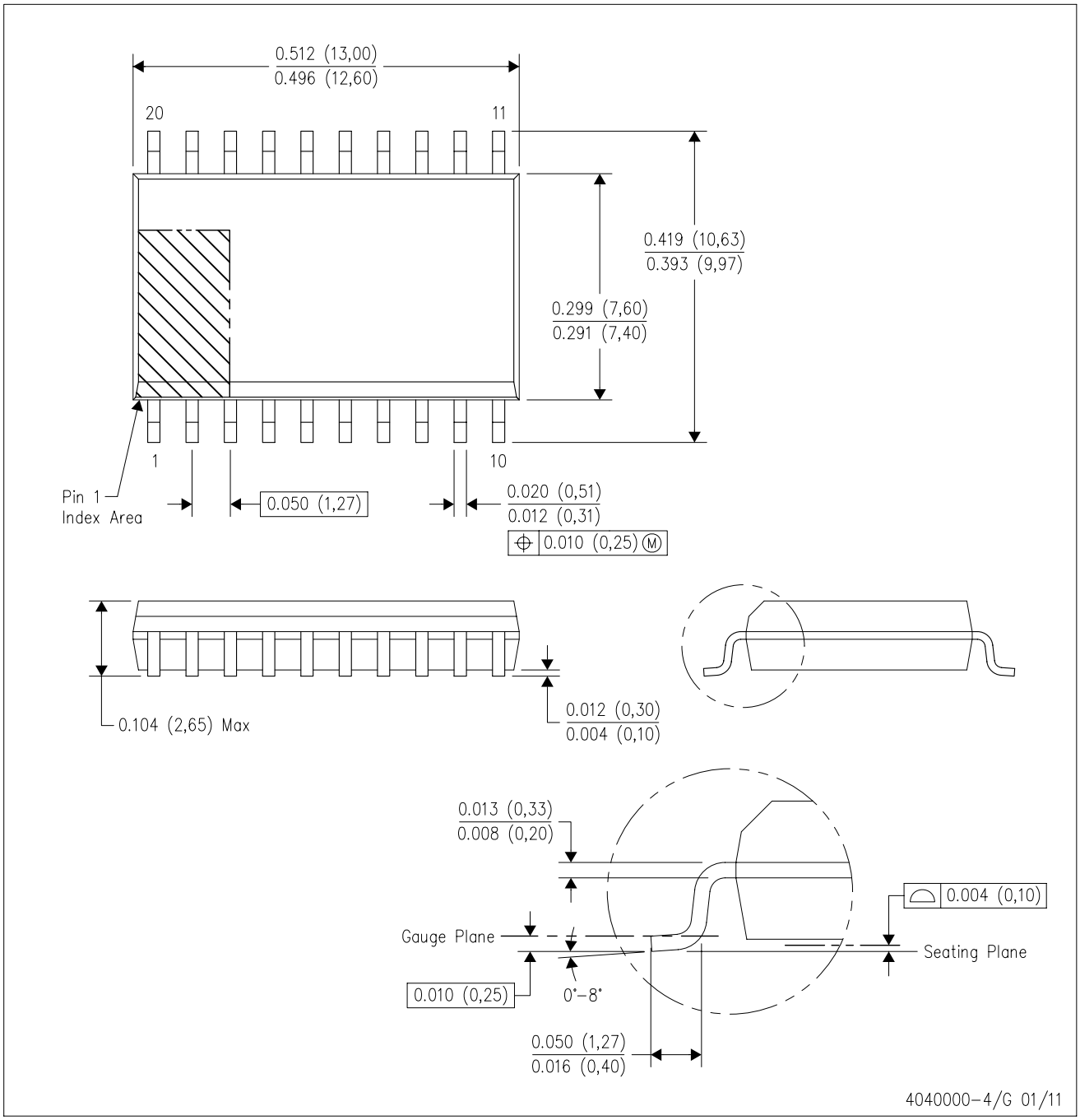
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

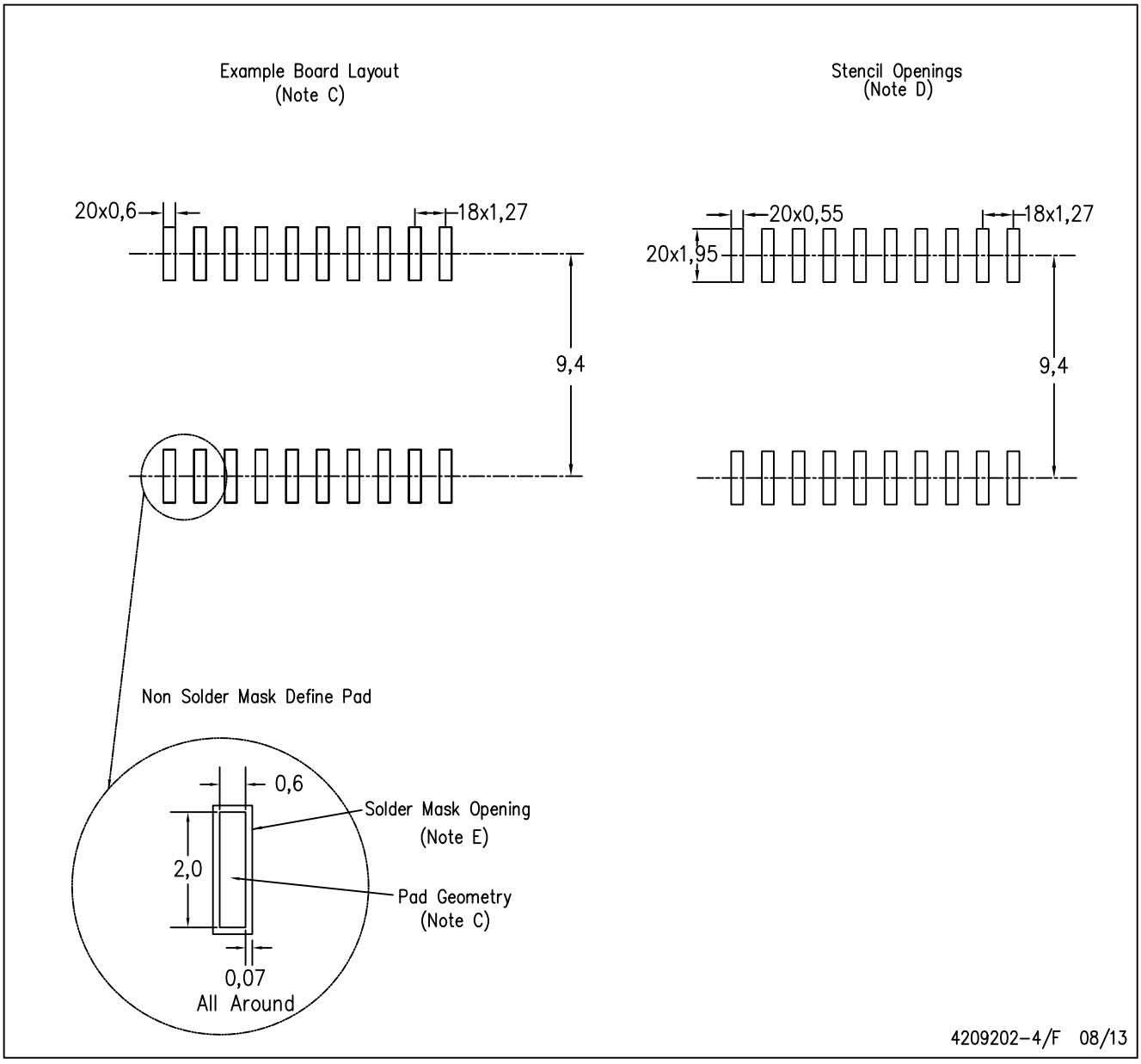
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



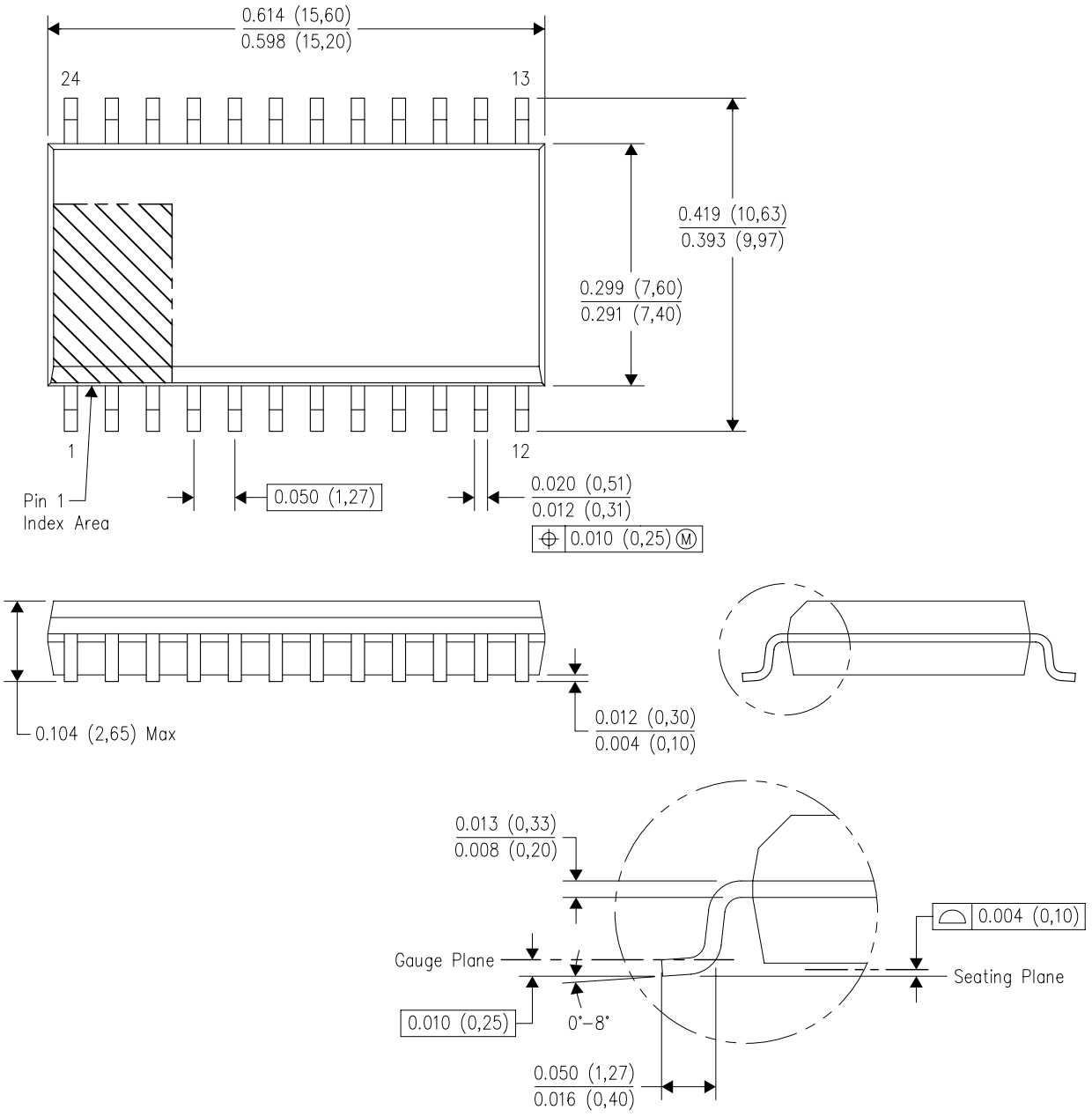
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

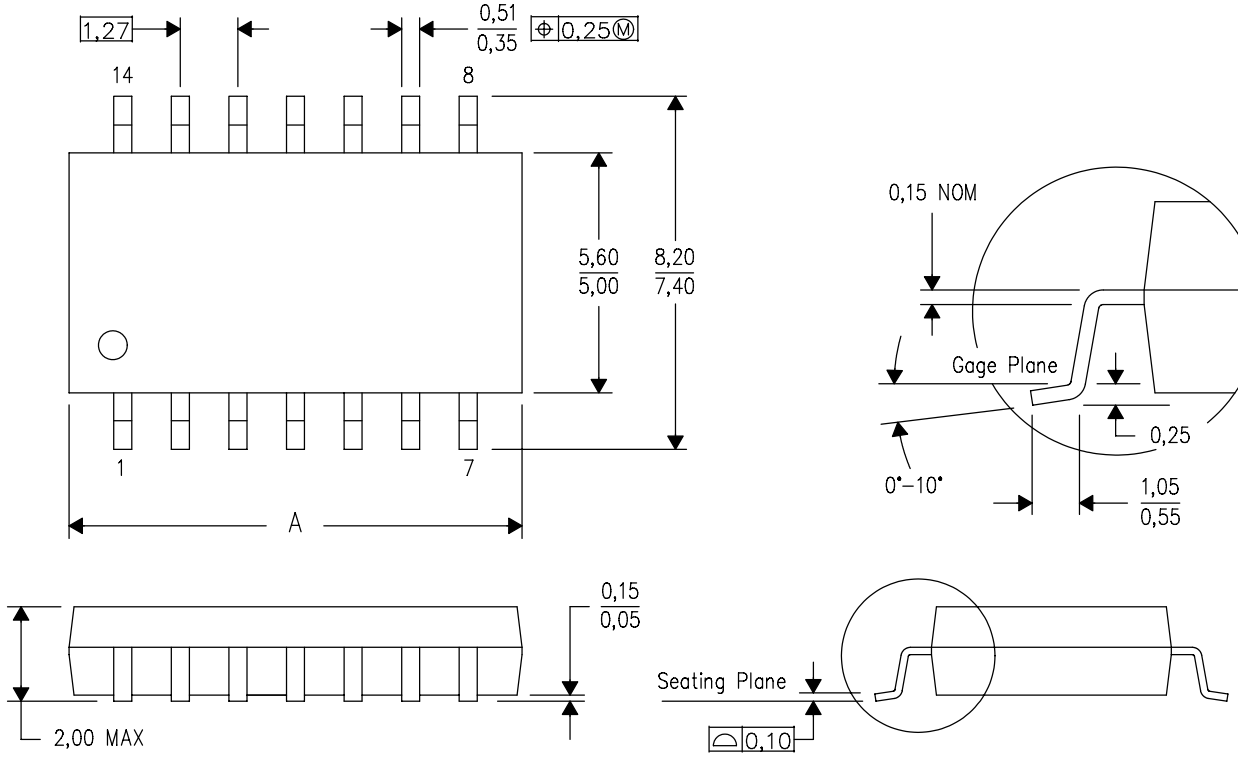


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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