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Maximum Power Enhancement Techniques for SOT-223 Power MOSFETs

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1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SOT-223 Power MOSFET offered by Fairchild Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of Fairchild's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain lead of the Power MOSFET is mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

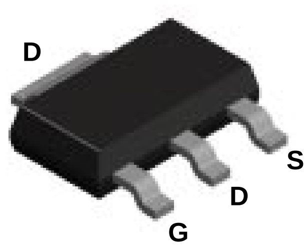

Figure 1. SOT-223 Power MOSFET achieves junction-to-case thermal resistance $R_{\theta JC}$ of 12°C/W.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \quad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

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where P_{Dmax} (t) and $R_{\theta JA}$(t) are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}$(t) increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details. Nevertheless, Fairchild provides a Discrete SPICE Thermal Model (LIT# 570240-002) for general thermal evaluation. The user may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (2.3)$$

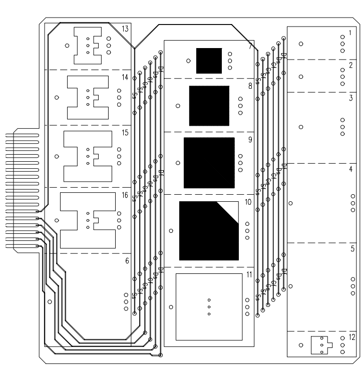
The case thermal reference of the SOT-223 Power MOSFET is defined as the point of contact between the drain lead of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. Layouts 1 to 6 have the copper pad sizes from 0.0123 to 1 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.2 to 1 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.132 to 1 square inches divided equally on both sides of the board.



Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.0123, 0.066, 0.03, 0.53, 0.76, 1	Top
7-11	0.2, 0.4, 0.6, 0.8, 1	Bottom
12-16	0.132, 0.35, 0.568, 0.784, 1	1/2 Top and 1/2 Bottom

Table 1: Thermal Board Configurations

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

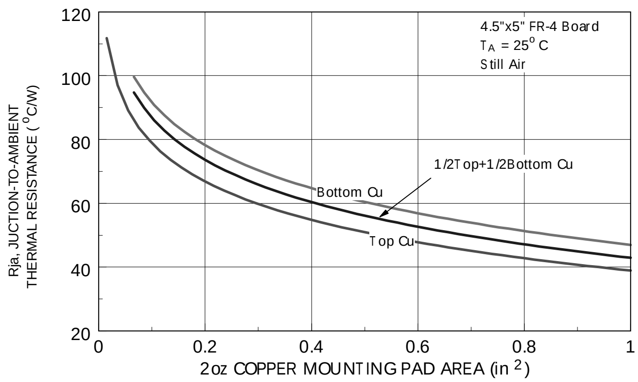


Figure 3. SOT-223 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 110 to 40°C/W in the range from 0.0123 to 1 square inches. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 10 to 15°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 18% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.0123 to 0.066 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

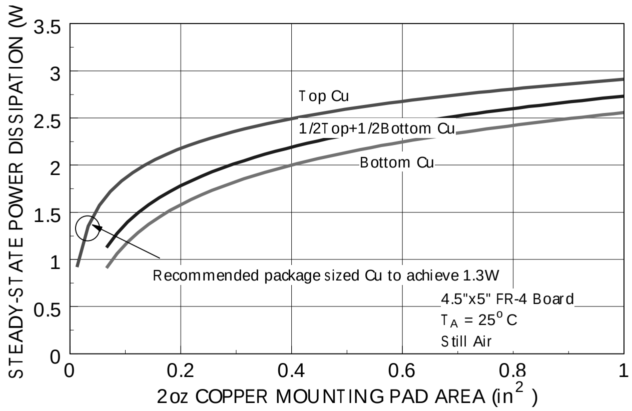


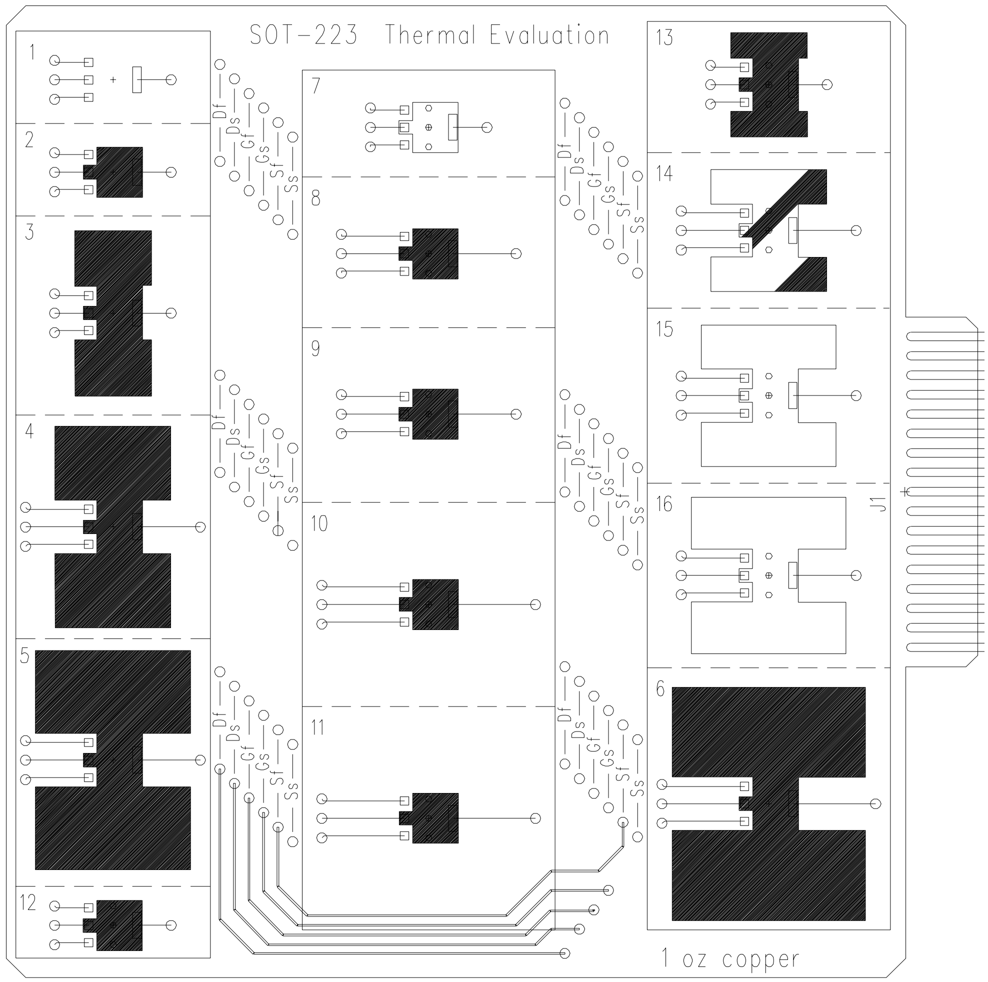
Figure 4. Maximum Power Dissipation Curves for SOT-223. In layout 2, 0.066 in² 2 Oz copper mounting pad area is recommended to achieve approximately 1.3W.

4. Conclusion

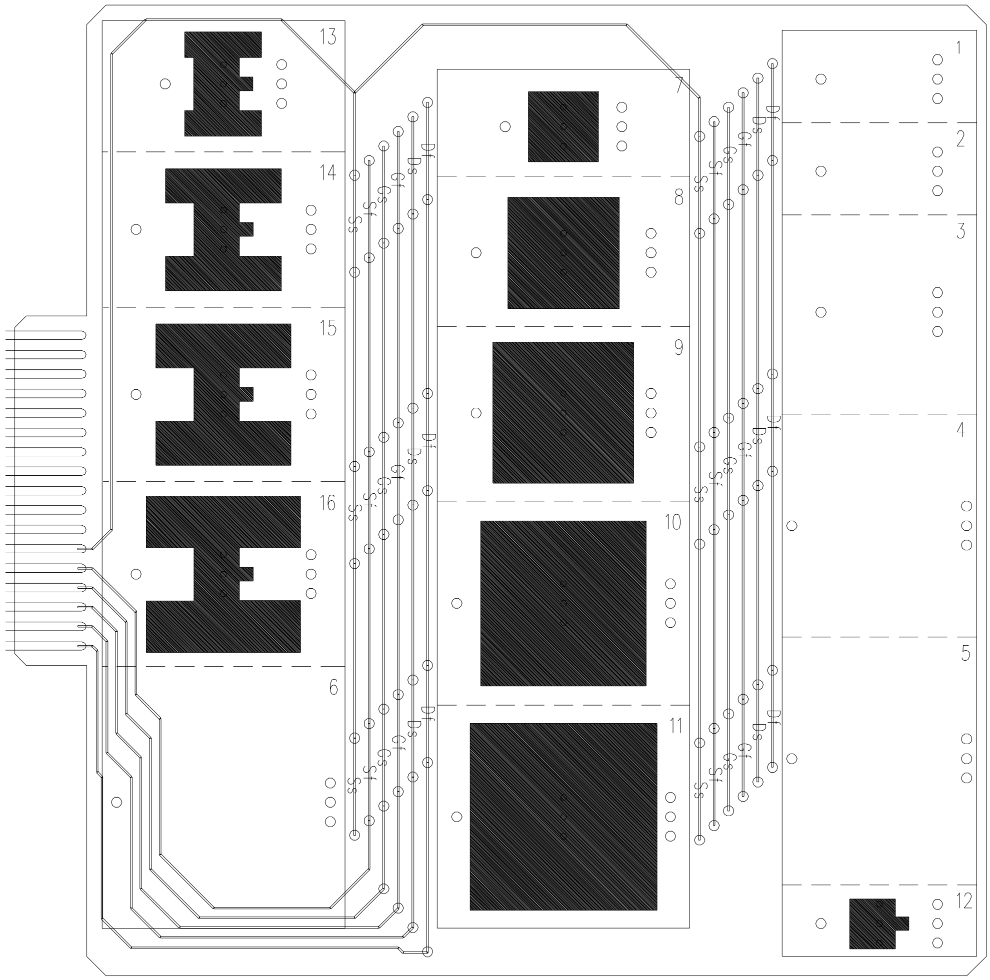
Fairchild Semiconductor has attempted to define the thermal performance of the SOT-223 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

- Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
- Placement of the copper pads on the top side of the board gives the best thermal performance.
- The most cost effective approach of designing layout 2 0.066 square inches copper pad directly under the package, without occupying additional board space, can increase the maximum power from approximately 1.1 to 1.3W.

5. SOT-223 Thermal Board Top View in Actual Scale



SOT-223 Thermal Board Bottom View in Actual Scale



Appendix A

Heat Flow Theory Applied to Power MOSFETs

When a Power MOSFET operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one dimensional steady-state model of conduction heat transfer is demonstrated in figure 5. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. There are also secondary heat paths. One is from the package to the ambient air. The other is from the drain lead frame to the detached source and gate leads then to the printed circuit board. These secondary heat paths are assumed to be negligible contributors to the heat flow in this analysis.

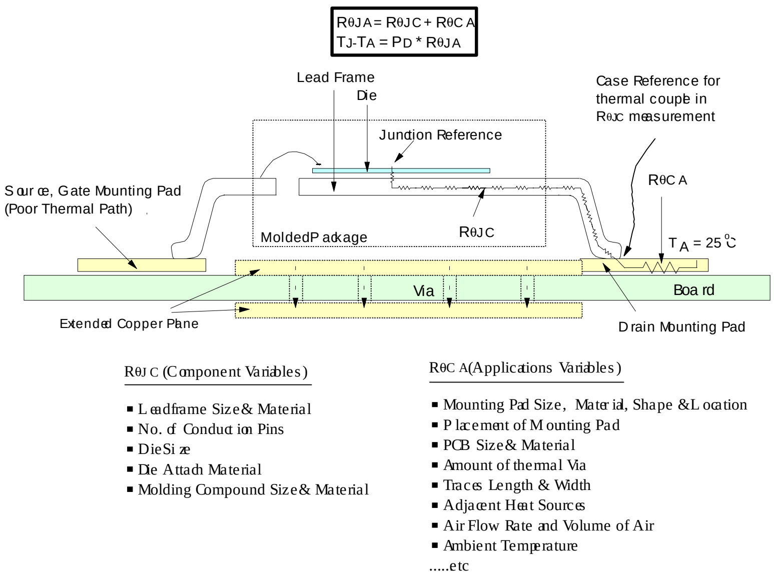


Figure 5: Cross-sectional view of a Power MOSFET mounted on a printed circuit board. Note that the case temperature is measured at the point where the drain lead(s) contact with the mounting pad surface.

The increase of junction temperature above the surrounding environment is directly proportional to dissipated power and the thermal resistance.

The steady-state junction-to-ambient thermal resistance, $R_{\theta JA}$, is defined as
$R_{\theta JA} = (T_J - T_A) / P$

where T_J is the average temperature of the device junction. The term junction refers to the point of thermal reference of the semiconductor device. T_A is the average temperature of the ambient environment. P is the power applied to the device which changes the junction temperature.

$R_{\theta JA}$ is a function of the junction-to-case $R_{\theta JC}$ and case-to-ambient $R_{\theta CA}$ thermal resistance

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where the case of a Power MOSFET is defined at the point of contact between the drain lead(s) and the mounting pad surface. $R_{\theta JC}$ can be controlled and measured by the component manufacturer independent of the application and mounting method and is therefore the best means of comparing various suppliers component specifications for thermal performance. On the other hand, it is difficult to quantify $R_{\theta CA}$ due to heavy dependence on the application. Before using the data sheet thermal data, the user should always be aware of the test conditions and justify the compatibility in the application.

Appendix B

Thermal Measurement

Prior to any thermal measurement, a K factor must be determined. It is a linear factor related to the change of intrinsic diode voltage with respect to the change of junction temperature. From the slope of the curve shown in figure 6, K factor can be determined. It is approximately 2.2mV/°C for most Power MOSFET devices.

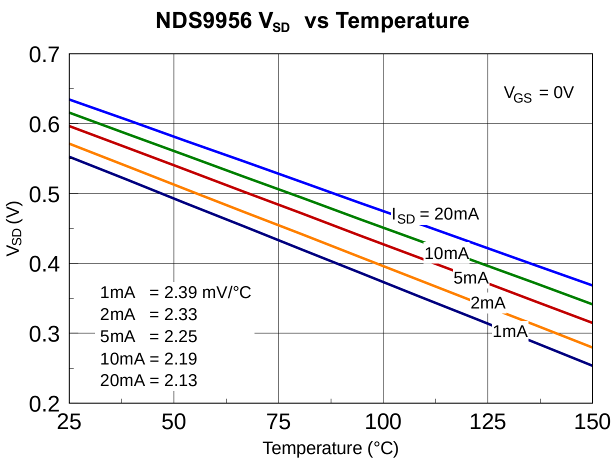


Figure 6. K factors, slopes of a V_{SD} vs temperature curves, of a typical Power MOSFET

After the K factor calibration, the drain-source diode voltage of the device is measured prior to any heating. A pulse is then applied to the device and the drain-source diode voltage is measured 30us following the end of the power pulse. From the change of the drain-source diode voltage, the K factor, input power, and the reference temperature, the time dependent single pulsed junction-to-reference thermal resistance can be calculated. From the single pulse curve on figure 7, duty cycle curves can be determined. Note: a curve set in which $R_{\theta JA}$ is specified indicates that the part was characterized using the ambient as the thermal reference. The board layout specified in the data sheet notes will help determine the applicability of the curve set.

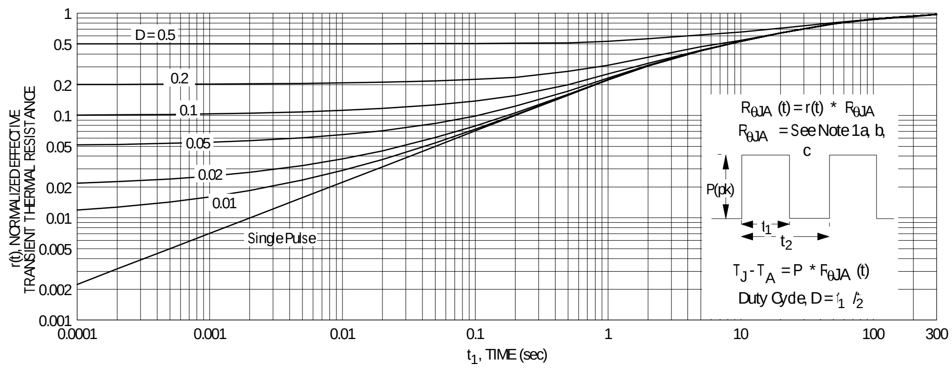


Figure 7. Normalized Transient Thermal Resistance Curves

B.1 Junction-to-Ambient Thermal Resistance Measurement

Equipment and Setup:
- Tesec DV240 Thermal Tester
- 1 cubic foot still air environment
- Thermal Test Board with 16 layouts defined by the size of the copper mounting pad and their relative surface placement. For layouts with copper on the top and bottom planes, there are 0.02 inch copper plated vias (heat pipes) connecting the two planes. See figure 2 and table 1 on the thermal application note for board layout and description. The conductivity of the FR-4 PCB used is 0.29 W/m-C. The length is 5.00 inches ± 0.005; width 4.50 inches ± 0.005; and thickness 0.062 inches ± 0.005. 2Oz copper clad PCB.

The junction-to-ambient thermal measurement was conducted in accordance with the requirements of MIL-STD-883 and MIL-STD-750 with the exception of using 2 Oz copper and measuring diode current at 10mA.

A test device is soldered on the thermal test board with minimum soldering. The copper mounting pad reaches the remote connection points through fine traces. Jumpers are used to bridge to the edge card connector. The fine traces and jumpers do not contribute significant thermal dissipation but serve the purpose of electrical connections. Using the intrinsic diode voltage measurement described above, the junction-to-ambient thermal resistance can be calculated.

B.2 Junction-to-Case Thermal Resistance Measurement

Equipment and Setup:
- Tesec DV240 Thermal Tester
- large aluminum heat sink
- type-K thermocouple with FLUKE 52 K/J Thermometer

The drain lead(s) is soldered on a 0.5 x 1.5 x 0.05 copper plate. The plate is mechanically clamped to a heat sink which is large enough to be considered ideal. Thermal grease is applied in-between the two planes to provide good thermal contact. Theoretically the case temperature should be held constant regardless of the conditions. Thus a thermocouple is used and fixed at the point of contact between the drain lead(s) and the copper plate surface, to account for any heatsink temperature change. Using the intrinsic diode voltage measurement described earlier, the junction-to-case thermal resistance can be obtained. A plot of junction-to-case thermal resistance for various packages is shown in figure 8. Note $R_{\theta JC}$ can vary with die size and the effect is more prominent as $R_{\theta JC}$ decreases.

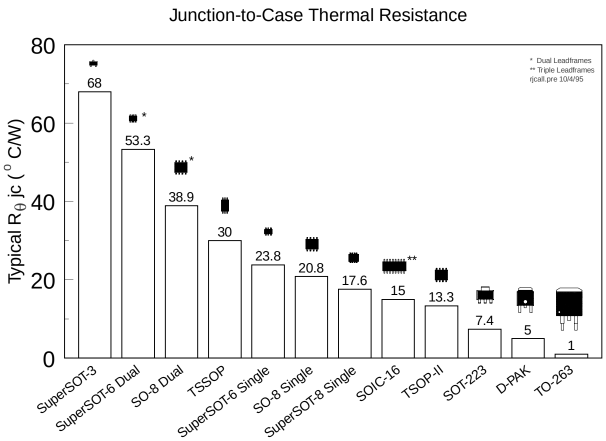


Figure 8. Junction-to-case thermal resistance $R_{\theta JC}$ of various surface mount Power MOSFET packages.

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