



MAC97A8

4Q Triac

1 May 2015

Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 plastic package intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power phase control
- General purpose low power switching
- Solid-state relay

4. Quick reference data

Table 1. Quick reference data

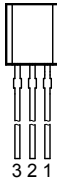
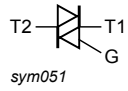
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 50\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	0.6	A
Static characteristics						
I_{GT}	gate trigger current	$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G+; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	1	5	mA
		$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2	5	mA
		$V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2- G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2	5	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	4	7	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
MAC97A8	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
MAC97A8/DG	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 50\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	0.6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	8	A
		full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	8.8	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.32	A^2s
dl_T/dt	rate of rise of on-state current	$I_G = 10\text{ mA}$; T2+ G+	-	50	$\text{A}/\mu\text{s}$
		$I_G = 10\text{ mA}$; T2+ G-	-	50	$\text{A}/\mu\text{s}$
		$I_G = 14\text{ mA}$; T2- G+	-	10	$\text{A}/\mu\text{s}$
		$I_G = 10\text{ mA}$; T2- G-	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 2\text{ microseconds (max)}$	-	1	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period; $T(lead) \leq 80\text{ }^{\circ}\text{C}$; $t = 2\text{ microseconds (max)}$	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$

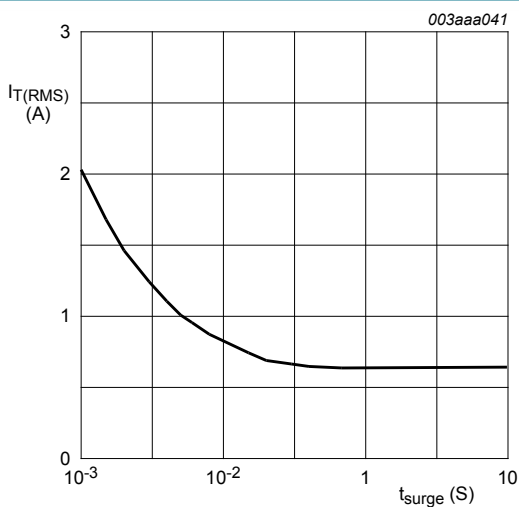


Fig. 1. RMS on-state current as a function of surge duration; maximum values

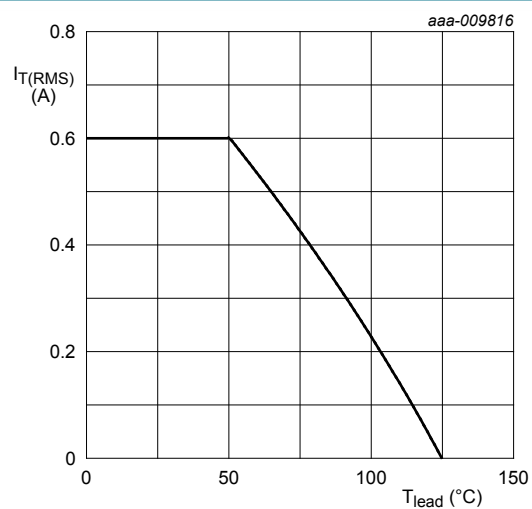
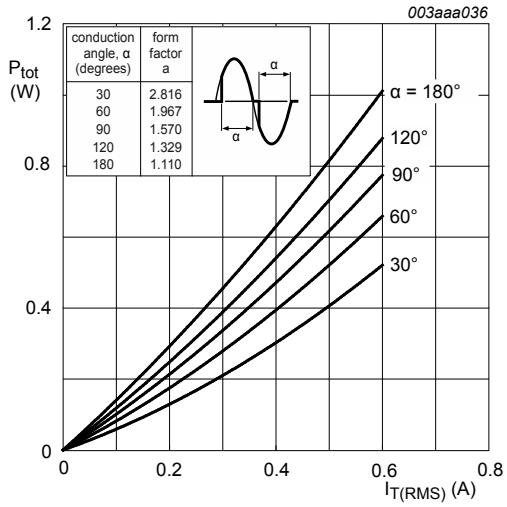
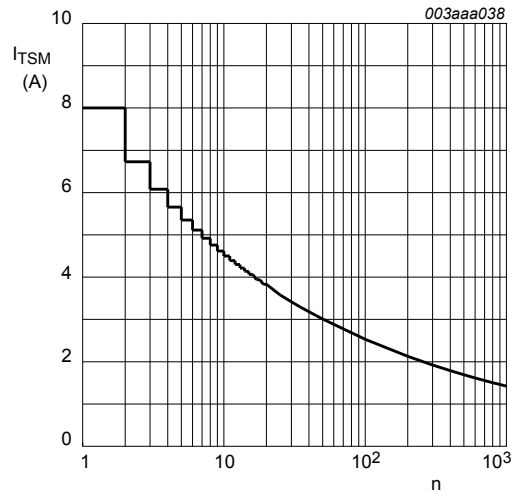


Fig. 2. RMS on-state current as a function of lead temperature; maximum values



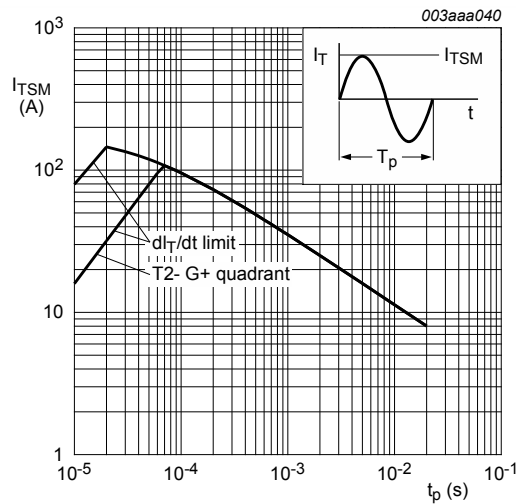
α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50$ Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

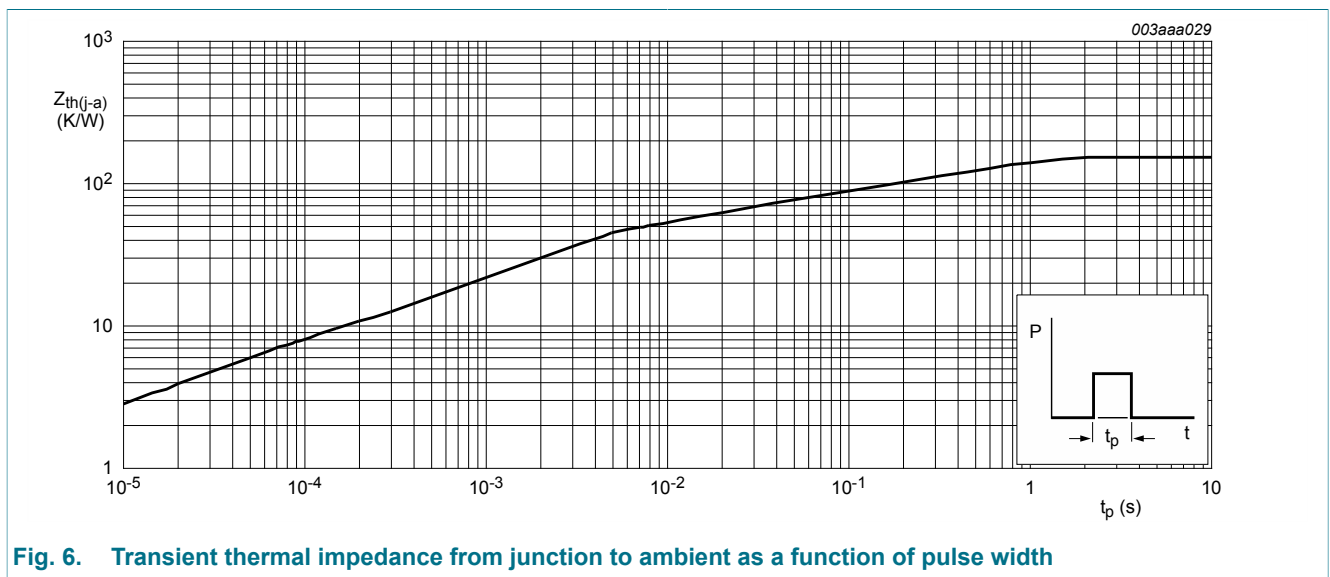


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	-	1	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	-	2	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	-	2	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7	-	4	7	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8	-	1	10	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8	-	5	10	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8	-	1	10	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8	-	2	10	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9	-	1	10	mA
V _T	on-state voltage	I _T = 0.85 A; T _j = 25 °C; Fig. 10	-	1.4	1.9	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.9	1.5	V
		V _D = 400 V; I _T = 0.1 A; T _j = 110 °C; Fig. 11	0.1	0.7	-	V
I _D	off-state current	V _D = 600 V; T _j = 110 °C	-	3	100	μA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 110 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 12	30	45	-	V/μs
dV _{com} /dt	rate of change of commutating voltage	V _D = 600 V; T _j = 50 °C; dI _{com} /dt = 0.3 A/ms; I _T = 0.84 A; gate open circuit	-	5	-	V/μs
t _{gt}	gate-controlled turn-on time	I _{TM} = 1 A; V _D = 600 V; I _G = 25 mA; dI _G /dt = 5 A/μs	-	2	-	μs

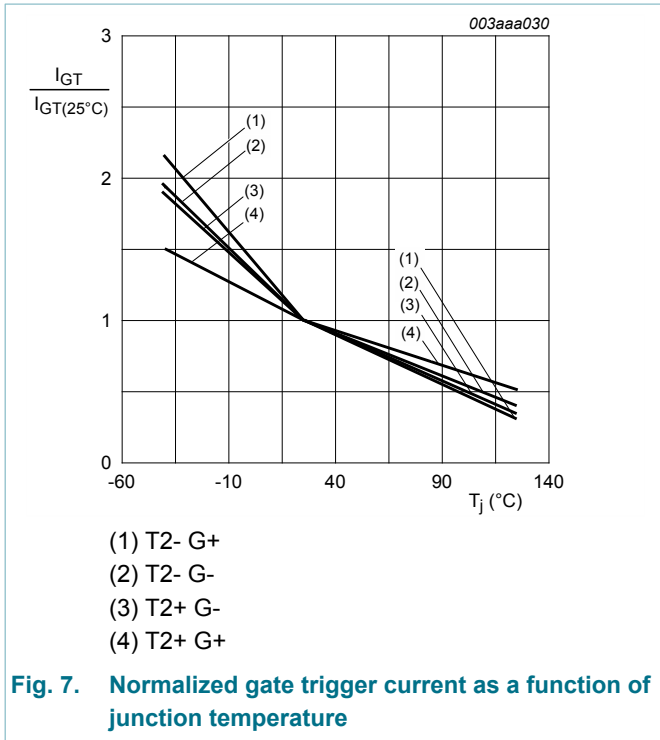


Fig. 7. Normalized gate trigger current as a function of junction temperature

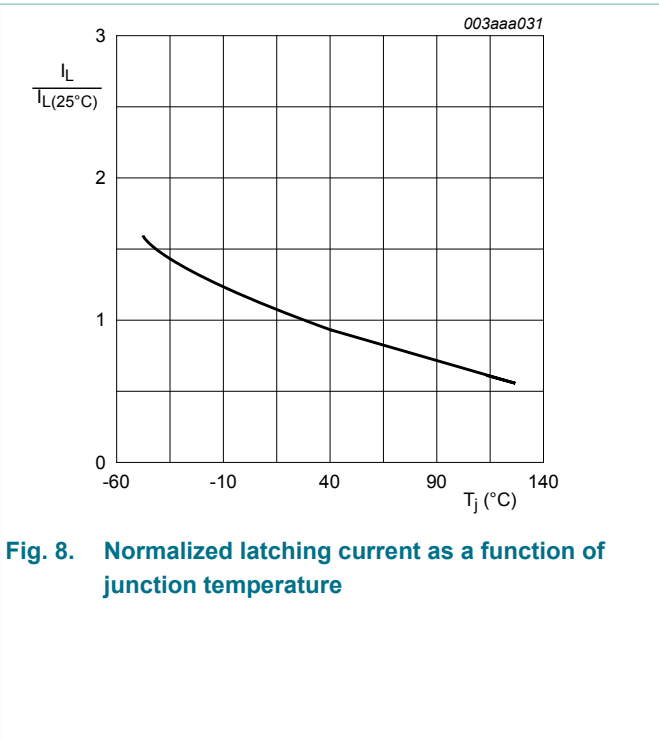


Fig. 8. Normalized latching current as a function of junction temperature

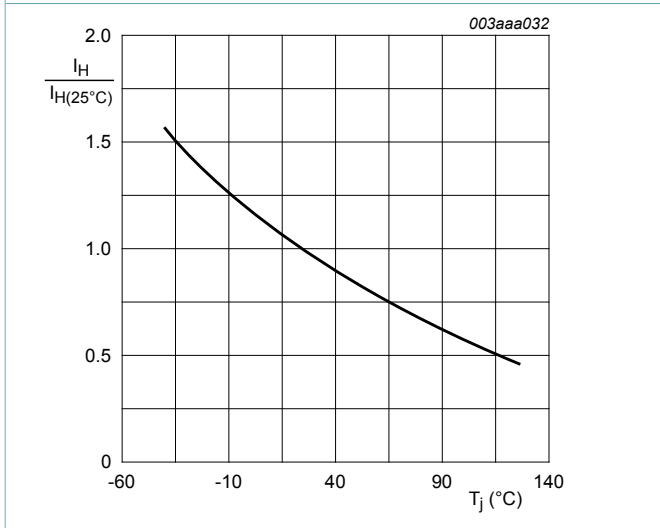
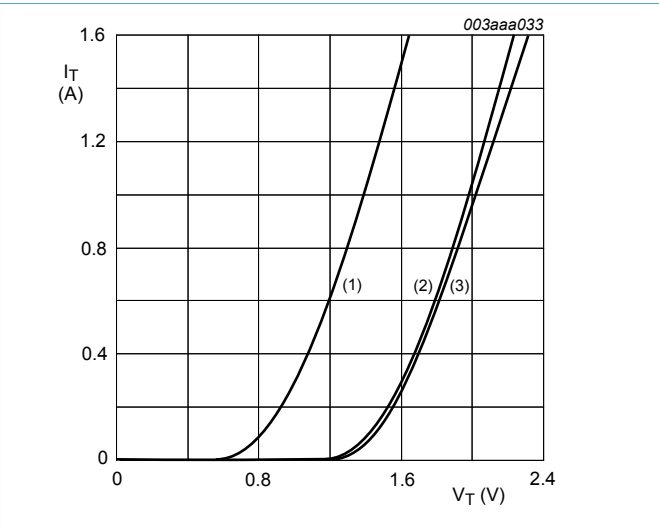


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.45\text{ V}$; $R_s = 0.1875\ \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

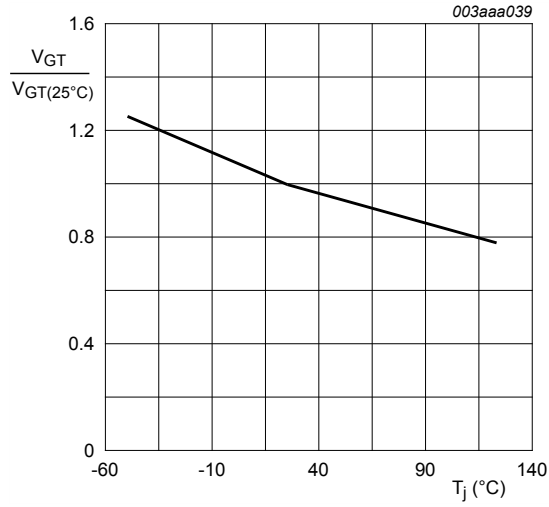


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

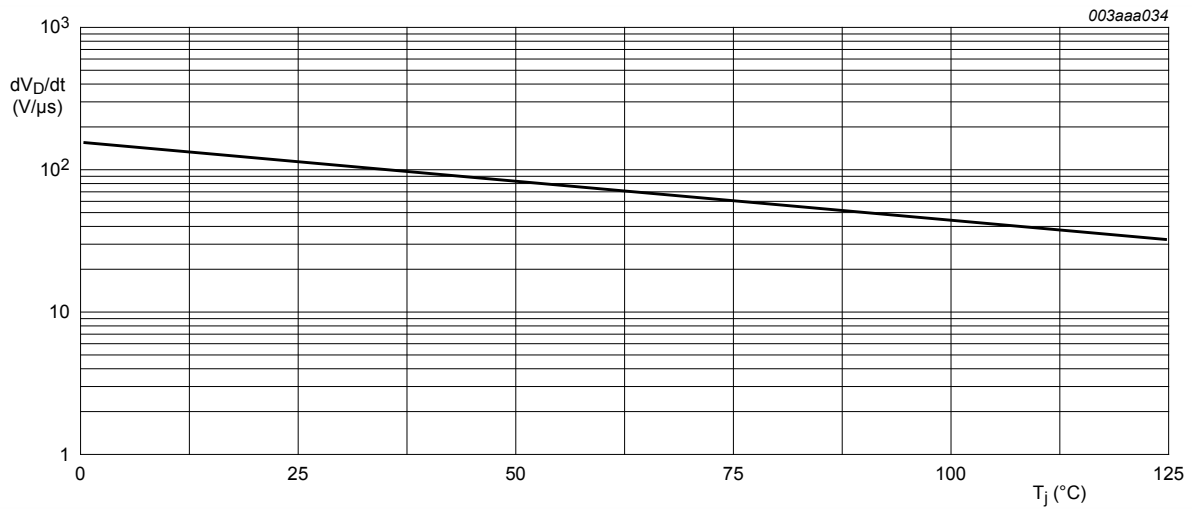


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

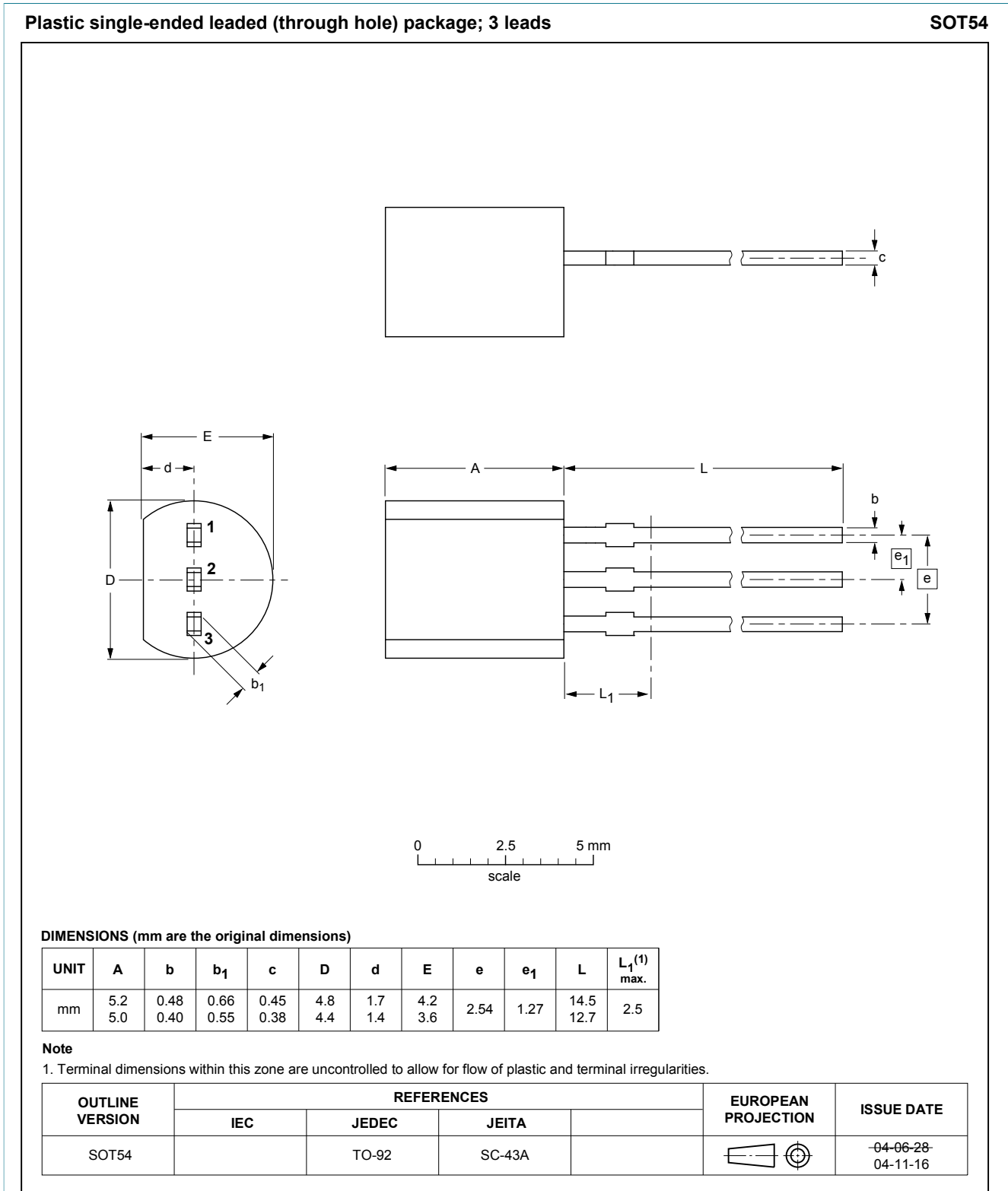


Fig. 13. Package outline TO-92 (SOT54)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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