QorIQ T1024 Reference Design Board User Guide

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freescale™

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Chapter 1
Overview

The T1024 Reference Design Board (T1024RDB) is a high-performance computing evaluation, development, and test platform supporting the QorIQ T1024 Power Architecture® processor. The T1024RDB is optimized to support the high-bandwidth DDR3L memory and a full complement of high-speed SerDes ports.

1.1 Related documentation

The table below lists and explains the additional documents that you can refer to, for more information about T1024RDB.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Useful references

Document	Description
QorIQ T1024, T1014 Data Sheet (T1024EC)	Provides specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations.
QorIQ T1024 Reference Manual (T1024RM)	Provides a detailed description on T1024 QorIQ multicore processor, and on some of its features, such as memory map, serial interfaces, power supply, chip features, and clock information. The T1024 QorIQ processor combines two 64-bit ISA Power Architecture® processor cores with high-performance datapath acceleration logic and network peripheral bus interfaces, required for networking and telecommunications. This chip can be used in applications, such as routers, switches, Internet access devices, firewall and other packet filtering processors, and general-purpose embedded computing. Its high-level integration offers significant performance benefits and greatly helps to simplify board design.
T1024 Product Brief (T1024PB)	Provides an overview of the T1024 features and its usage examples.
QorIQ T1024 Reference Design Board User Guide (T1024RDBPAUG)	Describes the features and operation of T1024 performance reference platform, which supports QorIQ Power Architecture® processors.

Table continues on the next page...

Table 1-1. Useful references (continued)

Document	Description
QorIQ Data Path Acceleration Architecture (DPAA) Reference Manual (DPAARM)	Describes the core set of DPAA functionality implemented in many QorIQ chips, and identifies those portions of the DPAA whose implementation varies from chip to chip. The QorIQ data path acceleration architecture (DPAA) provides the infrastructure to support simplified sharing of networking interfaces and accelerators by multiple CPU cores. These resources are abstracted into enqueue/dequeue operations by means of a common DPAA Queue Manager (QMan) driver.

1.2 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1-2. Acronyms and abbreviations

Usage	Description
COP	Common On-chip Processor
CPC	CoreNet Platform Cache
CPLD	Complex Programmable Logic Device
DIMM	Dual In-Line Memory Module
DIP	Dual In-Line Package
DIU	Display Interface Unit
DMA	Direct Memory Access
DPAA	Data Path Acceleration Architecture
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EC	Ethernet Controllers
EDC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Ethernet Management Interfaces
eMMC	embedded MultiMediaCard
eSDHC	enhanced Secure Digital Host Controller
eSPI	enhanced Serial Peripheral Interface
FET	Field Effect Transistor
HDLC	High-level Data Link Control
I2C	Inter-Integrated Circuit
IFC	Integrated Flash Controller
JTAG	Joint Test Action Group
MPIC	Multicore Programmable Interrupt Controller
PCIe/PEX	PCI Express
PLD	Programmable Logic Device
POR	Power On Reset

Table continues on the next page...

Table 1-2. Acronyms and abbreviations (continued)

Usage	Description
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDRAM	Synchronous Dynamic Random-Access Memory
SDHC	Secure Digital High Capacity
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
SYSCLK	System Clock
TDM	Time-Division Multiplexing
UART	Universal Asynchronous Receiver/Transmitter
VCC	Voltage for Circuit
VTT	Voltage for Terminal

1.3 T1024RDB board features

The T1024RDB board features are as follows:

- SerDes connections
  - XFI
  - PCI Express x1: supports Gen 1 and Gen 2
  - Two mini PCI Express x1
  - SGMII 2.5G
- DDR controller
  - Data rates of up to 1600 MHz are supported
  - One DDR3L DIMM of single, dual, or quad-rank types is supported
  - 1.35 V DDR power supply to all devices with automatic tracking of VTT
- IFC
  - NAND flash: 8-bit, asynchronous, up to 1 GB
  - NOR flash: 16-bit, non-multiplexed, up to 128 MB; NOR devices support 8 virtual banks
- Ethernet
  - Two on-board RGMII 10/100/1G Ethernet ports; PHY #0 remains powered up during deep sleep
  - One on-board XFI 10G EDC for 10GBase-T port
  - One on-board SGMII 2.5G Ethernet port

NOTE

Due to RCW limitations, SGMII 2.5G Ethernet port cannot work with XFI 10GBase-T port and MAC3 RGMII ethernet port in the same mode.

- CPLD
  - Manages system power and reset sequencing
  - Configures DUT, board, and clock with dynamic shmoo
  - Reset and interrupt monitor and control
  - General fault monitoring and logging
  - Sleep mode control
- Clocks
  - System and DDR clock or single differential clock
  - SerDes clocks: : Clocks are provided to all SerDes blocks and slots. Supported clock frequencies are:
    - 100 MHz
    - 125 MHz
    - 156.25 MHz
- USB
  - Supports two USB 2.0 ports with integrated PHYs
- SDHC
  - SDHC port connects directly to an adapter card slot
- SPI
  - On-board support of two different devices
- Other IO
  - Two serial ports with RJ45 interface
  - Two I2C ports

NOTE

For details on T1024 silicon features and block diagram, see *QorIQ T1024 Reference Manual*.

Chapter 2
Architecture

This chapter explains the architecture of T1024RDB:

- Processor
- Power
- Reset
- Clocks
- DDR
- SerDes port
- Ethernet controllers
- Ethernet Management Interface (EMI)
- I2C
- SPI interface
- IFC
- SDHC interface
- USB interface
- UART
- JTAG/COP port
- Connectors, Headers, Jumper, Push buttons, and LEDs
- Temperature
- DIP switch definition

2.1 Processor

The T1024RDB supports many features of the T1024 processor, as detailed in the following sections. The boards and supporting hardware are all identical, but the ability to use various features depends on the device installed.

2.2 Power

The power supply system of the T1024RDB systems uses power from a standard ATX PSU to provide power to the numerous processor, CPLD, and peripheral devices. To meet the required power specifications, the following goals guide the power supply architecture:

- Monolithic power supply for VCC (powering internal cores and platform logic).
- DUT-specific power rails are instrumented for current measurement.
- Automatic collection of voltage, current, and power is performed for critical supplies.
- Mounting holes of sufficient size are provided, to allow on-board supplies to be replaced by bench supplies.
- All power supplies can be sequenced as per hardware specifications.

The following table indicates the total power consumption of the T1024RDB.

The following figure shows the power supply architecture.

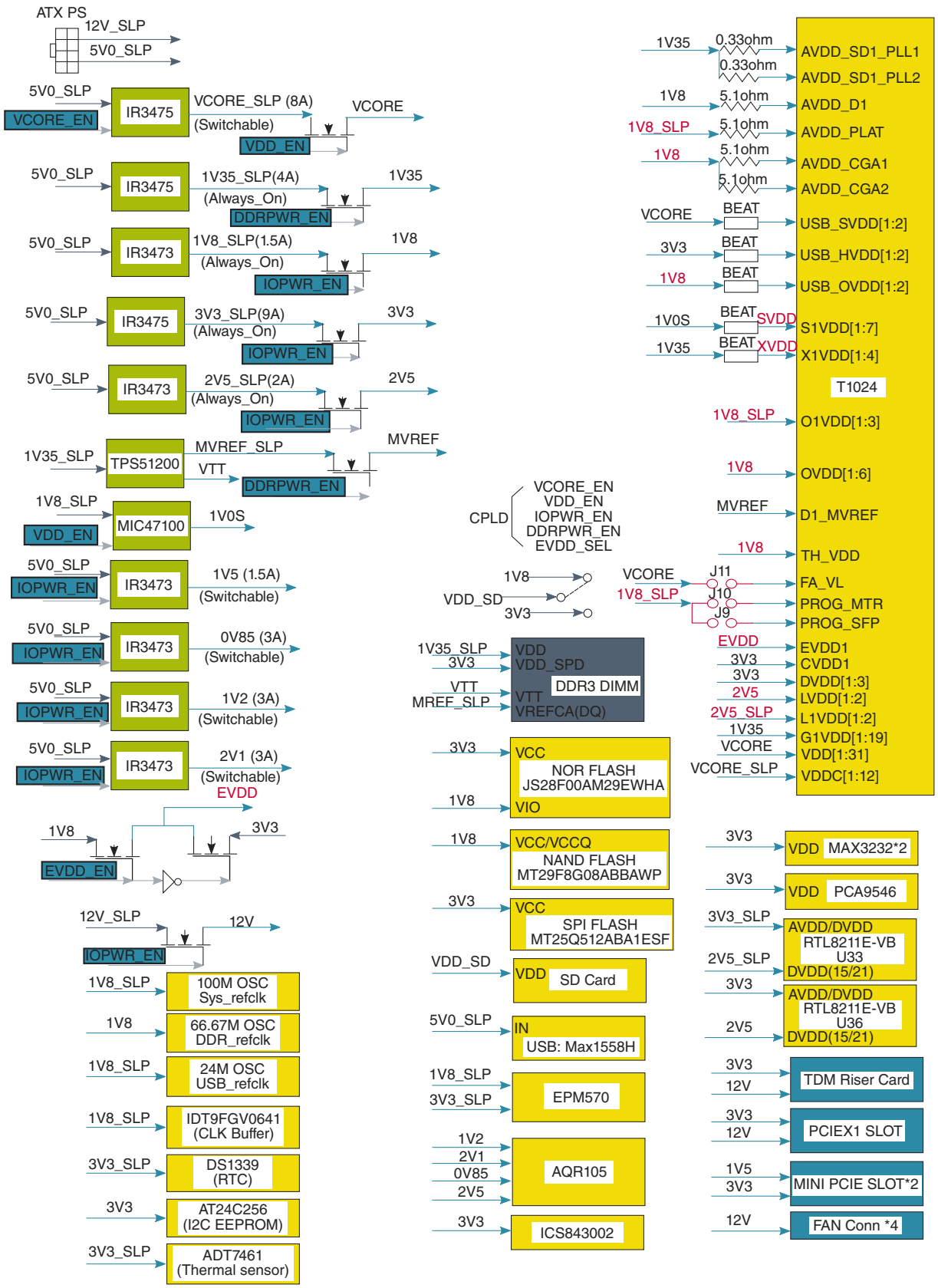

Figure 2-1. Power supply

NOTE

1. Set RGMII limits to LVDD=2.5 V.
2. Supply PROG_SFP/PROG_MTR with 1.8 V only during the secure boot fuse programming.

2.3 Deep sleep control

The T1024 processor has the ability to enter into the deep-sleep mode. Once the processor has readied itself for the deep-sleep mode, setting the CPLD register PWR_CTL[SLP] = 1 causes the power sequencer to begin an orderly shutdown of several power supplies, while others remain active.

Once ready, PWR_MSTAT[STATE] will indicate the system is asleep. However, the processor is already in the idle state, so this may not be needed by the system software.

Perform the following steps to send the T1024 processor to the deep-sleep mode:

- Prepare the CPLD to ignore the external signals. For example, some interrupt pins will power down, so the CPLD masks these pins from presenting valid interrupts.
- Prepare the DDR subsystem for self-refresh by forcing RST_MEM_B high, forcing the CKE# “clamp” FETs low.
- Gate the secondary powers to the DUT. Any power supply marked as “sleeps” in the power section diagrams are enable-disable, or can be gated.

Once the above steps are completed, the system enters into the deep-sleep mode. The system software has the timers or interrupt controllers programmed such that important events can wake the processor (which will be powered only by VDDC) and can decide if situations warrant returning to sleep, or activating full power.

2.4 Reset

The CPLD manages the reset signals to and from the T1024 processor and other devices on the T1024RDB. The following figure shows an overview of the reset architecture.

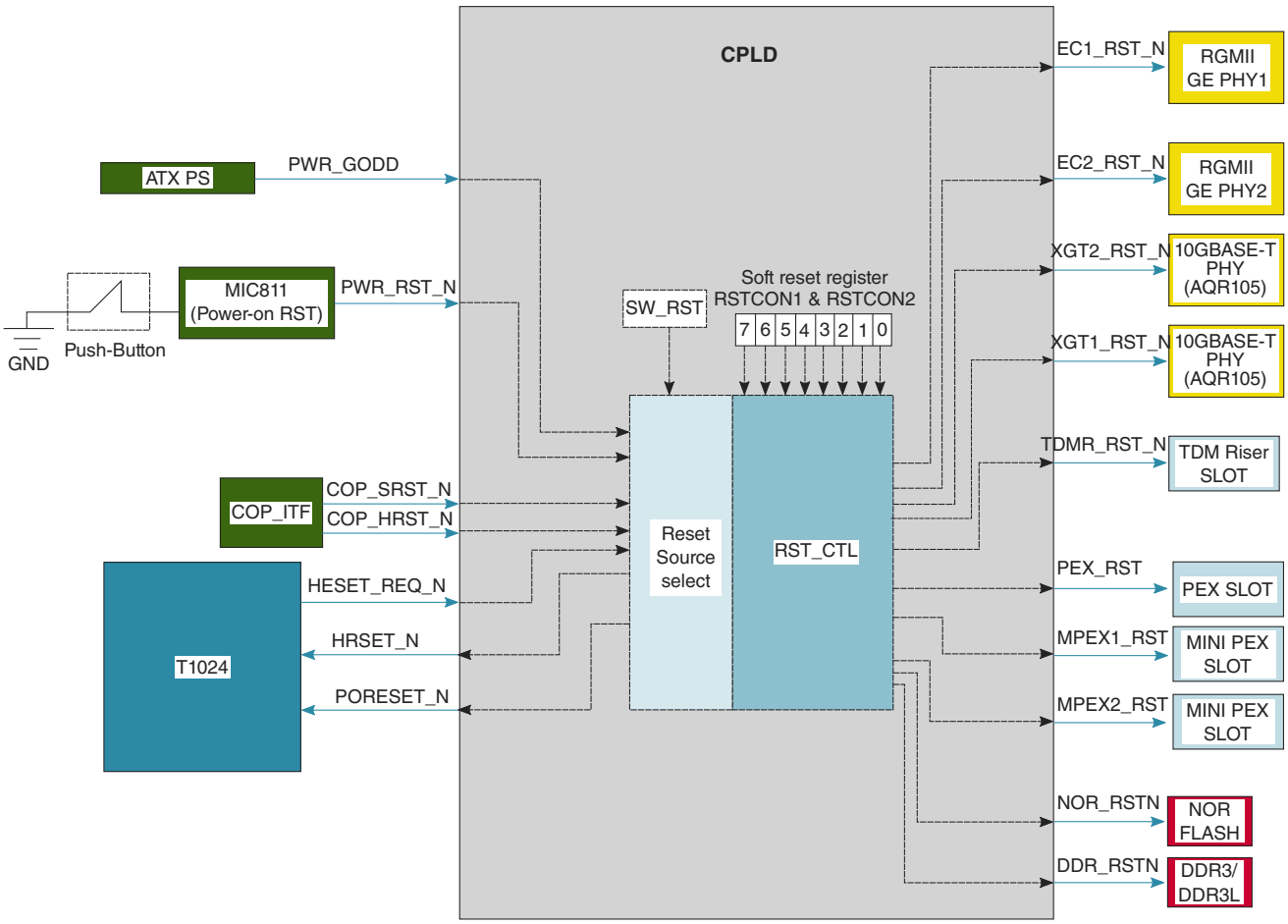

Figure 2-2. Reset architecture

2.5 Clocks

The clock circuitry provides the following clocks for the processor:

- SYSCLK
- DDRCLK (single-ended and differential)
- SerDes clocks
- Ethernet clocks
- USB clock

The architecture of the clock section is shown in the following figure.

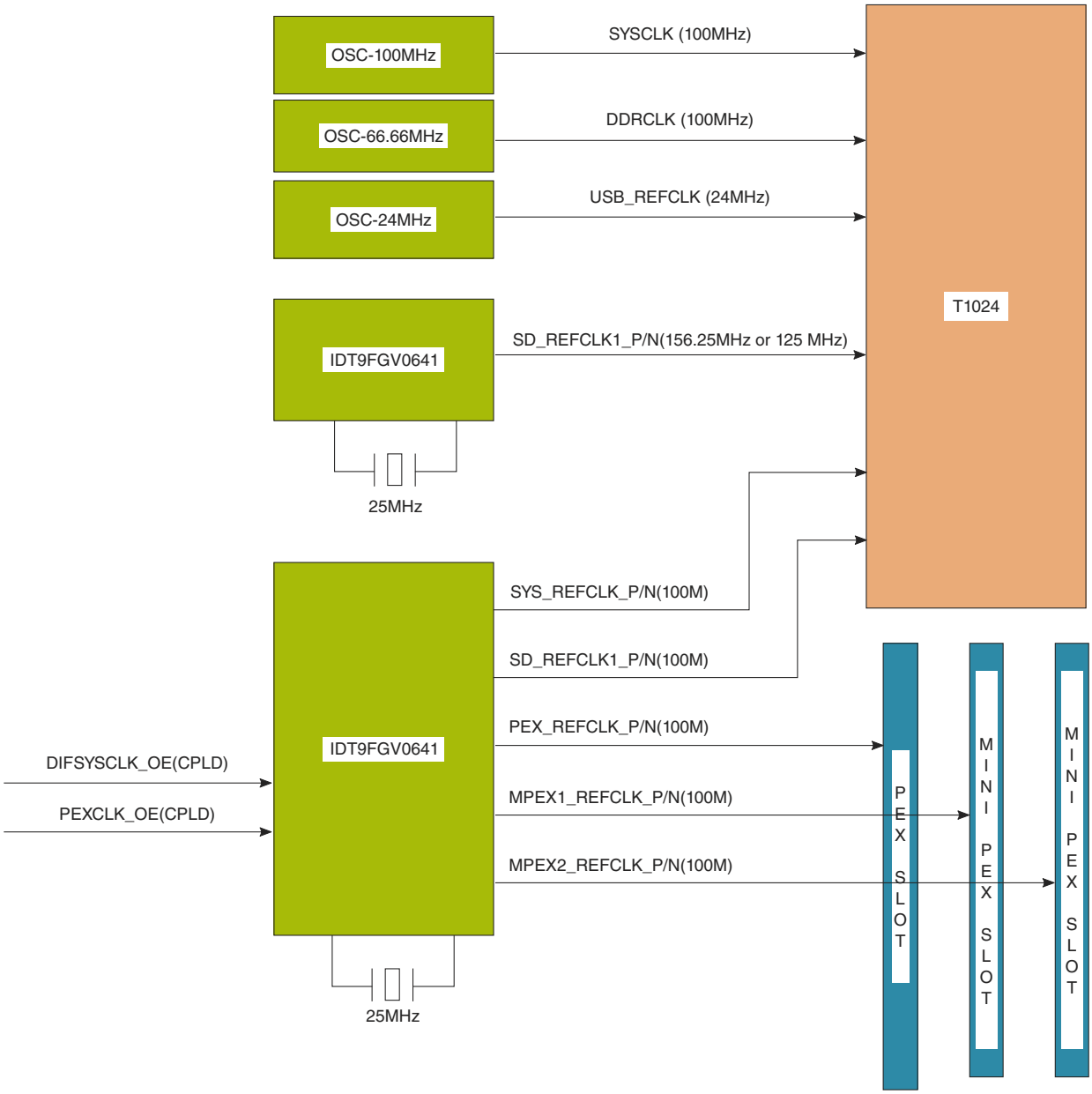

Figure 2-3. Clock architecture

2.6 DDR

The T1024RDB supports high-speed DRAM, with an unbuffered DDR3 (240-pin) socket (UDIMM) that features single-, dual-, and quad-rank support. The memory interface includes all the necessary termination and I/O power, and it is routed to achieve maximum performance by the memory bus, as shown in the following figure.

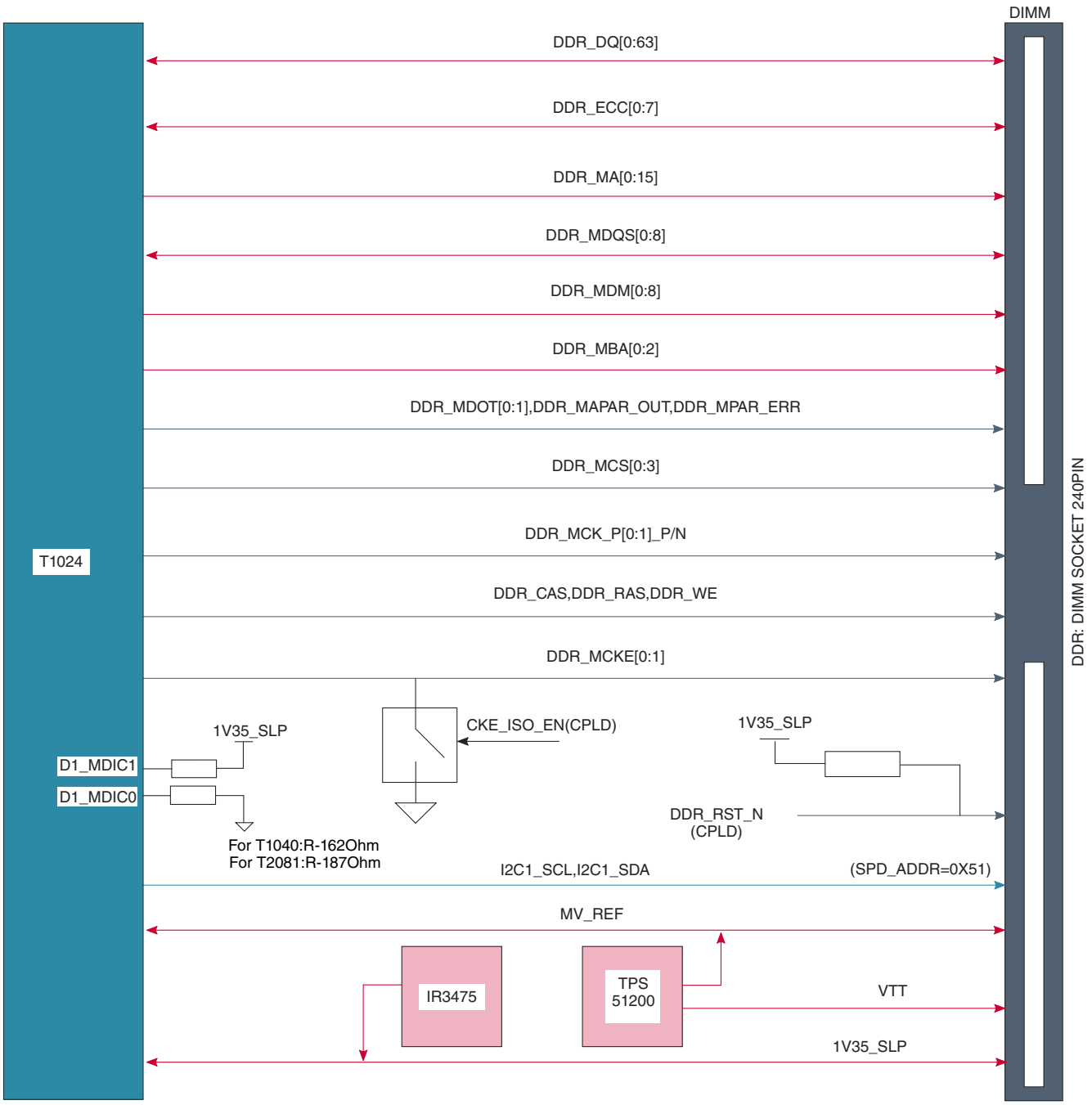

Figure 2-4. Memory interface

Although the platforms support all types, ranks, and speeds of DIMMs, but not all the combinations of these three exist in the memory market. Hence, the system is shipped with a “representative” DIMM, as noted in the below table. Other suitable memory DIMMs can be purchased and installed if needed. However, Freescale only supplies the device shown in the below table.

Table 2-1. Freescale supported DIMM

Platform	Type	Speeds	Ranks	DIMM
T1024RDB	DDR3L	1600 MT/s	Dual	Micron MT18KSF51272AZ-1G6K1 4GB, x72, CL=10

2.7 SerDes port

The T1024 SerDes block provides a four high-speed serial communication lanes, supporting a variety of protocols, including:

- XFI 1X 10.3125G bit/s
- PCI Express (PEX) Gen 1 1X 2.5 Gbit/s
- PCI Express (PEX) Gen 2 1X 5 Gbit/s
- SGMII 2.5G bit/s

An overview of the SerDes protocols supported on the T1024RDB is shown in Table 2-2.

Table 2-2. SerDes protocols

SRDS_PRTCL_S1	A	B	C	D	EC1	EC2	Per lane PLL mapping
0X095	XFI1(MAC1)	PEXc x1	PEXb x1	PEXa x1	RGMII (MAC4)	RGMII (MAC3)	1222
0X135	Aurora	2.5 SGMII (MAC3)	PEXb x1	PEXa x1	RGMII (MAC4)	N/A	1211

To comply with the T1024 application, some multiplexers are used to re-route and group the SerDes lanes as shown in the below figure.

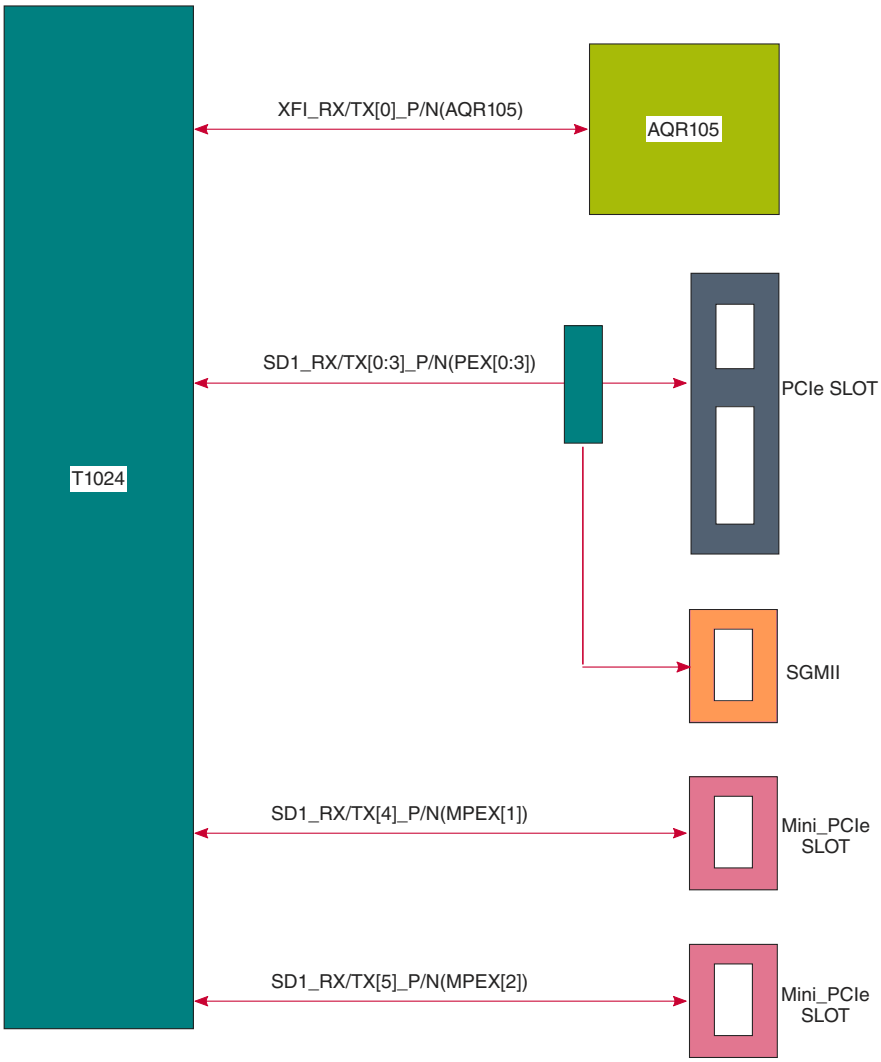

Figure 2-5. SerDes distribution of T1024RDB

2.7.1 PCI Express support

The T1024 processor supports evaluation of PCI Express using any standard PCI Express Gen 1 or Gen 2.

2.7.2 XFI support

The T1024 processor only supports the evaluation of the XFI protocol using Aquantia AQR105 single port 10GBase-T PHY. 10G data is carried over the XFI interface. The below figure shows the connectivity of the XFI interface.

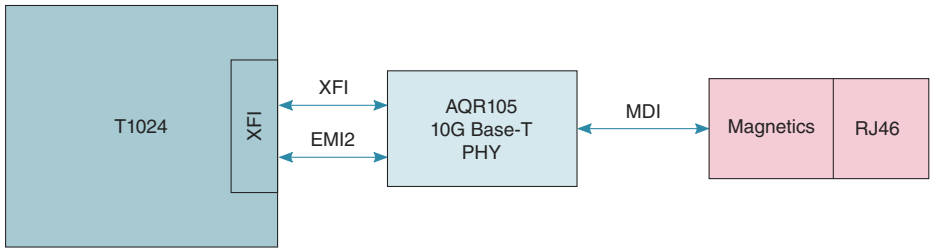

Figure 2-6. XFI interface

2.7.3 SGMII support

The T1024 processor supports evaluation of the 2.5G SGMII protocol for serialized Ethernet PHYs using Aquantia AQR105 PHY. Ethernet data is carried over the SGMII interface.

The below figure shows the connectivity of the SGMII interface.

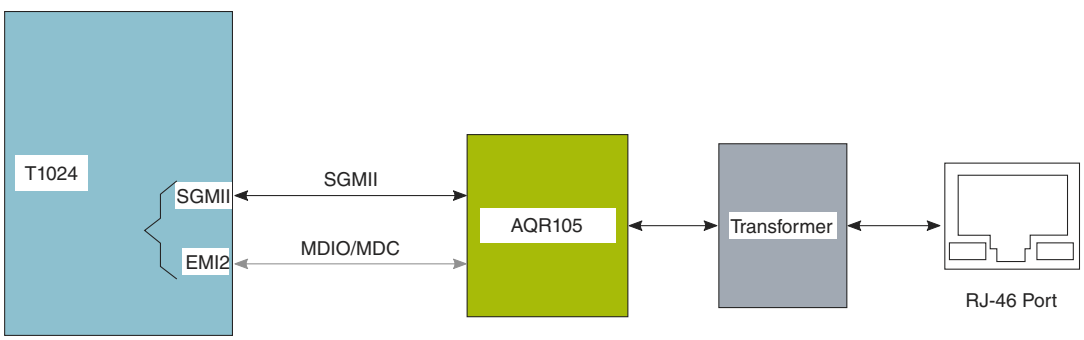

Figure 2-7. SGMII interface

2.8 Ethernet controllers

The T1024 processor supports two Ethernet Controllers (EC), which can connect to Ethernet PHYs using MII or RGMII protocols. On the T1024RDB, the EC1 and EC2 ports only operate in the RGMII mode. Both ports are connected to Realtek RTL8211 PHYs. The T1024RDB supports Energy Efficient Ethernet (EEE) on EC1 and sleep mode on EC2.

The below figure shows the connectivity of the EC1/EC2 interface.

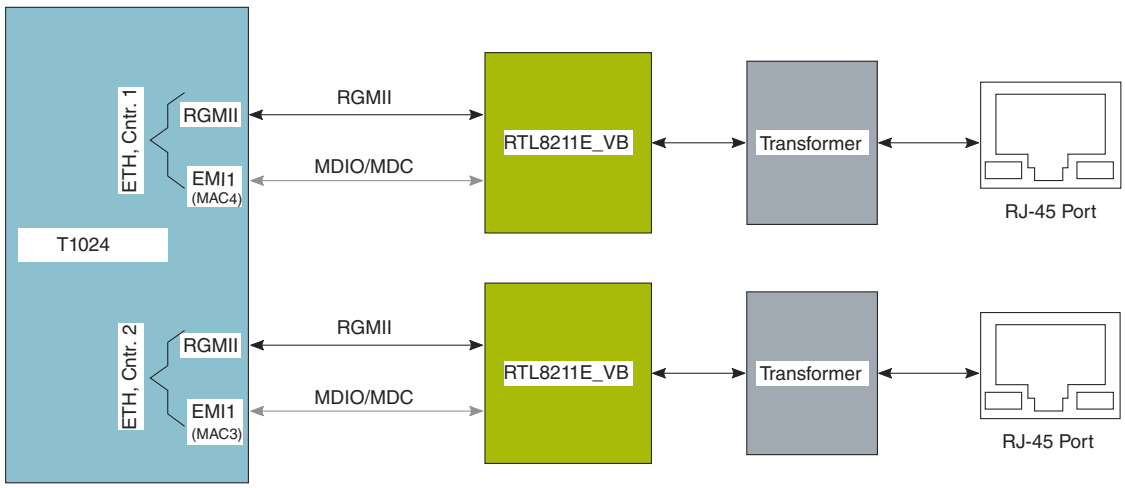

Figure 2-8. EC1/EC2 interface connectivity

2.9 Ethernet Management Interface (EMI)

The T1024 processor has two Ethernet Management Interfaces (EMI), EMI1 and EMI2. EMI2 is only used with 10G Base-T PHY and 2.5G SGMII PHY, which uses 1.2 V pull-up. EMI1 is used with RGMII PHYs. There are two working modes in the T1024RDB-PC. The following tables represents the configurations for 10GBase-T and 2.5G SGMII working modes:

Working mode	Image in Flash	SW3 [1:8] On = 0	SerDes Protocal	ETH0	ETH1	ETH2	ETH3	PCIe Slot
10GBase-T	Bank 0 (Default)	00100001	0x95	1G/100M	1G/100M	10G/ 2.5G/1G	Disable	Enable
2.5G SGMII	Bank4	01101001	0x135	1G/100M	Disable	Disable	2.5G	Disable

Working mode	SerDes Protocal	Lane A	Lane B	Lane C	Lane D	EC1	EC2
10GBase-T	0x95	XFI (MAC1)	PEXc	PEXb	PEXa	MAC4	MAC3
2.5G SGMII	0x135	Aurora	SGMII (MAC3)	PEXb	PEXa	MAC4	N/A

The below figure shows the EMI hardware block diagram.

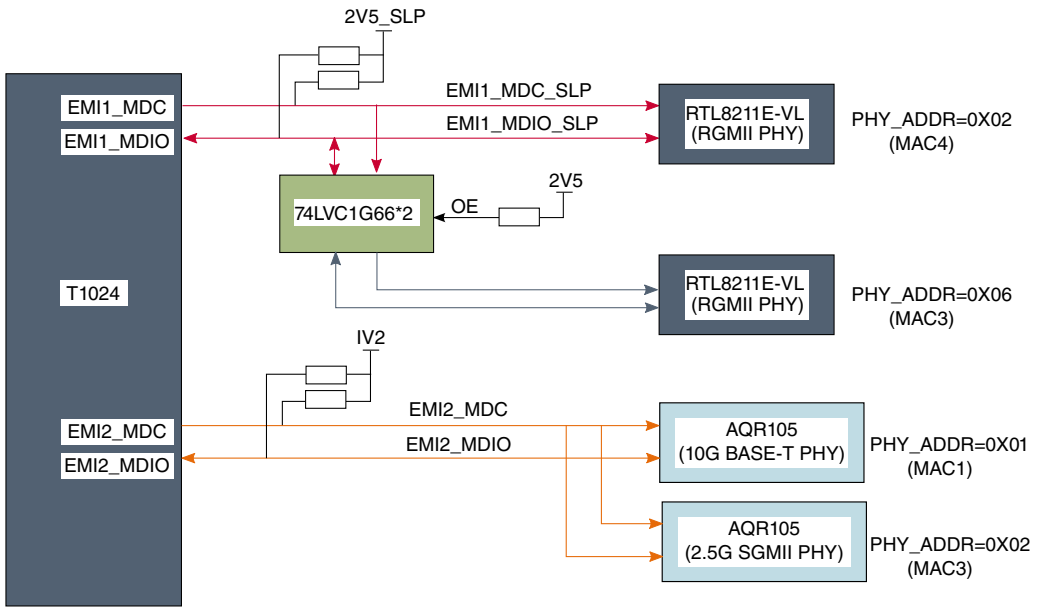

Figure 2-9. EMI hardware block

2.10 I2C

The T1024 devices supports up to four I2C buses, to make the I2C resources equally available to both local and remote systems. The T1024RDB uses I2C1 port to access on-board devices, such as DDR3 DIMM, thermal sensor (ADT7461), EEPROM, RTC, and clock PLL. The I2C2 bus uses multiplexers to partition the I2C bus into several channels. Two mini PCIe slots use channels 0 and 1, and the PCIe slot uses channel 3.

The following figure shows the I2C subsystem.

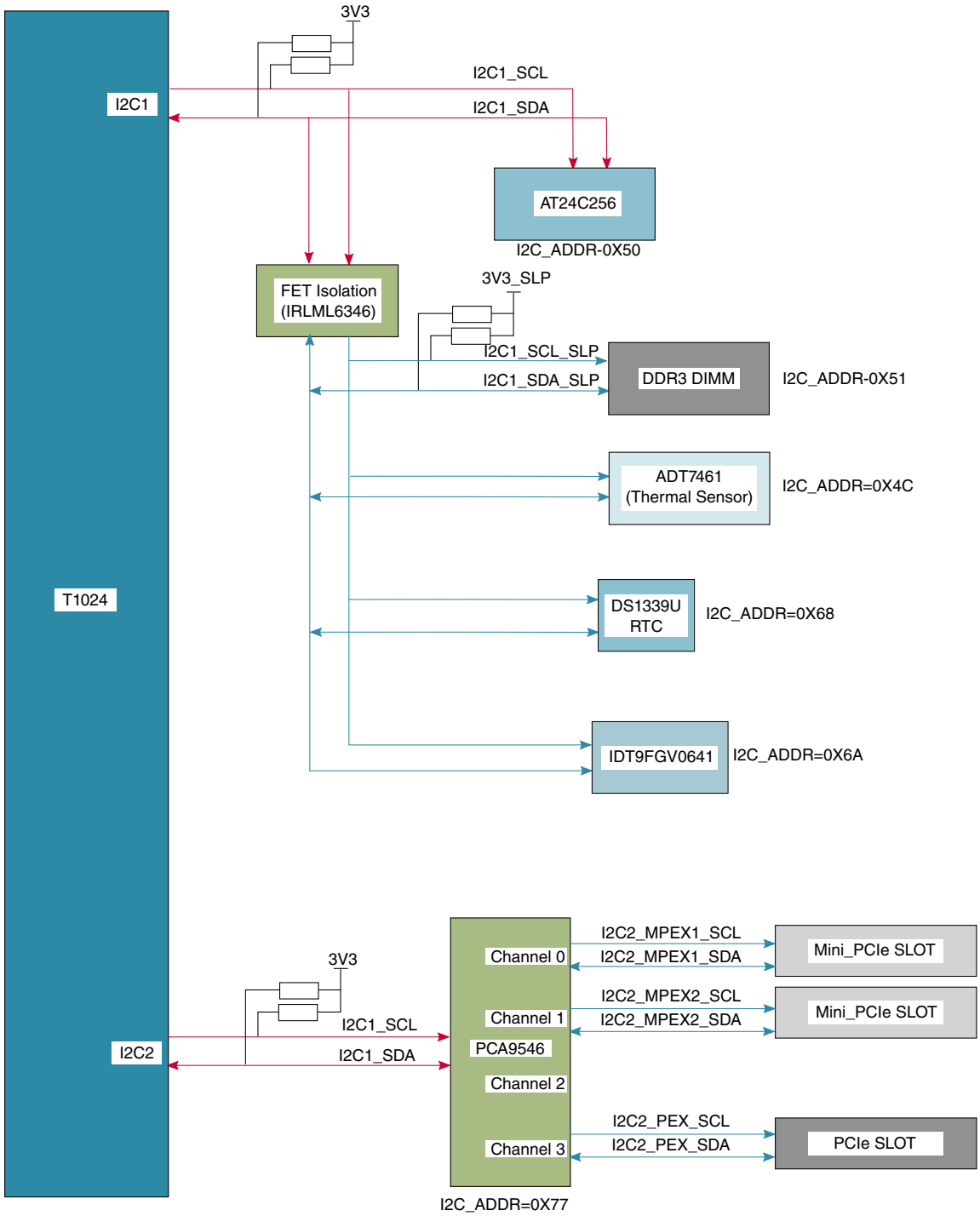

Figure 2-10. I2C subsystem

2.11 SPI interface

The T1024 Serial Peripheral Interface (SPI) pins are used for the following purposes:

- On-board SPI device accessing various SPI memory devices
- Off-board TDM riser card plug-in on J43 slot

SPI_CS0 is used to access a SPI memory device, with the remaining chip selects used to select additional on-board SPI devices, and a TDM device present on the TDM riser card. The below figure shows the overall connections of the SPI portion.

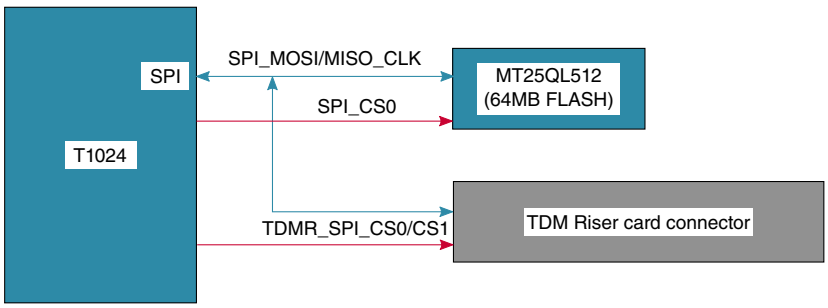

Figure 2-11. SPI interface

2.12 IFC

The T1024 Integrated Flash Controller (IFC) supports 32-bit addressing and 8- or 16-bit data widths for a variety of devices to effectively manage all the resources with maximum performance and flexibility. The below figure shows an overview of the IFC bus.

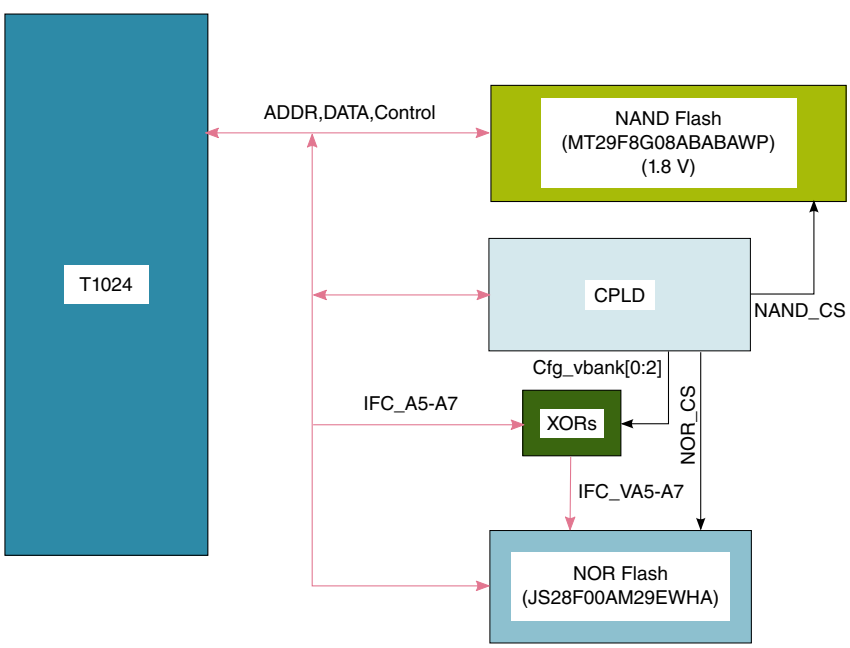

Figure 2-12. IFC bus

2.12.1 Virtual banks

The virtual bank feature is available when the NOR flash is connected to IFC_CS0_N. In that case, the value of VBANK[0:2] will be driven into three XOR gates, which toggle the MSB's of the NOR address, as shown in the below figure.

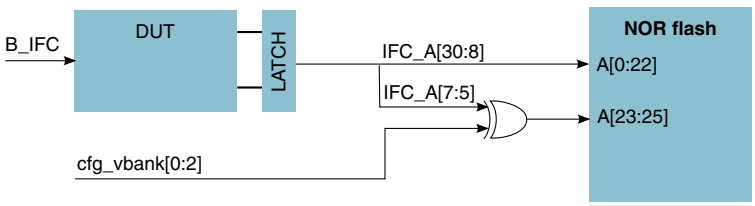

Figure 2-13. Virtual bank interface

When VBANK[0:2]=000, the IFC_A[7:5] is not altered, and the NOR flash behaves normally. If VBANK[0:2]=100, the LB_A[5] is toggled and effectively swaps the top and bottom halves of the NOR flash. If program "A" was stored in the bottom half and program "B" in the top half then, while selecting different VBANK settings, “A” and “B” will get their VBANKs changed as given in the below table.

Table 2-3. Virtual bank settings

NOR zones (1/8 of 128 MB)	VBANK							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
A	A	B	C	D	E	F	G	H
B	B	A	D	C	F	E	H	G
C	C	D	A	B	G	H	E	F
D	D	C	B	A	H	G	F	E
E	E	F	G	H	A	B	C	D
F	F	E	H	G	B	A	D	C
G	G	H	E	F	C	D	A	B
H	H	G	F	E	D	C	B	A

NOTE

In the above table, the NOR flash has been partitioned into eight 16 MB zones, which can be arranged under the control of VBANK.

2.13 SDHC interface

The enhanced SD Host Controller (eSDHC) provides an interface between host system and SD/MMC cards. The Secure Digital (SD) card is specifically designed to meet the security, capacity, performance, and environmental requirements, inherent in emerging audio and video consumer electronic devices. Booting from eSDHC interface is supported using the processor's on-chip ROM.

On the T1024RDB, a single connector is used for both SD and MMC memory cards, as shown in the below figure.

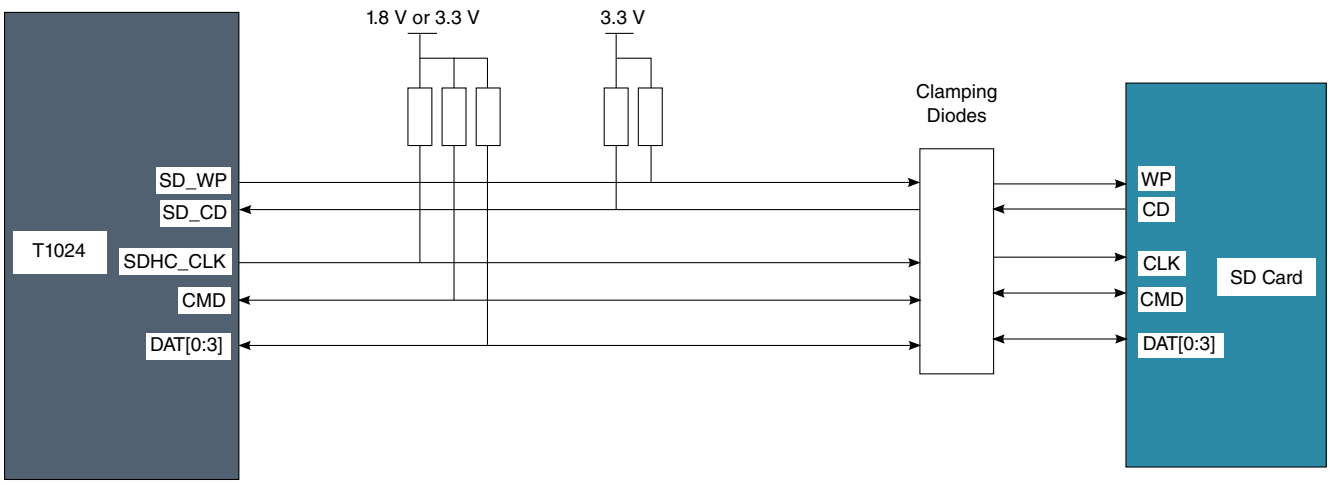

Figure 2-14. SDHC interface

2.14 USB interface

The T1024RDB systems have two integrated USB 2.0 controllers (USB1 and USB2), that allow direct connection to USB ports with appropriate protection circuitry and power supplies.

The board features are:

- High-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations
- Host mode
- Dual-stacked Type A connection

Each USB ports are connected to a standard Type A connector for compatibility with most USB peripherals.

Power to the USB ports is provided by a MAX1558H switch, which supplies 5 V at up to 1 A per port. The power enable and power-fault-detect pins are directly connected to the T1024 processor for individual port management.

The below figure shows how the USB connectivity is implemented on the T1024RDB.

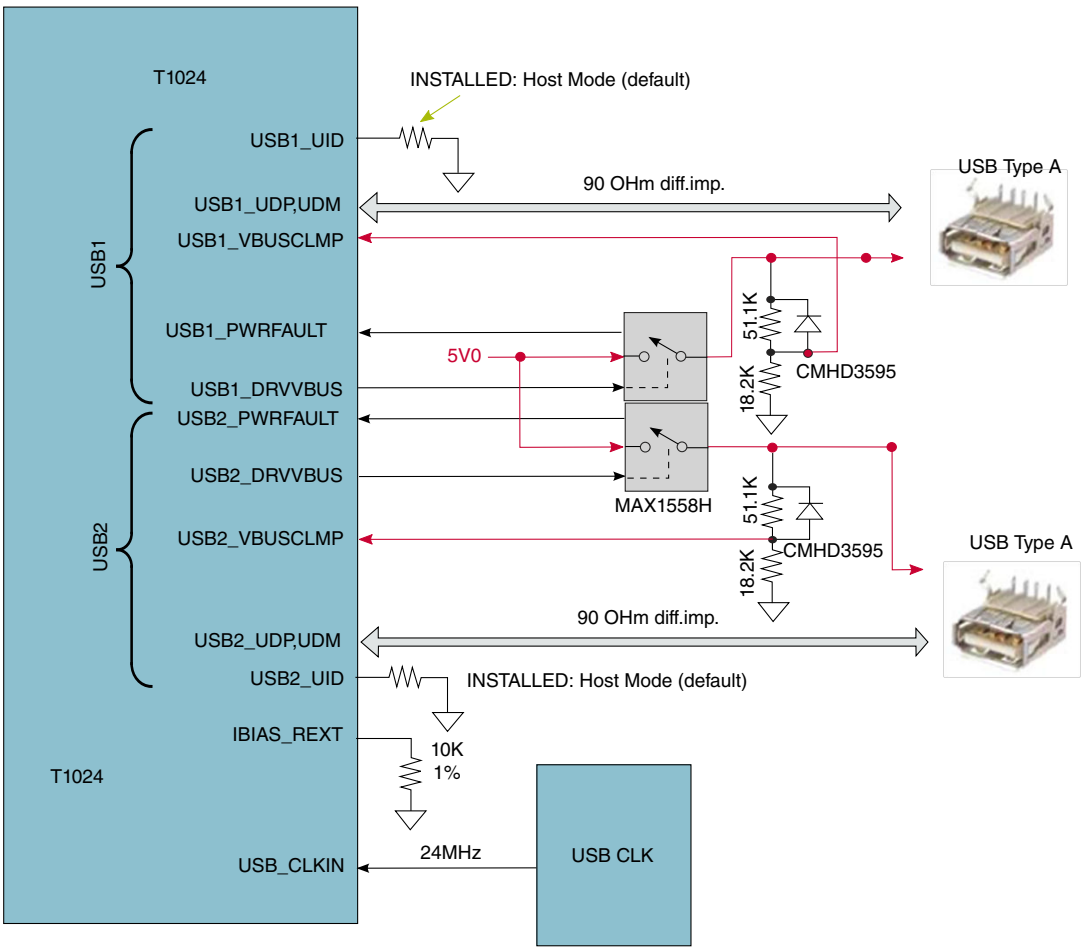

Figure 2-15. USB connectivity implementation

2.15 UART

The T1024 processor has two UART controllers, which provides a RS-232 standard interconnection between the board and an external host. The serial connection is typically configured to run at 11.5 Kbit/s.

Each UART supports:

- Full-duplex operation
- Software-programmable baud generators
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions

- Software-selectable serial interface data format that includes:
  - Data length
  - Parity
  - 1/1.5/2 STOP bit
  - Baud rate
- Overrun, parity, and framing error detection

The UART ports are routed to the RJ45 connectors, as shown in the below figure.

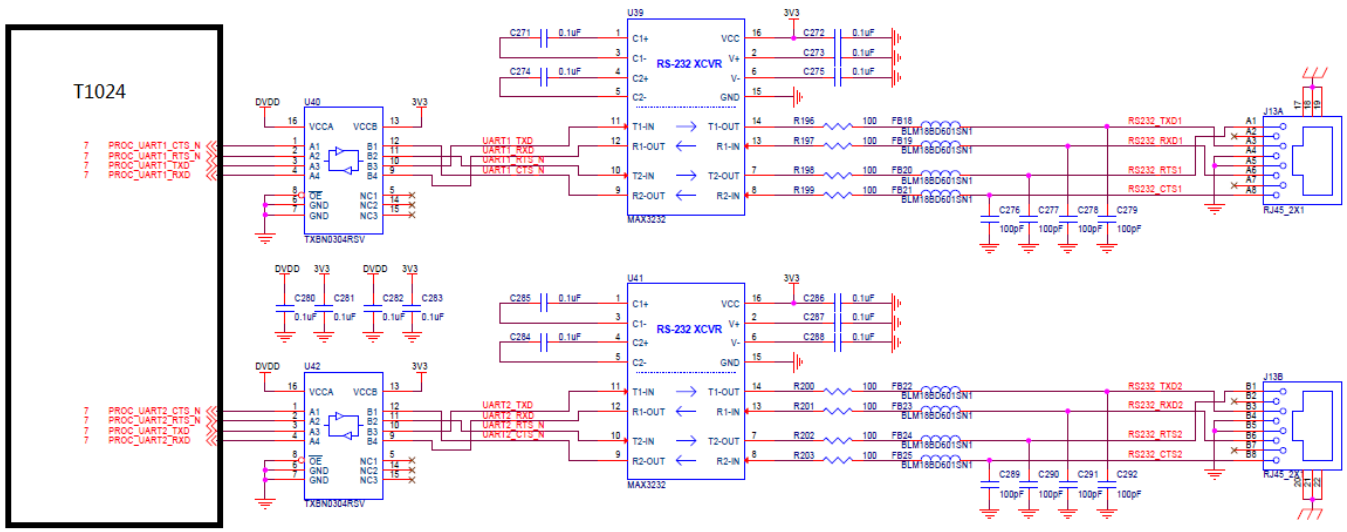

Figure 2-16. UART ports, routed to RJ45 connectors

The below table shows the connection settings for the UART RJ45 connector to the DB9 female cable connection.

Table 2-4. RJ45 to DB9 connection settings

RJ45 pin number	RS-232 signal	DB9 female pin number
1	RTS	8
2	NC	
3	TXD	2
4	GND	
5	GND	5
6	RXD	3
7	NC	
8	CTS	7

Before powering up the T1024RDB card, configure the serial port of the attached computer with the following values:

- Data rate: 115200 bit/s
- Number of data bits: 8

- Parity: None
- Number of stop bits: 1
- Flow control: Hardware/None

2.16 TDM riser card interface

The T1024RDB can support TDM riser card. The below figure shows the TDM riser card connector.

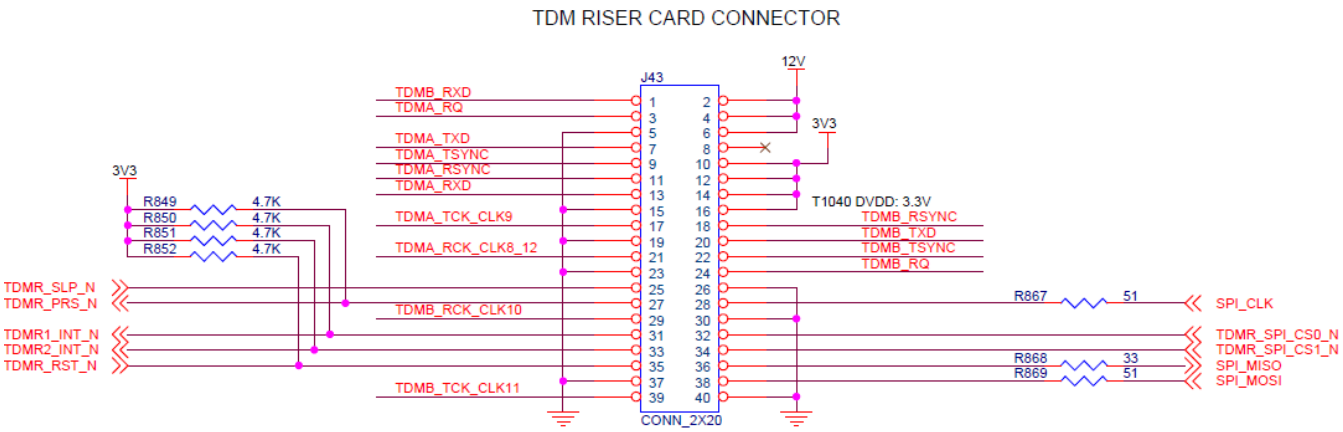

Figure 2-17. TDM Riser card connector

2.17 JTAG/COP port

The common on-chip processor (COP) is a part of the T1024 processor's JTAG module, and it is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, or RS-232. A setup using a USB port emulator is shown in the below figure.

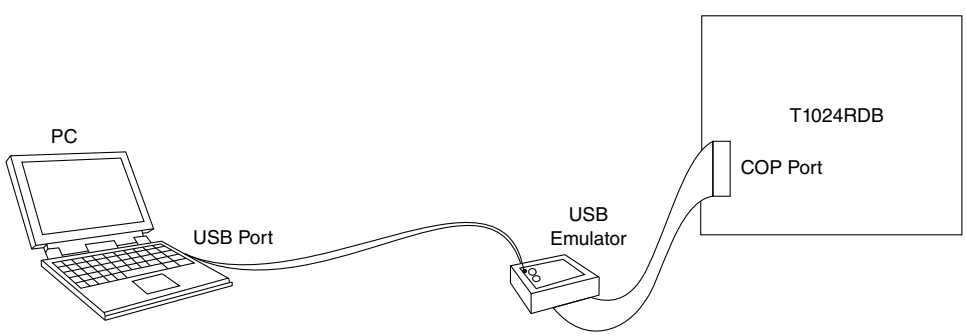

Figure 2-18. USB port emulator setup

The 16-pin generic header connector carries the COP/JTAG signals and additional signals for system debugging. The pin-out of this connector is shown in the below figure.

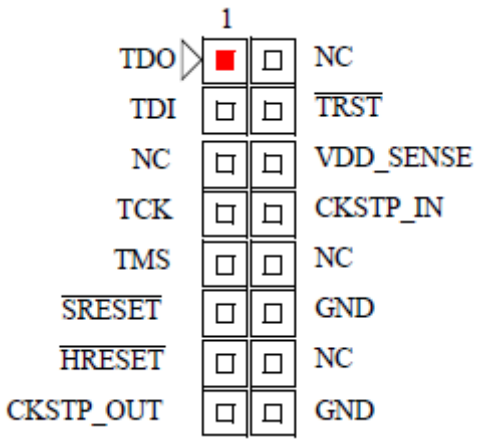

Figure 2-19. 16-pin connector

The table below displays the connections made from T1024RDB COP connector.

Table 2-5. Connections made from the T1024RDB COP connector

Pin number	Signal name	Connection
1	TDO	Connected directly between the processor and JTAG/COP connector.
2	NC	Not connected.
3	TDI	Connected directly between the processor and JTAG/COP connector.
4	TRST	Routed to the RESET PLD. TRST to the processor is generated from the PLD.
5	NC	Not connected.
6	VDD_SENSE	Pulled to 3.3 V using a 10 Ohm resistor.
7	TCK	Connected directly between the processor and JTAG/COP connector.
8	CKSTP_IN	Connected directly between the processor and JTAG/COP connector.
9	TMS	Connected directly between the processor and JTAG/COP connector.
10	NC	Not connected.
11	SRESET	Routed to the RESET PLD. SRESET to the processor is generated from the PLD.
12	GND	Connected to ground.
13	HRESET	Routed to the RESET PLD. HRESET to the processor is generated from the PLD.
14	NC	Not connected.
15	CKSTP_OUT	Connected directly between the processor and JTAG/COP connector.
16	GND	Connected to ground.

2.18 Connectors, Headers, Jumper, Push buttons, and LEDs

This section explains:

- Connectors

- Headers
- Jumpers
- Push buttons
- LEDs

2.18.1 Connectors

The below table lists the various connectors on the T1024RDB platform.

Table 2-6. Connectors on the T2080RDB-PB platform

Reference designators	Used for	Notes
J37	ATX power	
J2	SD card	
J18	PCIe x1 card	Intended use is for PCIe cards that are 25 W or less
J19, J20	Mini PCIe cards	
J43	TDM riser card	
J14 (two ports)	Ethernet ports	RGMII -> Copper
J50	10G Ethernet ports	10G Base-T Ethernet port
J41 (two ports)	Dual Type A USB	
J13 (two ports)	UART	
J49	Battery holder	
J1	UDIMM	
J34	CPU fan	
J33, J44-J46	Shelf fan	
J47	Remote reset switch	
J48	Remote power switch	

2.18.2 Headers

The below table lists the various headers on the T1024RDB platform.

Table 2-7. Headers on T1024RDB platform

Reference designators	Used for	Notes
J26	Altera header	Used for programming the Altera CPLD devices
J3	COP/JTAG	Used for debugging the T1024 devices

2.18.3 Jumpers

The below table describes how the Jumpers are used on the T1024RDB platform.

Table 2-8. Jumpers on T1024RDB platform

Reference designator	Description	Status 1	Status 2
J9	PROG_SFP selection	Mounted: Fuse programming	Un-mounted: Normally operate
J10	PROG_MTR selection	Mounted: Fuse programming	Un-mounted: Normally operate
J11	FA_VAL selection	-	Un-mounted: Normally operate
J35	FAN_FULL_SPEED	1-2: For full speed on fan	No: Fan can be adjusted by CPLD
J53	VDD_SD	1-2: VDD_SD uses 3.3 V	2-3: VDD_SD uses 1.8 V

2.18.4 Push buttons

The following table describes how the push buttons are used on the T1024RDB platform.

Table 2-9. Push buttons on T1024RDB platform

Reference designators	Used for	Notes
SW4	Reset	Used for resetting the whole board
SW5	Power on/off	Used for turning the power on or off on the board

2.18.5 LEDs

The below table lists all the LEDs on the T1024RDB front plate.

Table 2-10. LEDs on the T1024RDB front plate

LEDs	Used for	Controlled by
D44	Power on	+3.3 V rail
D43	Status	CPLD

2.19 Temperature

The T1024 processor has a thermal diode attached to the die for direct temperature measurement. The diode pins are connected to a two-channel ADT7461 thermal monitor, which allows direct reading of the temperature of the die and it is accurate to ±1 °C. The second channel of the ADT7461 measures the ambient (board) temperature.

The ADT7461 temperature warning and alarm signals are connected to the CPLD for monitoring. The CPLD uses these signals to adjust CPU fan speed and protect the CPU from over-temperature failure.

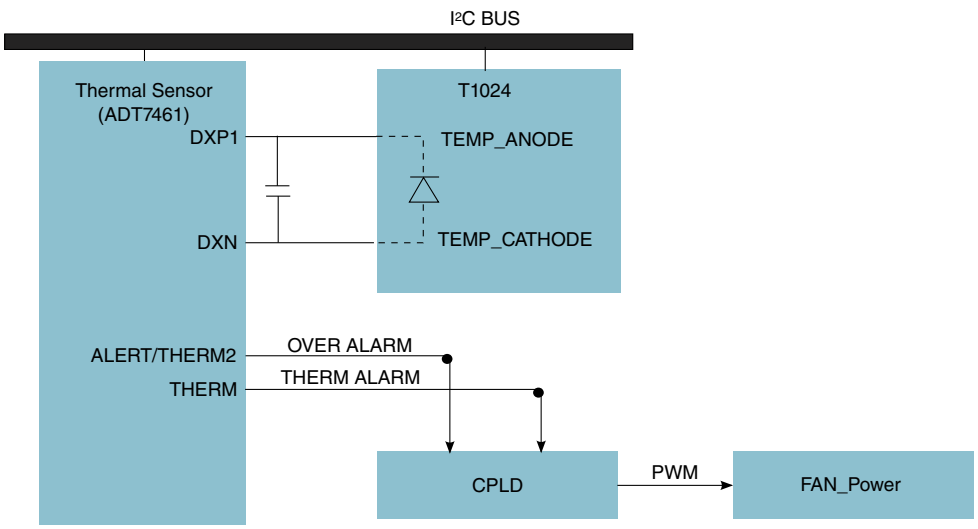

Figure 2-20. Temperature

2.20 DIP switch definition

The T1024RDB board has user selectable switches, for evaluating different boot configurations and other special configurations for this device.

This configuration allows either the switch or the CPLD register to set the POR pin. The CPLD register allows software to override the pin remotely when the board is in the board farm.

To use the CPLD override option, software sets an override bit, which allows the CPLD to override the switch setting during power on reset.

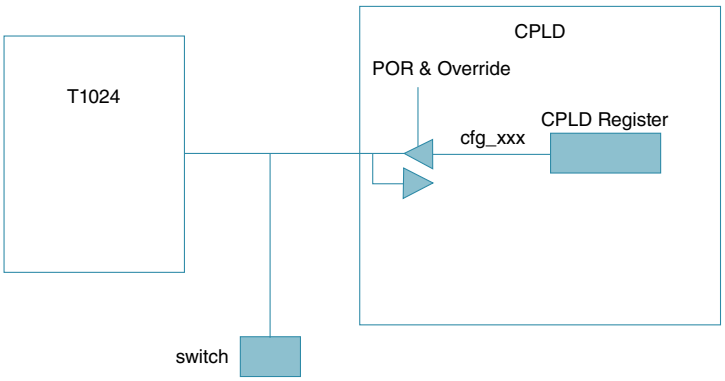

Figure 2-21. DIP switch definition

The table below shows how POR configuration is done through switches.

Table 2-11. POR configuration through switches

Switch	Signal name	Pin name	Signal meaning	Setting
SW1[1:8]	cfg_rcw_src[0:7]	IFC_AD[8:15]	Reset configuration word source	For details, see *T1024 QorIQ Integrated Multicore Communications Processor Data Sheet*.
SW2[1]	cfg_rcw_src[8]	IFC_CLE	Reset configuration word source	For details, see *T1024 QorIQ Integrated Multicore Communications Processor Data Sheet*.
SW2[2]	cfg_ifc_te	IFC_TE	IFC external transceiver enable polarity select	0: IFC drives logic 1 for TE assertion 1: IFC drives logic 0 for TE assertion
SW2[3]	cfg_pll_config_sel_b	IFC_A18	Reserved	Reserved
SW2[4]	cfg_por_ainit	IFC_A19	Reserved	Reserved
SW2[5:6]	cfg_svr[0:1]	IFC_A[16:17]	Reserved	Reserved
SW2[7]	cfg_dram_type	IFC_A21	DRAM type selection	Reserved
SW2[8]	cfg_rsp_dis	IFC_AVD	Reserved	Reserved
SW3[1]	cfg_eng_use0	IFC_WE0	Sys_clock selection	Reserved
SW3[2]	cfg_eng_use1	IFC_OE_N		ON (0): Choose 10G working mode OFF (1): Choose 2.5G working mode
SW3[3]	cfg_eng_use2	IFC_WP_N		Reserved
SW3[4]	BOOT_FLASH_SEL	-	Boot flash selection	0: NOR flash connects to CS0, NAND flash connects to CS1 1:NOR flash connects to CS1, NAND flash connects to CS0
SW3[5:7]	CFG_VBANK[0:2]	-	NOR flash bank select	000: boot from VBANK0 with RCW 0x095 for 10G XFI mode

Table continues on the next page...

Table 2-11. POR configuration through switches (continued)

Switch	Signal name	Pin name	Signal meaning	Setting
				100: boot from VBANK4 with RCW 0x135 for 2.5G SGMII mode See note[1]
SW3[8]	TEST_SEL_N	TEST_SEL_B	-	

1. SW3[5:7] can be used to change the starting address for the memory banks. The NOR flash memory is divided into eight memory banks with 16 MB size each. Eight different U-Boot images can be programmed into each memory bank. When NOR flash is selected as boot flash, different U-Boot images can be selected to boot up the board, by setting SW3[5:7].

NOTE

For other DIP switch settings and definitions, see *T1024 QorIQ Integrated Multicore Communications Processor Data Sheet*.

Chapter 3
CPLD Specification

This section explains the CPLD registers.

3.1 CPLD Memory Map/Register Definition

The table below shows the memory map for CPLD registers.

CPLD memory map

Offset address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Chip ID1 Register (CPLD_CHIPID1)	8	R	55h	3.1.1/36
1	Chip ID2 Register (CPLD_CHIPID2)	8	R	AAh	3.1.2/36
2	Hardware Version Register (CPLD_HWVER)	8	R	See section	3.1.3/36
3	Software Version Register (CPLD_SWVER)	8	R	See section	3.1.4/37
10	Reset Control Register (CPLD_RSTCON)	8	w1c	00h	3.1.5/37
11	Reset Control Register (CPLD_RSTCON2)	8	w1c	00h	3.1.6/38
12	Interrupt Status Register (CPLD_INTSR)	8	R	00h	3.1.7/39
13	Flash Control and Status Register (CPLD_FLHCSR)	8	R/W	See section	3.1.8/40
14	Fan Control and Status Register (CPLD_FANCSR)	8	R/W	0Fh	3.1.9/40
15	Panel LED Control and Status Register (CPLD_LEDCSR)	8	R/W	00h	3.1.10/41
16	SDHC Card Status Register (CPLD_SDSR)	8	R	See section	3.1.11/41
17	Miscellanies Control and Status Register (CPLD_MISCCSR)	8	R/W	See section	3.1.12/42
18	Boot Configuration Override Register (CPLD_BOOTOR)	8	R/W	00h	3.1.13/42
19	Boot Configuration Register 1 (CPLD_BOOTCFG1)	8	R/W	00h	3.1.14/43
19	Boot Configuration Register 2 (CPLD_BOOTCFG2)	8	R/W	00h	3.1.15/43

3.1.1 Chip ID1 Register (CPLD_CHIPID1)

Address: 0h base + 0h offset = 0h

Bit	0	1	2	3	4	5	6	7
Read	CHIPID1							
Write								
Reset	0	1	0	1	0	1	0	1

CPLD_CHIPID1 field descriptions

Field	Description
0–7 CHIPID1	Chip ID1.

3.1.2 Chip ID2 Register (CPLD_CHIPID2)

Address: 0h base + 1h offset = 1h

Bit	0	1	2	3	4	5	6	7
Read	CHIPID2							
Write								
Reset	1	0	1	0	1	0	1	0

CPLD_CHIPID2 field descriptions

Field	Description
0–7 CHIPID2	Chip ID2.

3.1.3 Hardware Version Register (CPLD_HWVER)

Address: 0h base + 2h offset = 2h

Bit	0	1	2	3	4	5	6	7
Read	HW_VER							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x depends on actual board setting.x = Undefined at reset.

CPLD_HWVER field descriptions

Field	Description
0–7 HW_VER	Hardware version. The version field of the hardware board.

3.1.4 Software Version Register (CPLD_SWVER)

Address: 0h base + 3h offset = 3h

Bit	0	1	2	3	4	5	6	7
Read	SW_VER							
Write								
Reset	x*	x*	x*	x*	x*	x*	x*	x*

* Notes:
- x depends on actual board setting.x = Undefined at reset.

CPLD_SWVER field descriptions

Field	Description
0–7 SW_VER	

3.1.5 Reset Control Register (CPLD_RSTCON)

Address: 0h base + 10h offset = 10h

Bit	0	1	2	3	4	5	6	7
Read	SW_RST	DDR_RST	EC1_RST	EC2_RST	Reserved		XGT1_RST	XGT2_RST
Write	w1c	w1c	w1c	w1c			w1c	w1c
Reset	0	0	0	0	0	0	0	0

CPLD_RSTCON field descriptions

Field	Description
0 SW_RST	0 No reset occurs 1 Write a logic 1 will produce whole board reset# signal, this bit can auto clear.
1 DDR_RST	0 No reset occurs 1 Write a logic 1 will produce DDR3 reset# signal, this bit can auto clear.
2 EC1_RST	0 No reset occurs. 1 Write a logic 1 will produce RGMII PHY1(RTL82111E-VB) reset# signal, this bit can auto clear.
3 EC2_RST	0 No reset occurs. 1 Write a logic 1 will produce RGMII PHY2(RTL82111E-VB) reset# signal, this bit can auto clear.

Table continues on the next page...

CPLD_RSTCON field descriptions (continued)

Field	Description
4–5 -	This field is reserved.
6 XGT1_RST	0 No reset occurs. 1 Write a logic 1 will produce 10G BASE-T PHY(AQR105) reset# signal, this bit can auto clear.
7 XGT2_RST	0 No reset occurs. 1 Write a logic 1 will produce 2.5G SGMII PHY(AQR105) reset# signal, this bit can auto clear.

3.1.6 Reset Control Register (CPLD_RSTCON2)

Address: 0h base + 11h offset = 11h

Bit	0	1	2	3	4	5	6	7
Read	Reserved				TDMR_RST	PEX_RST	MPEX1_RST	MPEX2_RST
Write					w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

CPLD_RSTCON2 field descriptions

Field	Description
0–3 -	This field is reserved.
4 TDMR_RST	0 No reset occurs. 0 Write a logic 1 will produce TDM riser card reset# signal, this bit can auto clear.
5 PEX_RST	0 No reset occurs. 1 Write a logic 1 will produce PCIe x4 slot reset# signal, this bit can auto clear.
6 MPEX1_RST	0 No reset occurs. 1 Write a logic 1 will produce miniPCIe card1 reset# signal, this bit can auto clear.
7 MPEX2_RST	0 No reset occurs. 1 Write a logic 1 will produce miniPCIe card2 reset# signal, this bit can auto clear.

3.1.7 Interrupt Status Register (CPLD_INTSR)

NOTE

INTSR register is related with system IRQ0(CPLD_INT1_N) signal, when interrupt occurs, IRQ0 will be logic 0 until all interrupts of INTSR register clear.

Address: 0h base + 12h offset = 12h

Bit	0	1	2	3	4	5	6	7
Read	THERM_INT	RTC_INT	XGT1_INT	XGT2_INT	Reserved		TDMR1_INT	TDMR2_INT
Write								
Reset	0	0	0	0	0	0	0	0

CPLD_INTSR field descriptions

Field	Description
0 THERM_INT	0 No interrupt occurs. 1 Board over temperature interrupt occurs.
1 RTC_INT	0 No interrupt occurs. 1 RTC interrupt occurs.
2 XGT1_INT	0 No reset occurs. 1 10G BASE-T PHY1(AQR105) interrupt occurs.
3 XGT2_INT	0 No reset occurs. 1 2.5G SGMII PHY1(AQR105) interrupt occurs.
4–5 -	This field is reserved.
6 TDMR1_INT	0 No reset occurs. 1 TDM riser card interrupt 1 occurs.
7 TDMR2_INT	0 No reset occurs. 1 TDM riser card interrupt 2 occurs.

3.1.8 Flash Control and Status Register (CPLD_FLHCSR)

Address: 0h base + 13h offset = 13h

Bit	0	1	2	3	4	5	6	7
Read	BOOT_SEL	BANK_OR	SW_BANK_SEL0	SW_BANK_SEL1	SW_BANK_SEL2	BANK_SEL0	BANK_SEL1	BANK_SEL2
Write								
Reset	x*	0	x*	x*	x*	0	0	0

* Notes:
- x depends DIP switch setting.x = Undefined at reset.

CPLD_FLHCSR field descriptions

Field	Description
0 BOOT_SEL	0 Boot from 16bit NOR flash. 1 Boot from 8bit NAND flash.
1 BANK_OR	0 NOR flash bank select from CPLD override disable. 0 NOR flash bank select from CPLD override enable.
2 SW_BANK_SEL0	0 NOR flash bank select bit0 of switch status is 0. 1 NOR flash bank select bit0 of switch status is 1.
3 SW_BANK_SEL1	0 NOR flash bank select bit1 of switch status is 0. 1 NOR flash bank select bit1 of switch status is 1.
4 SW_BANK_SEL2	0 NOR flash bank select bit2 of switch status is 0. 1 NOR flash bank select bit2 of switch status is 1.
5 BANK_SEL0	0 NOR flash bank select bit0 set 0. 1 NOR flash bank select bit0 set 1.
6 BANK_SEL1	0 NOR flash bank select bit1 set 0. 1 NOR flash bank select bit1 set 1.
7 BANK_SEL2	0 NOR flash bank select bit2 set 0. 1 NOR flash bank select bit2 set 1.

3.1.9 Fan Control and Status Register (CPLD_FANCSR)

Address: 0h base + 14h offset = 14h

Bit	0	1	2	3	4	5	6	7
Read Write	Reserved				FAN_PWM			
Reset	0	0	0	0	1	1	1	1

CPLD_FANCSR field descriptions

Field	Description
0–3 -	This field is reserved.
4–7 FAN_PWM	0000 PWM duty cycle is 0%, fan stop running. 0001~1110 PWM duty cycle is 6.7%~93.3%, fan speed control. 1111 PWM duty cycle is 100%, fan full speed.

3.1.10 Panel LED Control and Status Register (CPLD_LEDCSR)

Address: 0h base + 15h offset = 15h

Bit	0	1	2	3	4	5	6	7
Read Write	STS_LED	Reserved						
Reset	0	0	0	0	0	0	0	0

CPLD_LEDCSR field descriptions

Field	Description
0 STS_LED	Light emitting device. 0 Panel LED is on 1 Panel LED flashes at 0.5 s
1–7 -	This field is reserved. Reserved.

3.1.11 SDHC Card Status Register (CPLD_SDSR)

Address: 0h base + 16h offset = 16h

Bit	0	1	2	3	4	5	6	7
Read	Reserved							SD_VDD
Write								
Reset	0	0	0	0	0	0	0	x*

* Notes:
- x depends Jumper setting.x = Undefined at reset.

CPLD_SDSR field descriptions

Field	Description
0–6 -	This field is reserved.
7 SD_VDD	0 SDHC card VDD voltage is 1.8V. 1 SDHC card VDD voltage is 3.3V.

3.1.12 Miscellanies Control and Status Register (CPLD_MISCCSR)

Address: 0h base + 17h offset = 17h

Bit	0	1	2	3	4	5	6	7
Read	Reserved	SLEEP_EN	REQ_MD		TDMR_PRS	PEX_PRS	Reserved	TEST_SEL_N
Write								
Reset	0	0	1	1	x*	x*	0	x*

* Notes:
- x depends on whether TDM or PCIe card is plugged in.x = Undefined at reset.

CPLD_MISCCSR field descriptions

Field	Description
0 -	This field is reserved.
1 SLEEP_EN	Deep sleep enable bit 0 Normal operation. 1 Before enter deep sleep mode, set ‘1’ to this bit, after exit deep sleep mode, set ‘0’ to this bit.
2–3 REQ_MD	00 No reset occurs when HRESET_REQ triggered. 01 HRESET occurs when HRESET_REQ triggered. 10 NA 11 PORESET occurs when HRESET_REQ triggered.
4 TDMR_PRS	0 TDM riser card not present. 1 TDM riser card present.
5 PEX_PRS	0 PCIe x1 card not present. 1 PCIe x1 card present.
6 -	This field is reserved.
7 TEST_SEL_N	0 TEST_SEL_N pin status is 0. 0 TEST_SEL_N pin status is 1.

3.1.13 Boot Configuration Override Register (CPLD_BOOTOR)

Address: 0h base + 18h offset = 18h

Bit	0	1	2	3
Read Write	Reserved			
Reset	0	0	0	0

Bit	4	5	6	7
Read Write	Reserved		PCIE_2.5G_OR	BOOT_OR
Reset	0	0	0	0

CPLD_BOOTOR field descriptions

Field	Description
0–5 -	This field is reserved.
6 PCIE_2.5G_OR	0 PCIe and SGMII 2.5G configuration from CPLD override disable. 1 PCIe and SGMII 2.5G configuration from CPLD override enable.
7 BOOT_OR	0 Boot configuration from CPLD override disable. 1 Boot configuration from CPLD override enable.

3.1.14 Boot Configuration Register 1 (CPLD_BOOTCFG1)

NOTE

For more information on BOOTCFG1 register, refer to QorIQ T1024 datasheet.

Address: 0h base + 19h offset = 19h

Bit	0	1	2	3	4	5	6	7
Read Write	cfg_rcw_src[0:7]							
Reset	0	0	0	0	0	0	0	0

CPLD_BOOTCFG1 field descriptions

Field	Description
0–7 cfg_rcw_src[0:7]	Configure RCW source

3.1.15 Boot Configuration Register 2 (CPLD_BOOTCFG2)

NOTE

For more information on BOOTCFG2 register, refer to QorIQ T1024 datasheet.

Address: 0h base + 19h offset = 19h

Bit	0	1	2	3	4	5	6	7
Read Write	cfg_rcw_ src8	Reserved	cfg_svr[0:1]		Reserved	cfg_eng_use[0:2]		
Reset	0	0	0	0	0	0	0	0

CPLD_BOOTCFG2 field descriptions

Field	Description
0 cfg_rcw_src8	Configure RCW source
1 -	This field is reserved.
2–3 cfg_svr[0:1]	These bit fields overrides SVR register.
4 -	This field is reserved.
5–7 cfg_eng_use[0:2]	These bits are defined by engineers for special use.

Appendix A
How to use AQ_API in U-Boot to Flash Firmware for Aquantia PHY

This appendix describes the steps required to use AQ_API in U-Boot to flash firmware for Aquantia PHY. The prerequisites are given below:

- The AQ_API version is 2.1.0
- The U-Boot is for T1024RDB
- The U-Boot source code is from SDK1.7 and later versions

Perform the following steps to use AQ_API in U-Boot:

1. Apply the following three patches to the U-Boot tree:
   - `added-source-codes-of-API-2.1.0.patch`: Adds the source code of AQ_API 2.1.0. It copies all the AQ_API source code (*.c, *.h) into one folder in U-Boot.
   - `AQ_API-fix-compile-error-for-API-2.1.0.patch`: Fixes the compilation issues that occurred in the original source code while building U-Boot.
   - `mdio-added-flash-command.patch`: Adds an MDIO flash command for U-Boot. This command will call a function in AQ_API to perform the actual flash programming.
2. Build and update a new U-Boot on the T1024RDB board.

The Aquantia AQR105 PHY firmware has been programmed to PHY when shipping the board to customers, there is no need to update PHY firmware. If it is still required to update the PHY firmware, follow the instructions given below:

- Program AQR105 PHY firmware for 10G XFI (using RCW 0x95):

```
=> tftp 1000000 AQ28nm-FW_2.0.B9_Freescale_T1024RDB_012115.cld
Using FM1@DTSEC4 device
Filename 'AQ28nm-FW_2.0.B9_Freescale_T1024RDB_012115.cld'.
Load address: 0x1000000
Loading: ############################
         2.4 MiB/s
done
Bytes transferred = 287746 (46402 hex)
=> mdio list
FSL_MDIO0:
2 - RealTek RTL8211E <--> FM1@DTSEC4
6 - RealTek RTL8211E <--> FM1@DTSEC3
FM_TGEC_MDIO:
1 - Aquantia AQR105 <--> FM1@TGEC1
=> mii dev FM_TGEC_MDIO
```

```
=> mdio flash FM1@TGEC1 0x1000000 0x46402
flashing firmware for AQR105
Device burned and verified
```

- Program AQR105 PHY firmware for 2.5G SGMII (using RCW 0x135):

```
=> tftp 1000000 AQ28nm-FW_2.0.B3_Freescale_T1024RDB_120514.cld
Using FM1@DTSEC4 device
Filename 'AQ28nm-FW_2.0.B3_Freescale_T1024RDB_120514.cld'.
Load address: 0x1000000
Loading: ##############################
         2.2 MiB/s
done
Bytes transferred = 287746 (46402 hex)
=> mdio list
FSL_MDIO0:
2 - RealTek RTL8211E <--> FM1@DTSEC4
FM_TGEC_MDIO:
2 - Aquantia AQR105 <--> FM1@DTSEC3
=> mii dev FM_TGEC_MDIO
=> mdio flash FM1@DTSEC3 0x1000000 0x46402
flashing firmware for AQR105
Device burned and verified

=>  mdio read FM1@DTSEC3  0x1e.0xc885
Reading from bus FM_TGEC_MDIO
PHY at address 2:
30.51333 - 0xb3
```

The AQR105 PHY is connected to EMI2 bus and FM_TGEC_MDIO. The syntax of the MDIO flash command is:

```
mdio flash <port_name> <firmware_address> <firmware_size>
```

After flash programming, the firmware version can be read out from registers 0x1e.0x20 and 0x1e.0xc885.

Appendix B
Revision History

The below table summarizes the revisions to this document.

Table B-1. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 0	04/2015		Initial public release.

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