LMX2571 Low-Power, High-Performance PLLatinum™ RF Synthesizer with FSK Modulation

1 Features

- Any Frequency from 10 MHz to 1344 MHz
- Low Phase Noise and Spurs
  - –123 dBc/Hz at 12.5 kHz Offset @ 480 MHz
  - –145 dBc/Hz at 1 MHz Offset @ 480 MHz
  - Normalized PLL Noise Floor of –231 dBc/Hz
  - Spurious Better Than –75 dBc/Hz
- New FastLock to Reduce Lock Time
- A Novel Technique to Remove Integer Boundary Spurs
- Integrated 5-V Charge Pump and Output Divider for External VCO Operation
- 2-, 4- and 8-level or Arbitrary Level Direct Digital FSK Modulation
- One TX/RX Output or Two Fanout Outputs
- Crystal, XO or Differential Reference Clock Input
- Low Current Consumption
  - 39-mA Typical Synthesizer Mode (Int. VCO)
  - 9-mA Typical PLL Mode (Ext. VCO)
- 24-Bit Fractional-N Delta Sigma Modulator

2 Applications

- Duplex Mode Digital Professional 2-Way Radio
  - dPMR, DMR, PDT, P25 Phase I
- Low Power Radio Communication Systems
  - Satcom Modem
  - Wireless Microphone
  - Propriety Wireless Connectivity
- Handheld Test and Measurement Equipment

3 Description

The LMX2571 is a low-power, high-performance, wideband PLLatinum™ RF synthesizer that integrates a delta-sigma fractional N PLL, multiple core voltage-controlled oscillator (VCO), programmable output dividers and two output buffers. The VCO cores work up to 5.376 GHz resulting in continuous output frequency range of 10 MHz to 1344 MHz.

This synthesizer can also be used with an external VCO. To that end, a dedicated 5-V charge pump and an output divider are available for this configuration.

A unique programmable multiplier is also incorporated to help improve spurs, allowing the system to use every channel even if it falls on an integer boundary.

The output has an integrated SPDT switch that can be used as a transmit/receive switch in FDD radio application. Both outputs can also be turned on to provide 2 outputs at the same time.

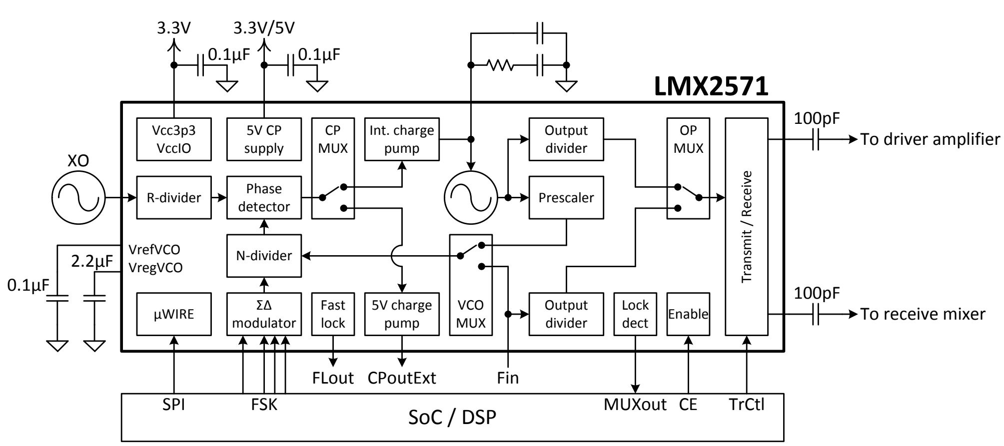
The LMX2571 supports direct digital FSK modulation through programming or pins. Discrete level FSK, pulse shaping FSK, and analog FM modulation are supported.

A new FastLock technique can be used allowing the user to step from one frequency to the next in less then 1.5 ms even when an external VCO is used with a narrow band loop filter.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX2571	WQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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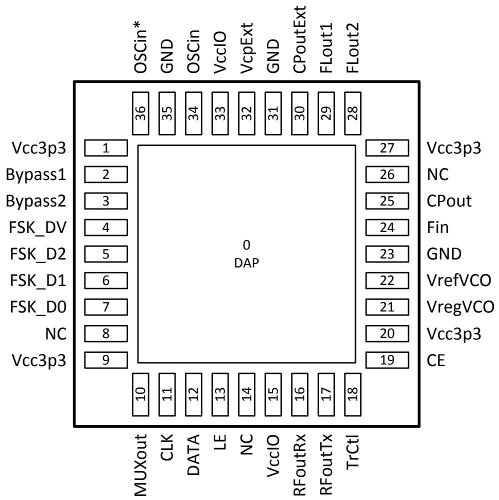
4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

5 Pin Configuration and Functions

WQFN (NJK) Package
36 Pins
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Bypass1	2	Bypass	Place a 100-nF capacitor to GND.
Bypass2	3	Bypass	Place a 100-nF capacitor to GND.
CE	19	Input	Chip Enable input. Active HIGH powers on the device.
CLK	11	Input	MICROWIRE clock input.
CPout	25	Output	Internal VCO charge pump access point to connect to a 2^{nd} order loop filter.
CPoutExt	30	Output	5-V charge pump output used in PLL mode (external VCO).
DAP	0	GND	The DAP should be grounded.
DATA	12	Input	MICROWIRE serial data input.
Fin	24	Input	High frequency AC coupled input pin for an external VCO. Leave it open or AC coupled to GND if not being used.
FSK_D0	7	Input	FSK data bit 0 (FSK PIN mode) / I2S FS input (FSK I2S mode).
FSK_D1	6	Input	FSK data bit 1 (FSK PIN mode) / I2S DATA input (FSK I2S mode).
FSK_D2	5	Input	FSK data bit 2 (FSK PIN mode).
FSK_DV	4	Input	FSK data valid input (FSK PIN mode) / I2S CLK input (FSK I2S mode).
FLout1	29	Output	FastLock output control 1 for external switch. Output is HIGH when F1 is selected.
FLout2	28	Output	FastLock output control 2 for external switch. Output is HIGH when F2 is selected.
GND	23	GND	VCO ground.
GND	31	GND	Charge pump ground.
GND	35	GND	OSCin ground.
LE	13	Input	MICROWIRE latch enable input.
MUXout	10	Output	Multiplexed output that can be assigned to lock detect or readback serial data output.
NC	8,14, 26	NC	Do not connect these pins.
OSCin	34	Input	Reference clock input.
OSCin*	36	Input	Complementary reference clock input.
RFoutRx	16	Output	RF output used to drive receive mixer. Selectable open drain or push-pull output.
RFoutTx	17	Output	RF output used to drive transmit signal. Selectable open drain or push-pull output.
TrCtl	18	Input	Transmit/Receive control. This pin controls the RF output port and the output frequency selection.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
Vcc3p3	1, 9, 20, 27	Supply	Connect to 3.3-V supply.
VccIO	15, 33	Supply	Supply for digital logic interface. Connect to 3.3-V supply.
VcpExt	32	Supply	Supply for 5-V charge pump. Connect to 5-V supply in PLL mode. Connect to either 3.3-V or 5-V supply in synthesizer mode.
VrefVCO	22	Bypass	LDO output. Place a 100-nF capacitor to GND.
VregVCO	21	Bypass	Bias circuitry for the VCO. Place a 2.2-µF capacitor to GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
V_{IO}	IO supply voltage	–0.3	3.6	V
V_{IN}	IO input voltage		V_{CC} + 0.3	V
V_{CP}	Charge pump supply voltage		5.25	V
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Power supply voltage		3.15	3.45	V
V_{IO}	IO supply voltage			V_{CC}	V
V_{CP}	Charge pump supply voltage	PLL mode (external VCO)		5	V
		Synthesizer mode (internal VCO)	V_{CC}	5	
T_A	Ambient temperature		–40	85	°C
T_J	Junction Temperature			125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMX2571 WQFN (NJK) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, V_{IO} = V_{CC}, –40 °C ≤ T_A ≤ 85 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, V_{CP} = 3.3 V or 5 V in synthesizer mode, V_{CP} = 5 V in PLL mode, T_A = 25 °C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I_{CC}	Total current in synthesizer mode (internal VCO)	f_{OUT} = 480 MHz SE OSCin	Configuration A[1]		39		mA
			Configuration B[2]		44		
			Configuration C[3]		46		
			Configuration D[4]		51		
I_{PLL}	Total current in PLL mode (external VCO)		Configuration E[5]		9		
			Configuration F[6]		15		
			Configuration G[7]		21		
$I_{CC}PD$	Power down current	CE = 0V or POWERDOWN bit = 1 V_{CC} = 3.3 V, Push-pull output			0.9		
OSCIN REFERENCE INPUT							
f_{OSCin}	OSCin frequency range	Single-ended or differential input		10		150	MHz
V_{OSCin}	OSCin input voltage[8]	Single-ended input		1.4		3.3	V
		Differential input		0.15		1.5	
CRYSTAL REFERENCE INPUT							
f_{XTAL}	Crystal frequency range	Fundamental model, ESR < 200 Ω		10		40	MHz
C_{IN}	OSCin input capacitance				1		pF
MULT							
f_{MULTin}	MULT input frequency	MULT > Pre-divider Not supported with crystal reference input		10		30	MHz
$f_{MULTout}$	MULT output frequency			60		130	MHz
PLL							
f_{PD}	Phase detector frequency					130	MHz
K_{PD}	Charge pump current[9]	Programmable minimum value	Internal charge pump		312.5		µA
			5-V charge pump		625		
		Per programmable step	Internal charge pump		312.5		
			5-V charge pump		625		
		Programmable maximum value	Internal charge pump		7187.5		
			5-V charge pump		6875		

(1) f_{OSCin} = 19.44 MHz, MULT = 1, Prescaler = 4, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(2) f_{OSCin} = 19.44 MHz, MULT = 1, Prescaler = 2, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(3) f_{OSCin} = 19.44 MHz, MULT = 5, Prescaler = 2, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(4) f_{OSCin} = 19.44 MHz, MULT = 5, Prescaler = 2, f_{PD} = 97.2 MHz, one RF output, output type = push pull, output power = –3 dBm
(5) f_{OSCin} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, output from VCO
(6) f_{OSCin} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(7) f_{OSCin} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, two RF outputs, output type = push pull, output power = –3 dBm
(8) See *OSCin Configuration* for definition of OSCin input voltage.
(9) This is referring to the total base charge pump current. In PLL mode, this is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. In synthesizer mode, this is equal to CP_IDN + CP_IUP. See Table 5, Table 6 and Table 7 for details.

Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, V_{IO} = V_{CC}, –40 °C ≤ T_A ≤ 85 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, V_{CP} = 3.3 V or 5 V in synthesizer mode, V_{CP} = 5 V in PLL mode, T_A = 25 °C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise(10)	At maximum charge pump current	Internal charge pump		–124		dBc/Hz
			5-V charge pump		–120		
PN_{PLL_Flat}	Normalized PLL noise floor(10)		Internal charge pump		–231		dBc/Hz
			5-V charge pump		–226		
f_{RFin}	External VCO input frequency			100		1400	MHz
P_{RFin}	External VCO input power	f_{RFin} < 1 GHz		–10			dBm
		f_{RFin} ≥ 1 GHz		–5			
VCO							
f_{VCO}	VCO frequency			4300		5376	MHz
K_{VCO}	VCO gain(11)	f_{VCO} = 4800 MHz			56		MHz/V
$\lvert \Delta T_{CL} \rvert$	Allowable temperature drift(12)	VCO not being re-calibrated, –40 °C ≤ T_A ≤ 85 °C				125	°C
t_{VCOCal}	VCO calibration time	f_{OSCin} = f_{PD} = 100 MHz			140		µs
PN_{VCO}	Open loop VCO phase noise	f_{OUT} = 480 MHz	100 Hz offset		–32.4		dBc/Hz
			1 kHz offset		–62.3		
			10 kHz offset		–92.1		
			100 kHz offset		–121.1		
			1 MHz offset		–144.5		
			10 MHz offset		–156.8		
RF OUTPUT							
f_{OUT}	RF output frequency	Synthesizer mode		10		1344	MHz
		PLL mode, RF output from buffer		10		1400	
P_{TX}, P_{RX}	RF output power	f_{OUT} = 480 MHz	Power control bit = 6		0		dBm
$H2_{RFout}$	Second harmonic				–25		dBc
DIGITAL FSK MODULATION							
FSK_{Level}	FSK level(13)	FSK PIN mode		2		8	
FSK_{Baud}	FSK baud rate(14)	Loop bandwidth = 200 kHz			100		kSPs
FSK_{Dev}	FSK deviation	Configuration H(15)			±39		kHz
DIGITAL INTERFACE							
V_{IH}	High level input voltage			1.4		V_{IO}	V
V_{IL}	Low level input voltage					0.4	V
I_{IH}	High level input current	V_{IH} = 1.75 V		–25		25	µA
I_{IL}	Low level input current	V_{IL} = 0 V		–25		25	µA
V_{OH}	High level output voltage	I_{OH} = 500 µA		2			V
V_{OL}	Low level output voltage	I_{OL} = –500 µA			0	0.4	V

(10) Measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as:
PLL_Total = 10 * log[$10^{(PLL\_Flat / 10)} + 10^{(PLL\_Flicker / 10)}$]
PLL_Flat = PN1Hz + 20 * log(N) + 10 * log(f_{PD})
PLL_Flicker = PN10kHz – 10 * log(Offset / 10 kHz) + 20 * log(f_{OUT} / 1 GHz)
(11) The VCO gain changes as a function of the VCO core and frequency. See Integrated VCO for details.
(12) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device, and still have the device stay in lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.
(13) The data showed here simply specifies the range of discrete FSK level that is supported in PIN mode. PIN mode supports 2-, 4- and 8-level of FSK modulation. If arbitrary level of FSK modulation is desired, use FSK SPI™ FAST mode or FSK I2S mode. See *Direct Digital FSK Modulation* for details.
(14) The baud rate is limited by the loop bandwidth of the PLL loop. As a general rule of thumb, it is desirable to have the loop bandwidth at least twice the baud rate.
(15) f_{PD} = 100 MHz, DEN = 2^{24}, CHDIV1 = 5, CHDIV2 = 2, Prescaler = 2, FSK step value = 32716, 32819. The maximum achievable frequency deviation depends on the configuration, see *Direct Digital FSK Modulation* for details.

6.6 Timing Requirements

3.15 V ≤ V_{CC} ≤ 3.45 V, V_{IO} = V_{CC}, –40 °C ≤ T_A ≤ 85 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, T_A = 25 °C.

			MIN	NOM	MAX	UNIT
MICROWIRE TIMING						
t_{ES}	Clock to enable low time	See Figure 1	5			ns
t_{CS}	Data to clock setup time		2			ns
t_{CH}	Data to clock hold time		2			ns
t_{CWH}	Clock pulse width high		5			ns
t_{CWL}	Clock pulse width low		5			ns
t_{CES}	Enable to clock setup time		5			ns
t_{EWH}	Enable pulse width high		2			ns

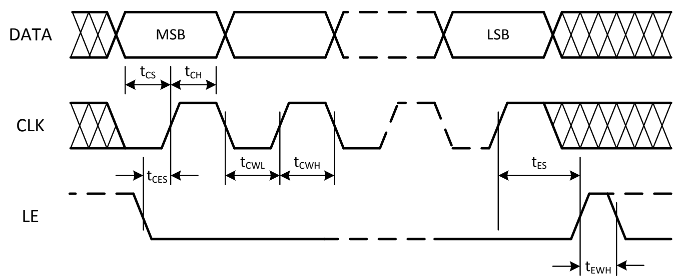


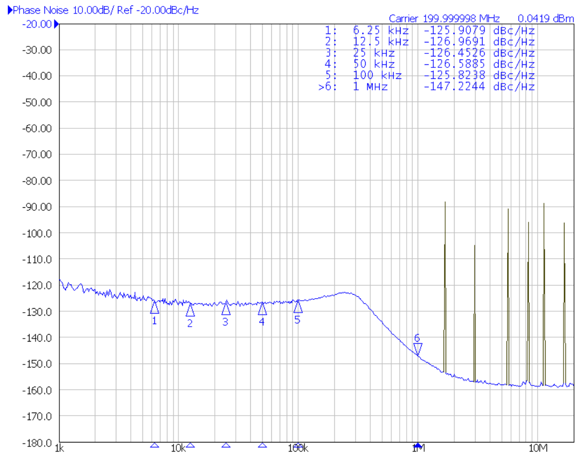
Figure 1. MICROWIRE Timing Diagram

There are several other considerations for programming:

- A slew rate of at least 30 V/µs is recommended for the CLK, DATA and LE. The same apply for other digital control signals such as FSK_D[0:2] and FSK_DV signals.
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift register to an active register.
- The LE pin may be held high after programming, causing the LMX2571 to ignore clock pulses.
- When CLK or DATA lines are shared between devices, it is recommended to divide down the voltage to the CLK, DATA, and LE pins closer to the minimum voltage. This provides better noise immunity.
- If the CLK and DATA lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

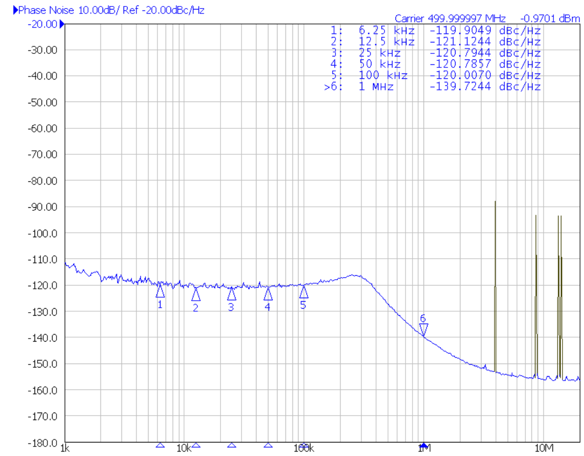
6.7 Typical Characteristics

At T_A = 25 °C, unless otherwise noted



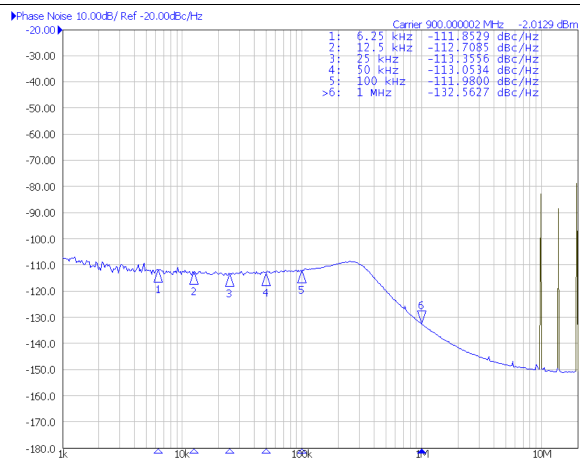
OSCin = 19.44 MHz f_{OUT} = 200 MHz Synthesizer mode

Figure 2. Typical Close Loop Phase Noise



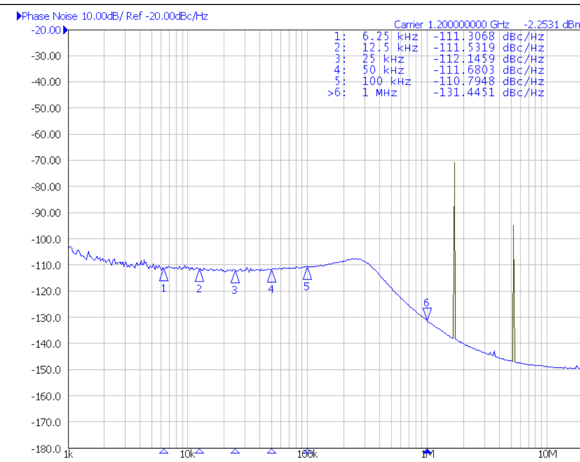
OSCin = 19.44 MHz f_{OUT} = 500 MHz Synthesizer mode

Figure 3. Typical Close Loop Phase Noise



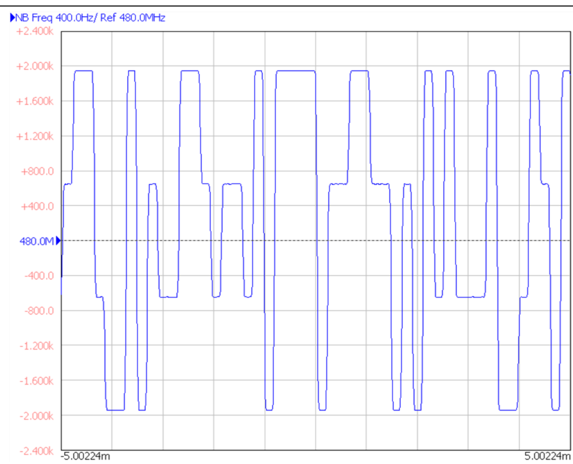
OSCin = 19.44 MHz f_{OUT} = 900 MHz Synthesizer mode

Figure 4. Typical Close Loop Phase Noise



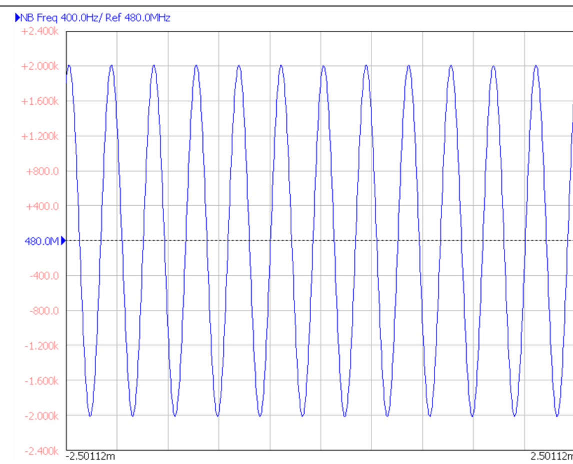
OSCin = 19.44 MHz f_{OUT} = 1200 MHz Synthesizer mode

Figure 5. Typical Close Loop Phase Noise



FSK_{Baud} = 4.8 kSPS FSK PIN mode

Figure 6. 4FSK Direct Digital Modulation

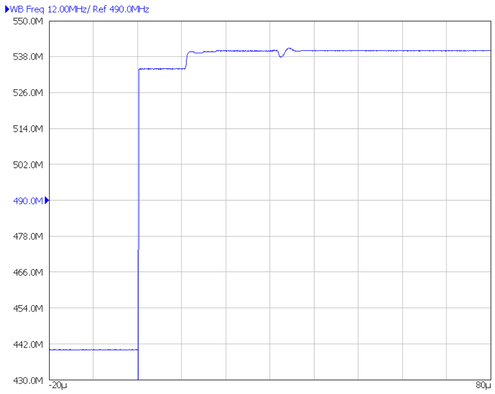


Reference clock is a FM modulated signal with f_{MOD} = 2.4 kHz

Figure 7. FM Modulation via Reference Clock

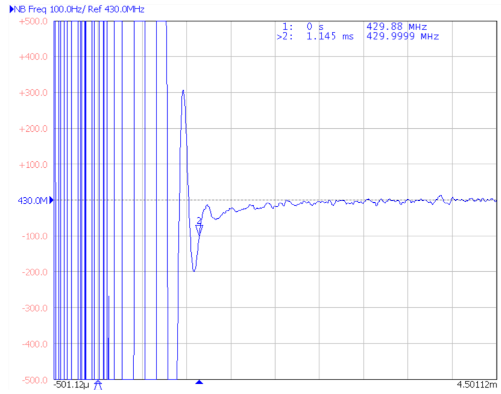
Typical Characteristics (continued)

At T_A = 25 °C, unless otherwise noted



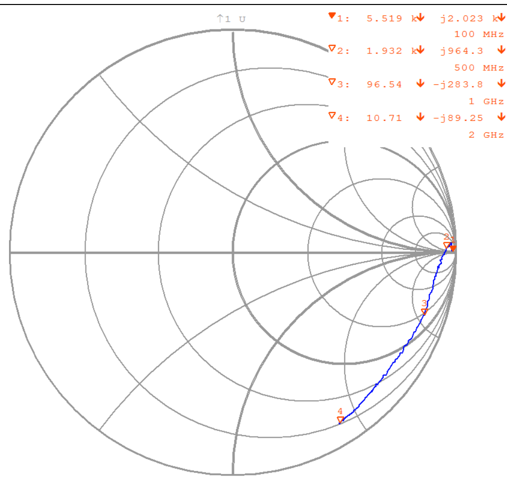
Switching between int. and ext. VCO as well as Tx and Rx port

Figure 8. Output Port and VCO Switching



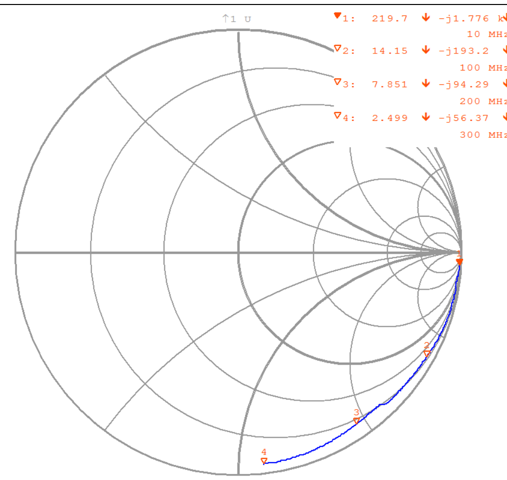
Freq. jump = 50 MHz LBW = 4 kHz PLL mode

Figure 9. FastLock with SPST Switch



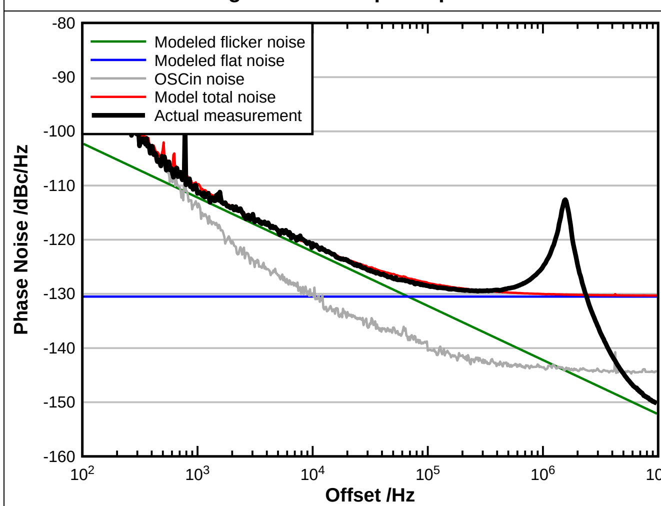
Start: 100 MHz Stop: 2000 MHz

Figure 10. Fin input impedance



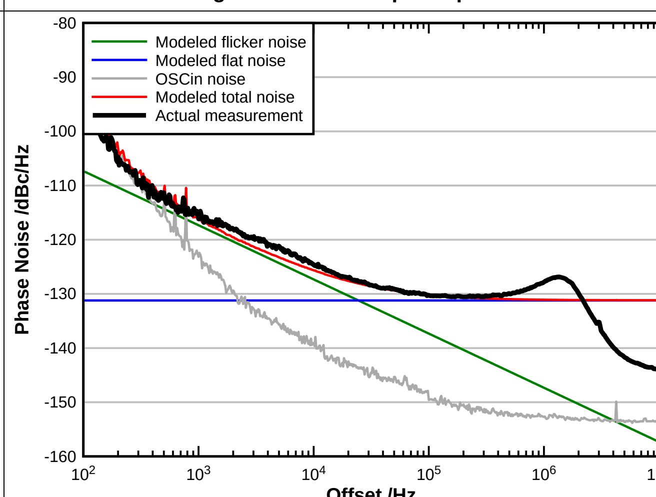
Start: 10 MHz Stop: 300 MHz

Figure 11. OSCin input impedance



f_{OUT} = 1228.8 MHz f_{PD} = 122.88 MHz Synthesizer mode

Figure 12. Normalized PLL 1/f Noise and Noise Floor



f_{OUT} = 430.08 MHz f_{PD} = 61.44 MHz PLL mode

Figure 13. Normalized PLL 1/f Noise and Noise Floor

7 Detailed Description

7.1 Overview

The LMX2571 is a frequency synthesizer with low-noise, high-performance integrated VCOs. The 5-GHz VCO cores, together with the output channel dividers, can produce frequencies from 10 MHz to 1344 MHz. The LMX2571 supports two operation modes, synthesizer mode and PLL mode. In synthesizer mode, the entire device is utilized; in PLL mode the internal VCO is bypassed, and an external VCO is required to implement a complete synthesizer.

The reference clock input supports a crystal used for the on-chip oscillator, AC-coupled differential clock signals, and DC-coupled single-ended clock signals such as XO or CMOS clock devices.

The PLL is a fractional-N PLL with programmable Delta Sigma modulator (first order to fourth order). The fractional denominator is of variable length and up to 24-bits long, providing a frequency step with very fine resolution.

The internal VCO can be bypassed, allowing the use of an external VCO. A separate 5-V charge pump is dedicated for the external VCO, eliminating the need for an op-amp to support 5-V VCOs. A new advanced FastLock technique is developed to shorten the lock time to less than 1.5 ms, even there is a very narrow loop bandwidth.

A unique programmable multiplier is incorporated in the R-divider. The multiplier is used to avoid and reduce integer boundary spurs or to increase the phase detector frequency for higher performance.

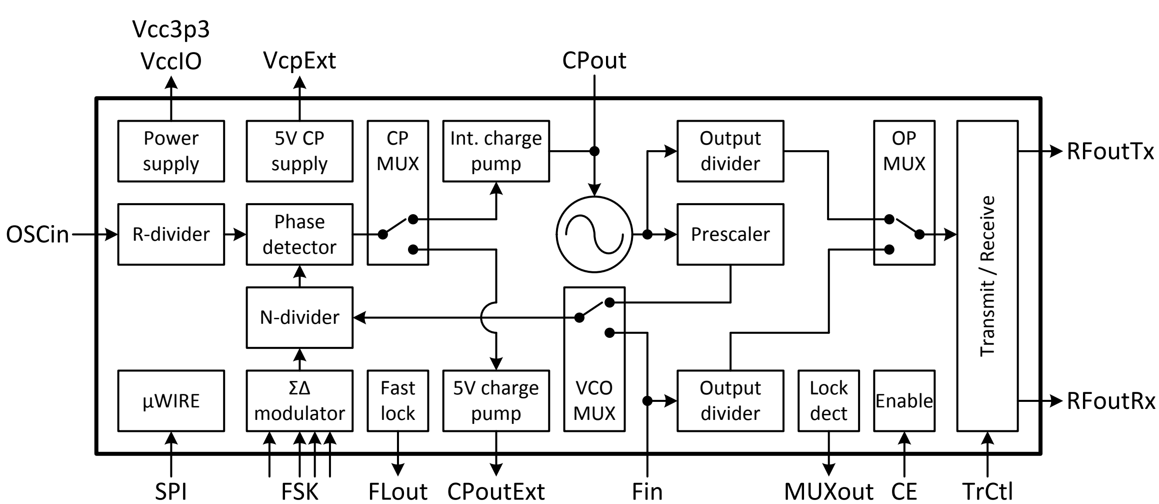
The LMX2571 supports direct digital FSK modulation, thus allowing a change in the output frequency by changing the N-divider value. The N-divider value can be programmed through MICROWIRE interface or through pins. Discrete 2-, 4- and 8-level FSK, as well as arbitrary-level FSK, are supported. Arbitrary-level FSK can be used to construct pulse-shaping FSK or analog-FM modulation.

The output has an integrated T/R switch, and the divided-down internal or external VCO signal can be output to either the TX port or the RX port. The switch can also be configured as a 1:2 fanout buffer, providing the signal on both outputs at the same time. In addition to port switching, the output frequency can be switched between two pre-defined frequencies, F1 and F2, simultaneously. This feature is ideal for use in FDD duplex system where the TX frequency is different from RX (LO) frequency.

The LMX2571 requires only a single 3.3-V power supply. Digital logic interface is 1.8-V input compatible. The analog blocks power supplies use integrated LDOs, eliminating the need for high performance external LDOs.

Programming of the device is achieved through the MICROWIRE interface. The device can be powered down through a register programming or toggling the Chip Enable (CE) pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCin and OSCin* pins are used as frequency reference inputs to the device. The OSCin pin can be driven single-ended with a CMOS clock or a crystal oscillator. The on-chip crystal oscillator can also be used with an external crystal as the reference clock. Differential clock input is also supported, making it easily to interface with high performance system clock devices such as TI's LMK series clock devices.

Because the OSCin or OSCin* signal is used as a clock for VCO calibration, a proper signal needs to be applied at the OSCin and/or OSCin* pin at the time of programming the R0 register. A higher slew rate tends to yield the best fractional spurs and phase noise, so a square wave signal is best for the OSCin and/or OSCin*pins. If using a sine wave, higher frequencies tend to yield better phase noise and fractional spurs due to their higher slew rates.

7.3.2 R-Dividers and Multiplier

The R-divider consists of a Pre-divider, a Multiplier (MULT), and a Post-divider.

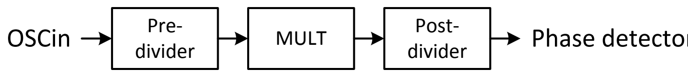


Figure 14. R-Divider

Both the Pre- and Post-dividers divide frequency down while the MULT multiplies frequency up. The purpose of adding a multiplier is to avoid and reduce integer boundary spurs or to increase the phase-detector frequency for higher performance. See *MULT Multiplier* for details. The phase detector frequency, f_{PD}, is therefore equal to

$$f_{PD} = (f_{OSCin} / \text{Pre-divider}) * (\text{MULT} / \text{Post-divider}) \quad (1)$$

When using the Multiplier (MULT > 1), there are some points to remember:

- The Multiplier must be greater than the Pre-divider.
- Crystal mode must be disabled (XTAL_EN=0).
- Using the multiplier may add noise, especially for multiplier values greater than 6.

7.3.3 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-divider and N-divider and generates a correction current corresponding to the phase error. This charge pump current is programmable to different strengths.

7.3.4 PLL N-Divider and Fractional Circuitry

The total N-divider value is determined by $N_{integer}$ + NUM / DEN. The N-divider includes fractional compensation and can achieve any fractional denominator (DEN) from 1 to 16,777,215 (2^{24} – 1). The integer portion, $N_{integer}$, is the whole part of the N-divider value and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. $N_{integer}$, NUM and DEN are programmable.

The order of the delta sigma modulator is also programmable from integer mode to fourth order. There are several dithering modes that are also programmable. Dithering is used to reduce fractional spurs. In order to make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

7.3.5 Partially Integrated Loop Filter

The LMX2571 integrates the third and fourth pole of the loop filter. The values for the resistors can be programmed independently through the MICROWIRE interface. The larger the values of the resistors, the stronger the attenuation of the internal loop filter. This partially integrated loop filter can only be used in synthesizer mode.

Feature Description (continued)

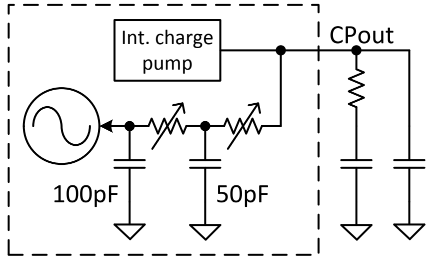


Figure 15. Integrated Loop Filter

7.3.6 Low-Noise, Fully Integrated VCO

The LMX2571 includes a fully integrated VCO. The VCO generates a frequency which varies with the tuning voltage from the loop filter. Output of the VCO is fed to a prescaler before going to the N-divider. The prescaler value is selectable between 2 and 4. In general, prescaler equals 2 will result in better phase noise especially when the PLL is operated in fractional-N mode. If the prescaler equals 4, however, the device will consume less current. The VCO frequency is related to the other frequencies and Prescaler as follows:

$$f_{VCO} = f_{PD} * \text{N-divider} * \text{Prescaler} \quad (2)$$

In order to reduce the VCO tuning gain, thus improving the VCO phase noise performance, the VCO frequency range is divided into several different frequency bands. This creates the need for frequency calibration in order to determine the correct frequency band given a desired output frequency. The VCO is also calibrated for amplitude to optimize phase noise. These calibration routines are activated any time that the R0 register is programmed with the FCAL_EN bit equals one. It is important that a valid OSCin signal must present before VCO calibration begins.

This device will support a full sweep of the valid temperature range of 125°C (–40°C to 85°C) without having to re-calibrate the VCO. This is important for continuous operation of the synthesizer under the most extreme temperature variation.

7.3.7 External VCO Support

The LMX2571 supports an external VCO in PLL mode. In PLL mode, the internal VCO and its associated charge pump are powered down, and a 5-V charge pump is switched in to support external VCO. No extra external low noise op-amp is required to support 5-V tuning range VCO. The external VCO output can be obtained directly from the VCO or from the device's RF output buffer.

7.3.8 Programmable RF Output Divider

The internal VCO RF output divider consists of two sub-dividers; the total division value is equal to the multiplication of them. As a result, the minimum division is 4 while the maximum division is 448.

Figure 16. VCO Output Divider

There is only one output divider when external VCO is being used. This divider supports even and odd division, and its values are programmable between 1 and 10.

7.3.9 Programmable RF Output Buffer

The RF output buffer type is selectable between push-pull and open drain. If open drain buffer is selected, external pullup to VccIO is required. Regardless of output type, output power can be programmed to various levels. The RF output buffer can be disabled while still keeping the PLL in lock. See *RF Output Buffer Type* for details.

Feature Description (continued)

7.3.10 Integrated TX, RX Switch

The LMX2571 integrates a T/R switch which is controlled by the TrCtl pin. The output from the internal VCO or external VCO divider will be routed to either the RFoutTx or RFoutRx ports, depending on the state of the TrCtl pin. The TrCtl pin not only controls the output port, but may also switch the output frequency simultaneously. For example, if TrCtl = 1, the active port is RFoutTx with an output frequency of F1. When TrCtl changes from 1 to 0, the active port could be RFoutRx with an output frequency of F2. LMX2571 has two sets of register to store the configurations for F1 and F2.

The T/R switch could also be configured as a fanout buffer to output the same signal at both RFoutTx and RFoutRx ports at the same time. All of these features are also programmable, see *Programming* and *Frequency and Output Port Switching with TrCtl Pin* for details.

7.3.11 Powerdown

The LMX2571 can be powered up and down using the CE pin or the POWERDOWN bit. All registers are preserved in memory while it is powered down. When the device comes out of the powered down state, either by resuming the POWERDOWN bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), it is required that register R0 with FCAL_EN=1 be programmed again to re-calibrate the device.

7.3.12 Lock Detect

The MUXout pin of the LMX2571 can be configured to output a signal that indicates when the PLL is being locked. If lock detect is enabled while the MUXout pin is configured as a lock-detect output, when the device is locked the MUXout pin output is a logic HIGH voltage. When the device is unlocked, MUXout output is a logic LOW voltage.

7.3.13 FSK Modulation

Direct digital FSK modulation is supported in LMX2571. FSK modulation is achieved by changing the output frequency by changing the N-divider value. The LMX2571 supports four different types of FSK operation.

1. FSK PIN mode. LMX2571 supports 2-, 4- and 8-level FSK modulation in PIN mode. In this mode, symbols are directly fed to the FSK_D0, FSK_D1, and FSK_D2 pins. Symbol clock is fed to the FSK_DV pin. Symbols are latched into the device on the rising edge of the symbol clock. The maximum supported symbol clock rate is 1 MHz. The device has eight dedicated registers to pre-store the desired FSK frequency deviations, with each register corresponding to one of the FSK symbols. The LMX2571 will change its output frequency according to the states on the FSK pins; no extra register programming is required.
2. FSK SPI mode. This mode is identical to the FSK PIN mode with the exception that the control for the selected FSK level is not performed with external pins but with register R34. Each time when register R34 is programmed, change only the FSK_DEV_SEL field to select the desired FSK frequency deviation as stored in the dedicated registers.
3. FSK SPI FAST mode. In this mode, instead of selecting one of the pre-stored FSK level, change the FSK deviation directly by writing to the register R33, FSK_DEV_SPI_FAST field. As a result, this mode supports arbitrary-FSK level, which is useful to construct pulse-shaping or analog-FM modulation.
4. FSK I2S mode. This mode is similar to the FSK SPI FAST mode, but the programming format is an I2S format on dedicated pins instead of SPI. The benefit of using I2S is that this interface could be shared and synchronous to other digital audio interfaces. The same FSK data input pins that are used in FSK PIN mode are re-used to support I2S programming. In this mode only the 16 bits of DATA field is required to program. The data is transmitted on the high or low side of the frame sync (programmable in register R34, FSK_I2S_FS_POL). The unused side of the frame sync needs to be at least one clock cycle. In other words, 17 (16 + 1) CLK cycles are required at a minimum for one I2S frame. Maximum I2S clock rate is 100 MHz.

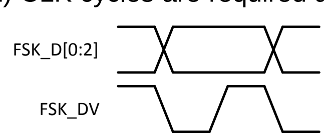


Figure 17. FSK PIN Mode Timing

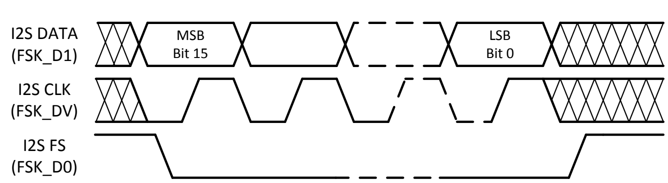


Figure 18. FSK I2S Mode Timing

Feature Description (continued)

See *Direct Digital FSK Modulation* for FSK operation details.

7.3.14 FastLock

The LMX2571 includes a FastLock feature that can be used to improve the lock times in PLL mode when the loop bandwidth is small. In general, the lock time is approximately equal to 4 divided by the loop bandwidth. If the loop bandwidth is 1 kHz, then the lock time would be 4 ms. However, if the f_{PD} is much higher than the loop bandwidth, cycle slipping may occur, and the actual lock time will be much longer. Traditional fastlock usually reduces lock time by increasing loop bandwidth during frequency switching. However, there is a limitation on the achievable maximum loop bandwidth due to limitation on charge-pump current and loop filter component values. In some cases, this kind of fastlock technique will make cycle slip even worse.

The LMX2571 adopts a new FastLock approach that eliminates the cycle slip problem. With an external analog SPST switch in conjunction with LMX2571's FastLock control, the lock time for a 100-MHz frequency switch could be settled in less than 1.5 ms. See *FastLock with External VCO* for details.

7.3.15 Register Readback

The LMX2571 allows any of its registers to be read back. The MUXout pin can be programmed to support either lock-detect output or register-readback serial-data output. To read back a certain register value, follow the following steps:

1. Set the R/W bit to 1; the data field contents are ignored.
2. Send the register to the device; readback serial data will be output starting at the 9th clock cycle.

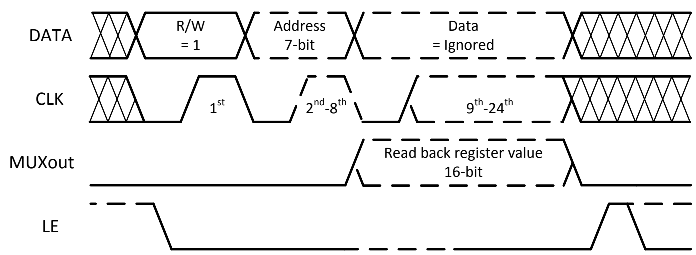


Figure 19. Register Readback Timing Diagram

7.4 Device Functional Modes

7.4.1 Operation Mode

The device can be operated in synthesizer mode or PLL mode.

1. Synthesizer mode. The internal VCO will be adopted.
2. PLL mode. The device is operated as a standalone PLL; an external VCO is required to complete the loop.

7.4.2 Duplex Mode

LMX2571 supports fast frequency switching between two pre-defined register sets, F1 and F2. This feature is good for duplex operation. The device supports three duplex modes:

1. Synthesizer duplex mode. Both F1 and F2 are operated in synthesizer mode.
2. PLL duplex mode. Both F1 and F2 are operated in PLL mode.
3. Synthesizer/PLL duplex mode. In this mode, F1 and F2 will be operated in different operation mode.

7.4.3 FSK Mode

LMX2571 supports four direct digital FSK modulation modes.

1. FSK PIN mode. 2-, 4- and 8-level FSK modulation. Modulation data is fed to the device through dedicated pins.
2. FSK SPI mode. 2-, 4- and 8-level FSK modulation. Pre-defined FSK deviation is selected through SPI programming.

Device Functional Modes (continued)

3. FSK SPI FAST mode. This mode supports arbitrary-level FSK modulation. Desired FSK deviation is written to the device through SPI programming.
4. FSK I2S mode. Arbitrary-level FSK modulation is supported. Desired FSK deviation is fed to the device through dedicated pins.

7.5 Programming

The LMX2571 is programmed using several 24-bit registers. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field, an address field, and a R/W bit. The MSB is the R/W bit. 0 means register write while 1 means register read. The following 7 bits, ADDR[6:0], form the address field which is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock. Serial data is shifted MSB first into the shift register when programming. When LE goes high, data is transferred from the data field into the selected active register bank. See Figure 1 for timing diagram details.

7.5.1 Recommended Initial Power on Programming Sequence

When the device is first powered up, it needs to be initialized, and the ordering of this programming is important. The sequence is listed below. After this sequence is completed, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the Vcc pins are at the proper levels.
2. If CE is LOW, pull it HIGH.
3. Wait 100 µs for the internal LDOs to become stable.
4. Ensure that a valid reference is applied to the OSCin pin.
5. Program register R0 with RESET=1. This will ensure all the registers are reset to their default values.
6. Program in sequence registers R60, R58, R53, …, R1 and then R0.

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies in different scenarios is as follows:

1. If the N-divider is changing, program the relevant registers, then program R0 with FCAL_EN = 1.
2. In FSK SPI mode, FSK SPI FAST mode, and FSK I2S mode, the fractional numerator is changing; program the relevant registers only.
3. If switching frequency between F1 and F2, program the relevant control registers only or toggle the TrCtl pin. See *Frequency and Output Port Switching with TrCtl Pin* for details.

7.6 Register Maps

REG.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	R/W	ADDRESS[6:0]							DATA[15:0]																
R60	R/W	0	1	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3C4000h
R58	R/W	0	1	1	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	3A0C00h
R53	R/W	0	1	1	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	352802h
R47	R/W	0	1	0	1	1	1	1	0	DITHERING		0	0	0	0	0	0	0	0	0	0	0	0	0	2F0000h
R42	R/W	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	EXTVCO_CP_POL	EXTVCO_CP_IDN					2A0210h
R41	R/W	0	1	0	1	0	0	1	0	0	0	0	EXTVCO_CP_IUP					EXTVCO_CP_GAIN		CP_IDN					290810h
R40	R/W	0	1	0	1	0	0	0	0	0	0	CP_IUP					CP_GAIN		0	1	1	1	0	0	28101Ch
R39	R/W	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1	1	1	1	1	SDO_LD_SEL	0	1	LD_EN	2711F0h
R35	R/W	0	1	0	0	0	1	1	0	0	MULT_WAIT											OUTBUF_AUTO_MUTE	OUTBUF_TX_TYPE	OUTBUF_RX_TYPE	230647h
R34	R/W	0	1	0	0	0	1	0	IPBUF DIFF_TERM	IPBUF_SE_DIFF_SEL	XTAL_PWRCTRL			XTAL_EN	0	FSK_I2S_FS_POL	FSK_I2S_CLK_POL	FSK_LEVEL		FSK_DEV_SEL			FSK_MODE_SEL0	FSK_MODE_SEL1	221000h
R33	R/W	0	1	0	0	0	0	1	FSK_DEV_SPI_FAST																210000h
R32	R/W	0	1	0	0	0	0	0	FSK_DEV7_F2																200000h
R31	R/W	0	0	1	1	1	1	1	FSK_DEV6_F2																1F0000h
R30	R/W	0	0	1	1	1	1	0	FSK_DEV5_F2																1E0000h
R29	R/W	0	0	1	1	1	0	1	FSK_DEV4_F2																1D0000h
R28	R/W	0	0	1	1	1	0	0	FSK_DEV3_F2																1C0000h
R27	R/W	0	0	1	1	0	1	1	FSK_DEV2_F2																1B0000h
R26	R/W	0	0	1	1	0	1	0	FSK_DEV1_F2																1A0000h
R25	R/W	0	0	1	1	0	0	1	FSK_DEV0_F2																190000h
R24	R/W	0	0	1	1	0	0	0	0	0	0	0	0	FSK_EN_F2	EXTVCO_CHDIV_F2				EXTVCO_SEL_F2	OUTBUF_TX_PWR_F2					180010h
R23	R/W	0	0	1	0	1	1	1	0	0	0	OUTBUF_RX_PWR_F2					OUTBUF_TX_EN_F2	OUTBUF_RX_EN_F2	0	0	0	LF_R4_F2			1710A4h
R22	R/W	0	0	1	0	1	1	0	LF_R3_F2			CHDIV2_F2			CHDIV1_F2		PFD_DELAY_F2			MULT_F2					168584h
R21	R/W	0	0	1	0	1	0	1	PLL_R_F2								PLL_R_PRE_F2								150101h
R20	R/W	0	0	1	0	1	0	0	PLL_N_PRE_F2	FRAC_ORDER_F2			PLL_N_F2												140028h
R19	R/W	0	0	1	0	0	1	1	PLL_DEN_F2[15:0]																130000h
R18	R/W	0	0	1	0	0	1	0	PLL_NUM_F2[15:0]																120000h
R17	R/W	0	0	1	0	0	0	1	PLL_DEN_F2[23:16]								PLL_NUM_F2[23:16]								110000h
R16	R/W	0	0	1	0	0	0	0	FSK_DEV7_F1																100000h
R15	R/W	0	0	0	1	1	1	1	FSK_DEV6_F1																F0000h
R14	R/W	0	0	0	1	1	1	0	FSK_DEV5_F1																E0000h

Register Maps (continued)

REG.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	R/W	ADDRESS[6:0]							DATA[15:0]																
R13	R/W	0	0	0	1	1	0	1	FSK_DEV4_F1																D0000h
R12	R/W	0	0	0	1	1	0	0	FSK_DEV3_F1																C0000h
R11	R/W	0	0	0	1	0	1	1	FSK_DEV2_F1																B0000h
R10	R/W	0	0	0	1	0	1	0	FSK_DEV1_F1																A0000h
R9	R/W	0	0	0	1	0	0	1	FSK_DEV0_F1																90000h
R8	R/W	0	0	0	1	0	0	0	0	0	0	0	0	FSK_EN_F1	EXTVCO_CHDIV_F1				EXTVCO_SEL_F1	OUTBUF_TX_PWR_F1					80010h
R7	R/W	0	0	0	0	1	1	1	0	0	0	OUTBUF_RX_PWR_F1					OUTBUF_TX_EN_F1	OUTBUF_RX_EN_F1	0	0	0	LF_R4_F1			710A4h
R6	R/W	0	0	0	0	1	1	0	LF_R3_F1			CHDIV2_F1			CHDIV1_F1		PFD_DELAY_F1			MULT_F1					68584h
R5	R/W	0	0	0	0	1	0	1	PLL_R_F1								PLL_R_PRE_F1								50101h
R4	R/W	0	0	0	0	1	0	0	PLL_N_PRE_F1	FRAC_ORDER_F1			PLL_N_F1												40028h
R3	R/W	0	0	0	0	0	1	1	PLL_DEN_F1[15:0]																30000h
R2	R/W	0	0	0	0	0	1	0	PLL_NUM_F1[15:0]																20000h
R1	R/W	0	0	0	0	0	0	1	PLL_DEN_F1[23:16]								PLL_NUM_F1[23:16]								10000h
R0	R/W	0	0	0	0	0	0	0	0	0	RESET	POWER DOWN	RXTX_CTRL	RXTX_POL	F1F2_INIT	F1F2_CTRL	F1F2_MODE	F1F2_SEL	0	0	0	0	1	FCAL_EN	3h

The POR value is the power-on reset value that is assigned when the device is powered up or the RESET bit is asserted. POR is not a default working mode, all registers are required to program properly in order to make the device works as desired.

7.6.1 R60 Register (offset = 3Ch) [reset = 4000h]

Figure 20. R60 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-4000h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0		R/W	4000h	Program A000h to this field.

7.6.2 R58 Register (offset = 3Ah) [reset = C00h]

Figure 21. R58 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
R/W-C00h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0		R/W	C00h	Program 8C00h to this field.

7.6.3 R53 Register (offset = 35h) [reset = 2802h]

Figure 22. R53 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0
R/W-2802h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0		R/W	2802h	Program 7806h to this field.

7.6.4 R47 Register (offset = 2Fh) [reset = 0h]

Figure 23. R47 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DITHERING		0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h		R/W-0h												

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
15		R/W	0h	Program 0h to this field.
14-13	DITHERING	R/W	0h	Set the level of dithering. This feature is used to mitigate spurs level in certain use case by increasing the level of randomness in the Delta Sigma modulator, typically done at the expense of noise at certain offset. 0 = Disabled 1 = Weak 2 = Medium 3 = Strong
12-0		R/W	0h	Program 0h to this field.

7.6.5 R42 Register (offset = 2Ah) [reset = 210h]

Figure 24. R42 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	EXTVCO_CP_POL	EXTVCO_CP_IDN				
R/W-8h										R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6		R/W	8h	Program 8h to this field.
5	EXTVCO_CP_POL	R/W	0h	Sets the phase detector polarity for external VCO in PLL mode operation. Positive means VCO frequency increases directly proportional to Vtune voltage. 0 = Positive 1 = Negative
4-0	EXTVCO_CP_IDN	R/W	10h	Set the base charge pump current for external VCO in PLL mode operation. The total base charge pump current is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. EXTVCO_CP_IDN must be equal to EXTVCO_CP_IUP. Only even number values are supported. 0 = Tri-state 2 = 312.5 µA 4 = 625 µA ... 30 = 3437.5 µA

7.6.6 R41 Register (offset = 29h) [reset = 810h]

Figure 25. R41 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	EXTVCO_CP_IUP					EXTVCO_CP_GAIN		CP_IDN				
R/W-0h				R/W-10h					R/W-0h		R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12		R/W	0h	Program 0h to this field.
11-7	EXTVCO_CP_IUP	R/W	10h	Set the base charge pump current for external VCO in PLL mode operation. The total base charge pump current is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. EXTVCO_CP_IDN must be equal to EXTVCO_CP_IUP. Only even number values are supported. 0 = Tri-state 2 = 312.5 µA 4 = 625 µA ... 30 = 3437.5 µA
6-5	EXTVCO_CP_GAIN	R/W	0h	Set the multiplication factor to the base charge pump current for external VCO in PLL mode operation. For example, if the gain here is 2x and if the total base charge pump current (EXTVCO_CP_IDN + EXTVCO_CP_IUP) is 2.5 mA, then the final charge pump current applied to the loop filter is 5 mA. The gain values are not precise. They are provided as a quick way to boost the total charge pump current for debug purposes or specific applications. 0 = 1x 1 = 2x 2 = 1.5x 3 = 2.5x
4-0	CP_IDN	R/W	10h	Set the base charge pump current for internal VCO in synthesizer mode operation. The total base charge pump current is equal to CP_IDN + CP_IUP. CP_IDN must be equal to CP_IUP. 0 = Tri-state 1 = 156.25 µA 2 = 312.5 µA 3 = 468.75 µA ... 31 = 3593.75 µA

7.6.7 R40 Register (offset = 28h) [reset = 101Ch]

Figure 26. R40 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	CP_IUP					CP_GAIN		0	1	1	1	0	0
R/W-0h			R/W-10h					R/W-0h		R/W-1Ch					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13		R/W	0h	Program 0h to this field.
12-8	CP_IUP	R/W	10h	Set the base charge pump current for internal VCO in synthesizer mode operation. The total base charge pump current is equal to CP_IDN + CP_IUP. CP_IDN must be equal to CP_IUP. 0 = Tri-state 1 = 156.25 µA 2 = 312.5 µA 3 = 468.75 µA ... 31 = 3593.75 µA
7-6	CP_GAIN	R/W	0h	Set the multiplication factor to the base charge pump current for internal VCO in synthesizer mode operation. For example, if the gain here is 2x and if the total base charge pump current (CP_IDN + CP_IUP) is 2.5 mA, then the final charge pump current applied to the loop filter is 5 mA. The gain values are not precise. They are provided as a quick way to boost the total charge pump current for debug purposes or specific applications. 0 = 1x 1 = 2x 2 = 1.5x 3 = 2.5x
5-0		R/W	1Ch	Program 1Ch to this field.

7.6.8 R39 Register (offset = 27h) [reset = 11F0h]

Figure 27. R39 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1	1	1	1	1	SDO_LD_SEL	0	1	LD_EN
R/W-11Fh												R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4		R/W	11Fh	Program 11Fh to this field.
3	SDO_LD_SEL	R/W	0h	Defines the MUXout pin function. 0 = Register readback serial data output 1 = Lock detect output
2-1		R/W	0h	Program 1h to this field.

Table 8. R39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LD_EN	R/W	0h	Enables lock detect function. 0 = Disabled 1 = Enabled

7.6.9 R35 Register (offset = 23h) [reset = 647h]

Figure 28. R35 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	MULT_WAIT											OUTBUF_AUTOMUTE	OUTBUF_TX_TYPE	OUTBUF_RX_TYPE
R/W-0h		R/W-C8h											R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14		R/W	0h	Program 0h to this field.
13-3	MULT_WAIT	R/W	C8h	A 20-µs settling time is required for MULT, if it is enabled. These bits set the correct settling time according to the OSCin frequency. For example, if OSCin frequency is 100 MHz, set these bits to 2000. No matter if MULT is enabled or not, the configured MULT settling time forms part of the total frequency switching time. 0 = Do not use this setting 1 = 1 OSCin clock cycle ... 2047 = 2047 OSCin clock cycles
2	OUTBUF_AUTOMUTE	R/W	1h	If this bit is set, the output buffers will be muted until PLL is locked. This bit applies to the following events: (a) device initialization (b) manually change VCO frequency, and (c) F1F2 switching. However, if the PLL is unlocked afterward (for example, OSCin is removed), the output buffers will not be muted and will remain active. 0 = Disabled 1 = Enabled
1	OUTBUF_TX_TYPE	R/W	1h	Sets the output buffer type of RFoutTx. If the buffer is open drain output, a pullup to VccIO is required. See RF Output Buffer Type for details. 0 = Open drain 1 = Push pull
0	OUTBUF_RX_TYPE	R/W	1h	Sets the output buffer type of RFoutRx. If the buffer is open drain output, a pullup to VccIO is required. See RF Output Buffer Type for details. 0 = Open drain 1 = Push pull

7.6.10 R34 Register (offset = 22h) [reset = 1000h]

Figure 29. R34 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPBUFDIFF_TERM	IPBUF_SE_DIFF_SEL	XTAL_PWRCTRL			XTAL_EN	0	FSK_I2S_FS_POL	FSK_I2S_CLK_POL	FSK_LEVEL		FSK_DEV_SEL			FSK_MODE_SEL0	FSK_MODE_SEL1
R/W-0h	R/W-0h	R/W-2h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	IPBUFDIFF_TERM	R/W	0h	Enables independent 50 Ω input termination on both OSCin and OSCin* pins. This function is valid even if OSCin input is configured as single-ended input. 0 = Disabled 1 = Enabled
14	IPBUF_SE_DIFF_SEL	R/W	0h	Selects between single-ended and differential OSCin input. 0 = Single-ended input 1 = Differential input
13-11	XTAL_PWRCTRL	R/W	2h	Set the value of the series resistor being used to limit the power dissipation through the crystal when crystal is being used as OSCin input. See OSCin Configuration for details. 0 = 0 Ω 1 = 100 Ω 2 = 200 Ω 3 = 300 Ω 4-7 = Reserved
10	XTAL_EN	R/W	0h	Enables the crystal oscillator buffer for use as OSCin input. This bit will overwrite IPBUF_SE_DIFF_SEL. 0 = Disabled 1 = Enabled
9		R/W	0h	Program 0h to this field.
8	FSK_I2S_FS_POL	R/W	0h	Sets the polarity of the I2S Frame Sync input in FSK I2S mode. 0 = Active HIGH 1 = Active LOW
7	FSK_I2S_CLK_POL	R/W	0h	Sets the polarity of the I2S CLK input in FSK I2S mode. 0 = Rising edge strobe 1 = Falling edge strobe
6-5	FSK_LEVEL	R/W	0h	Define the desired FSK level in FSK PIN mode and FSK SPI mode. When this bit is zero, FSK operation in these modes is disabled even if FSK_EN_Fx = 1. 0 = Disabled 1 = 2FSK 2 = 4FSK 3 = 8FSK
4-2	FSK_DEV_SEL	R/W	0h	In FSK SPI mode, these bits select one of the FSK deviations as defined in registers R25-32 or R9-16. 0 = FSK_DEV0_Fx 1 = FSK_DEV1_Fx ... 7 = FSK_DEV7_Fx

Table 10. R34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FSK_MODE_SEL0	R/W	0h	FSK_MODE_SEL0 and FSK_MODE_SEL1 define the FSK operation mode. FSK_MODE_SEL[1:0] = 00 = FSK PIN mode 01 = FSK SPI mode 10 = FSK I2S mode 11 = FSK SPI FAST mode
0	FSK_MODE_SEL1	R/W	0h	Same as above.

7.6.11 R33 Register (offset = 21h) [reset = 0h]

Figure 30. R33 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV_SPI_FAST															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FSK_DEV_SPI_FAST	R/W	0h	Define the desired frequency deviation in FSK SPI FAST mode. See Direct Digital FSK Modulation for details.

7.6.12 R25 to R32 Register (offset = 19h to 20h) [reset = 0h]

Figure 31. R25 to R32 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV0_F2 to FSK_DEV7_F2															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. R25 to R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FSK_DEV0_F2 to FSK_DEV7_F2	R/W	0h	Define the desired frequency deviation in FSK PIN mode and FSK SPI mode. See Direct Digital FSK Modulation for details.

7.6.13 R24 Register (offset = 18h) [reset = 10h]

Figure 32. R24 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	FSK_EN_F2	EXTVCO_CHDIV_F2				EXTVCO_SEL_F2	OUTBUF_TX_PWR_F2				
R/W-0h					R/W-0h	R/W-0h				R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11		R/W	0h	Program 0h to this field.
10	FSK_EN_F2	R/W	0h	Enables FSK operation in all FSK operation modes. When this bit is set, fractional denominator DEN should be zero. See Direct Digital FSK Modulation for details. 0 = Disabled 1 = Enabled
9-6	EXTVCO_CHDIV_F2	R/W	0h	Set the value of the output channel divider, CHDIV3, when using external VCO in PLL mode. 0 = Divide by 1 1 = Reserved 2 = Divide by 2 3 = Divide by 3 ... 10 = Divide by 10 11-15 = Reserved
5	EXTVCO_SEL_F2	R/W	0h	Selects synthesizer mode (internal VCO) or PLL mode (external VCO) operation. 0 = Synthesizer mode 1 = PLL mode
4-0	OUTBUF_TX_PWR_F2	R/W	10h	Set the output power at RFoutTx port. See RF Output Buffer Power Control for details.

7.6.14 R23 Register (offset = 17h) [reset = 10A4h]

Figure 33. R23 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OUTBUF_RX_PWR_F2					OUTBUF_TX_EN_F2	OUTBUF_RX_EN_F2	0	0	0	LF_R4_F2		
R/W-0h			R/W-10h					R/W-1h	R/W-0h	R/W-4h			R/W-4h		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13		R/W	0h	Program 0h to this field.
12-8	OUTBUF_RX_PWR_F2	R/W	10h	Set the output power at RFoutRx port. See RF Output Buffer Power Control for details.
7	OUTBUF_TX_EN_F2	R/W	1h	Enables RFoutTx port. 0 = Disabled 1 = Enabled
6	OUTBUF_RX_EN_F2	R/W	0h	Enables RFoutRx port. 0 = Disabled 1 = Enabled
5-3		R/W	4h	Program 0h to this field.
2-0	LF_R4_F2	R/W	4h	Set the resistor value for the 4th pole of the internal loop filter. The shunt capacitor of that pole is 100 pF. 0 = Bypass 1 = 3.2 kΩ 2 = 1.6 kΩ 3 = 1.1 kΩ 4 = 800 Ω 5 = 640 Ω 6 = 533 Ω 7 = 457 Ω

7.6.15 R22 Register (offset = 16h) [reset = 8584h]

Figure 34. R22 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LF_R3_F2			CHDIV2_F2			CHDIV1_F2		PFD_DELAY_F2			MULT_F2				
R/W-4h			R/W-1h			R/W-1h		R/W-4h			R/W-4h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. R22 Register Descriptions

Bit	Field	Type	Reset	Description
15-13	LF_R3_F2	R/W	4h	Set the resistor value for the 3rd pole of the internal loop filter. The shunt capacitor of that pole is 50 pF. 0 = Bypass 1 = 3.2 kΩ 2 = 1.6 kΩ 3 = 1.1 kΩ 4 = 800 Ω 5 = 640 Ω 6 = 533 Ω 7 = 457 Ω

Table 15. R22 Register Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	CHDIV2_F2	R/W	1h	Set the value of the output channel divider, CHDIV2, when using internal VCO in synthesizer mode. 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3 = Divide by 8 4 = Divide by 16 5 = Divide by 32 6 = Divide by 64
9-8	CHDIV1_F2	R/W	1h	Set the value of the output channel divider, CHDIV1, when using internal VCO in synthesizer mode. 0 = Divide by 4 1 = Divide by 5 2 = Divide by 6 3 = Divide by 7
7-5	PFD_DELAY_F2	R/W	4h	Used to optimize spurs and phase noise. Suggested values are: Integer mode (NUM = 0): use PFD_DELAY ≤ 5 Fractional mode with N-divider < 22: use PFD_DELAY ≤ 4 Fractional mode with N-divider ≥ 22: use PFD_DELAY ≥ 3
4-0	MULT_F2	R/W	4h	Set the MULT multiplier value. MULT value must be greater than Pre-divider value. MULT is not supported when crystal is being used as the reference clock input. See MULT Multiplier for details. 0 = Reserved 1 = Bypass 2 = 2x ... 13 = 13x 14-31 = Reserved

7.6.16 R21 Register (offset = 15h) [reset = 101h]

Figure 35. R21 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_R_F2								PLL_R_PRE_F2							
R/W-1h								R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. R21 Register Descriptions

Bit	Field	Type	Reset	Description
15-8	PLL_R_F2	R/W	1h	Set the OSCin buffer Post-divider value.
7-0	PLL_R_PRE_F2	R/W	1h	Set the OSCin buffer Pre-divider value. This value must be smaller than MULT value.

7.6.17 R20 Register (offset = 14h) [reset = 28h]

Figure 36. R20 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N_PRE_F2	FRAC_ORDER_F2			PLL_N_F2											
R/W-0h	R/W-0h			R/W-28h											

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. R20 Register Descriptions

Bit	Field	Type	Reset	Description
15	PLL_N_PRE_F2	R/W	0h	Sets the Prescaler value. 0 = Divide by 2 1 = Divide by 4
14-12	FRAC_ORDER_F2	R/W	0h	Select the order of the Delta Sigma modulator. 0 = Integer mode 1 = 1st order 2 = 2nd order 3 = 3rd order 4-7 = 4th order
11-0	PLL_N_F2	R/W	28h	Set the integer portion of the N-divider value. Maximum value is 1023.

7.6.18 R19 Register (offset = 13h) [reset = 0h]

Figure 37. R19 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F2[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN_F2[15:0]	R/W	0h	Set the LSB bits of the fractional denominator of the N-divider.

7.6.19 R18 Register (offset = 12h) [reset = 0h]

Figure 38. R18 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM_F2[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM_F2[15:0]	R/W	0h	Set the LSB bits of the fractional numerator of the N-divider.

7.6.20 R17 Register (offset = 11h) [reset = 0h]

Figure 39. R17 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F2[23:16]								PLL_NUM_F2[23:16]							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. R17 Register Descriptions

Bit	Field	Type	Reset	Description
15-8	PLL_DEN_F2[23:16]	R/W	0h	Set the MSB bits of the fractional denominator of the N-divider.
7-0	PLL_NUM_F2[23:16]	R/W	0h	Set the MSB bits of the fractional numerator of the N-divider.

7.6.21 R9 to R16 Register (offset = 9h to 10h) [reset = 0h]

Figure 40. R9 to R16 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV0_F1 to FSK_DEV7_F1															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. R9 to R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FSK_DEV0_F1 to FSK_DEV7_F1	R/W	0h	See Table 12.

7.6.22 R8 Register (offset = 8h) [reset = 10h]

Figure 41. R8 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	FSK_EN_F1	EXTVCO_CHDIV_F1				EXTVCO_SEL_F1	OUTBUF_TX_PWR_F1				
R/W-0h					R/W-0h	R/W-0h				R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11		R/W	0h	Program 0h to this field.
10	FSK_EN_F1	R/W	0h	See Table 13.
9-6	EXTVCO_CHDIV_F1	R/W	0h	See Table 13.
5	EXTVCO_SEL_F1	R/W	0h	See Table 13.
4-0	OUTBUF_TX_PWR_F1	R/W	10h	See Table 13.

7.6.23 R7 Register (offset = 7h) [reset = 10A4h]

Figure 42. R7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OUTBUF_RX_PWR_F1					OUTBUF_TX_EN_F1	OUTBUF_RX_EN_F1	0	0	0	LF_R4_F1		
R/W-0h			R/W-10h					R/W-1h	R/W-0h	R/W-4h			R/W-4h		

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13		R/W	0h	Program 0h to this field.
12-8	OUTBUF_RX_PWR_F1	R/W	10h	See Table 14.
7	OUTBUF_TX_EN_F1	R/W	1h	See Table 14.
6	OUTBUF_RX_EN_F1	R/W	0h	See Table 14.
5-3		R/W	4h	Program 0h to this field.
2-0	LF_R4_F1	R/W	4h	See Table 14.

7.6.24 R6 Register (offset = 6h) [reset = 8584h]

Figure 43. R6 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LF_R3_F1			CHDIV2_F1			CHDIV1_F1		PFD_DELAY_F1			MULT_F1				
R/W-4h			R/W-1h			R/W-1h		R/W-4h			R/W-4h				

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 24. R6 Register Descriptions

Bit	Field	Type	Reset	Description
15-13	LF_R3_F1	R/W	4h	See Table 15.
12-10	CHDIV2_F1	R/W	1h	See Table 15.
9-8	CHDIV1_F1	R/W	1h	See Table 15.
7-5	PFD_DELAY_F1	R/W	4h	See Table 15.
4-0	MULT_F1	R/W	4h	See Table 15.

7.6.25 R5 Register (offset = 5h) [reset = 101h]

Figure 44. R5 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_R_F1								PLL_R_PRE_F1							
R/W-1h								R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 25. R5 Register Descriptions

Bit	Field	Type	Reset	Description
15-8	PLL_R_F1	R/W	1h	See Table 16.
7-0	PLL_R_PRE_F1	R/W	1h	See Table 16.

7.6.26 R4 Register (offset = 4h) [reset = 28h]

Figure 45. R4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N_PRE_F1	FRAC_ORDER_F1			PLL_N_F1											
R/W-0h	R/W-0h			R/W-28h											

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 26. R4 Register Descriptions

Bit	Field	Type	Reset	Description
15	PLL_N_PRE_F1	R/W	0h	See Table 17.
14-12	FRAC_ORDER_F1	R/W	0h	See Table 17.
11-0	PLL_N_F1	R/W	28h	See Table 17.

7.6.27 R3 Register (offset = 3h) [reset = 0h]

Figure 46. R3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F1[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 27. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN_F1[15:0]	R/W	0h	See Table 18.

7.6.28 R2 Register (offset = 2h) [reset = 0h]

Figure 47. R2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM_F1[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 28. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM_F1[15:0]	R/W	0h	See Table 19.

7.6.29 R1 Register (offset = 1h) [reset = 0h]

Figure 48. R1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F1[23:16]								PLL_NUM_F1[23:16]							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 29. R1 Register Descriptions

Bit	Field	Type	Reset	Description
15-8	PLL_DEN_F1[23:16]	R/W	0h	See Table 20.
7-0	PLL_NUM_F1[23:16]	R/W	0h	See Table 20.

7.6.30 R0 Register (offset = 0h) [reset = 3h]

Figure 49. R0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RESET	POWERDOWN	RXTX_CTRL	RXTX_POL	F1F2_INIT	F1F2_CTRL	F1F2_MODE	F1F2_SEL	0	0	0	0	1	FCAL_EN
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h					R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 30. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14		R/W	0h	Program 0h to this field.
13	RESET	R/W	0h	Resets all the registers to the default values. This bit is self-clearing. 0 = Normal operation 1 = Reset
12	POWERDOWN	R/W	0h	Powers down the device. When the device comes out of the powered down state, either by resuming this bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), it is required that register R0 with FCAL_EN = 1 be programmed again to re-calibrate the device. A 100-µs wait-time is recommended before programming R0. 0 = Normal operation 1 = Power down
11	RXTX_CTRL	R/W	0h	Sets the control mode of TX/RX switching. 0 = Switching is controlled by register programming 1 = Switching is controlled by toggling the TrCtl pin
10	RXTX_POL	R/W	0h	Defines the polarity of the TrCtl pin. 0 = Active LOW = TX 1 = Active HIGH = TX
9	F1F2_INIT	R/W	0h	Toggling this bit re-calibrates F1F2 if F1, F2 are modified after calibration. This bit is not self-clear, so it is required to clear the bit value after use. See Register R0 F1F2_INIT, F1F2_MODE usage for details. 0 = Clear bit value 1 = Re-calibrate
8	F1F2_CTRL	R/W	0h	Sets the control mode of F1/F2 switching. Switching by TrCtl pin requires F1F2_MODE = 1. 0 = Switching is controlled by register programming 1 = Switching is controlled by toggling the TrCtl pin
7	F1F2_MODE	R/W	0h	Calibrates F1 and F2 during device initialization (initial power on programming). It also enables F1-F2 switching with the TrCtl pin. Even if this bit is not set, F1-F2 switching is still possible but the first switching time will not be optimized because either F1 or F2 will only be calibrated. If F1-F2 switching is not required, set this bit to zero. See Register R0 F1F2_INIT, F1F2_MODE usage for details. 0 = Disable F1F2 calibration 1 = Enable F1F2 calibration
6	F1F2_SEL	R/W	0h	Selects F1 or F2 configuration registers. 0 = F1 registers 1 = F2 registers
5-1		R/W	1h	Program 1h to this field.
0	FCAL_EN	R/W	1h	Activates all kinds of calibrations, suggest keep it enabled all the time. If it is desired that the R0 register be programmed without activating this calibration, then this bit can be set to zero. 0 = Disabled 1 = Enabled

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Direct Digital FSK Modulation

In fractional mode, the finest delta frequency difference between two programmable output frequencies is equal to

$$f_1 – f_2 = \Delta f_{min} = f_{PD} * \{[(N + 1) / DEN] – (N / DEN)\} = f_{PD} / DEN \quad (3)$$

In other words, when the fractional numerator is incremented by 1 (one step), the output frequency will change by Δf_{min}. A two steps increment will therefore change the frequency by 2 * Δf_{min}.

In FSK operation, the instantaneous carrier frequency is kept changing among some pre-defined frequencies. In general, the instantaneous carrier frequency is defined as a certain frequency deviation from the nominal carrier frequency. The frequency deviation could be positive and negative.

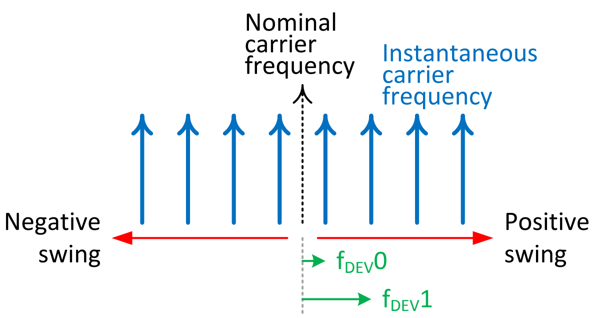


Figure 50. General FSK Definition

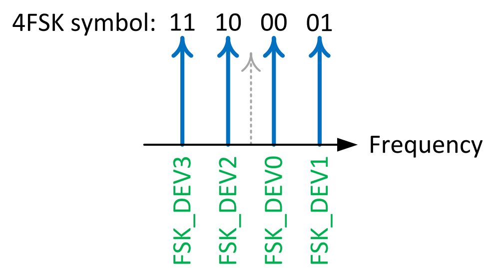


Figure 51. Typical 4FSK Definition

The following equations define the number of steps required for the desired frequency deviation with respect to the nominal carrier frequency output at the RFoutTx or RFoutRx port.

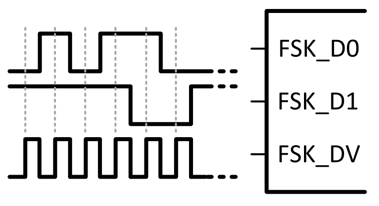
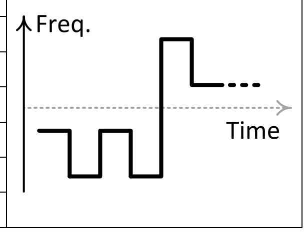
Table 31. FSK Step Equations

POLARITY	SYNTHESIZER MODE	PLL MODE
POSITIVE SWING	$\text{Round}\left(\frac{f_{DEV} * DEN}{f_{PD}} * \frac{CHDIV1 * CHDIV2}{Prescaler}\right)$ (4)	$\text{Round}\left(\frac{f_{DEV} * DEN}{f_{PD}} * CHDIV3\right)$ (5)
NEGATIVE SWING	2's complement of Equation 4 (6)	2's complement of Equation 5 (7)

In FSK PIN mode and FSK SPI mdoe, register R25-32 and R9-16 are used to store the desired FSK frequency deviations in term of the number of step as defined in the above equations. The order of the registers, 0 to 7, depends on the application system. A typical 4FSK definition is shown in Figure 51. In this case, FSK_DEV0_Fx and FSK_DEV1_Fx shall be calculated using Equation 4 or Equation 5 while FSK_DEV2_Fx and FSK_DEV3_Fx shall be calculated using Equation 6 or Equation 7.

For example, if FSK PIN mode is enabled in F1 to support 4FSK modulation, set
FSK_MODE_SEL1 = 0
FSK_MODE_SEL0 = 0
FSK_LEVEL = 2
FSK_EN_F1 = 1

Table 32. FSK PIN Mode Example

RAW FSK DATA STREAM INPUT	EQUIVALENT SYMBOL INPUT	REGISTER SELECTED	RF OUTPUT
	10	FSK_DEV2_F1	
	11	FSK_DEV3_F1	
	10	FSK_DEV2_F1	
	11	FSK_DEV3_F1	
	01	FSK_DEV1_F1	
	00	FSK_DEV0_F1	
	...	...	

FSK SPI mode assumes the user knows which symbol to send; user can directly write to register R34, FSK_DEV_SEL to select the desired frequency deviation.

For example, to enable the device to support 4FSK modulation at F1 using FSK SPI mode, set
FSK_MODE_SEL1 = 0
FSK_MODE_SEL0 = 1
FSK_LEVEL = 2
FSK_EN_F1 = 1

Table 33. FSK SPI Mode Example

DESIRED SYMBOL	WRITE REGISTER FSK_DEV_SEL	REGISTER SELECTED
10	2	FSK_DEV2_F1
11	3	FSK_DEV3_F1
10	2	FSK_DEV2_F1
11	3	FSK_DEV3_F1
01	1	FSK_DEV1_F1
00	0	FSK_DEV0_F1
...	...	...

Both the FSK PIN mode and FSK SPI mode support up to 8 levels of FSK. To support an arbitrary-level FSK, use FSK SPI FAST mode or FSK I2S mode. Constructing pulse-shaping FSK modulation by over-sampling the FSK modulation waveform is one of the use cases of these modes.

Analog-FM modulation can also be produced in these modes. For example, with a 1-kHz sine wave modulation signal with peak frequency deviation of ±2 kHz, the signal can be over-sampled, say 10 times. Each sample point corresponding to a scaled frequency deviation.

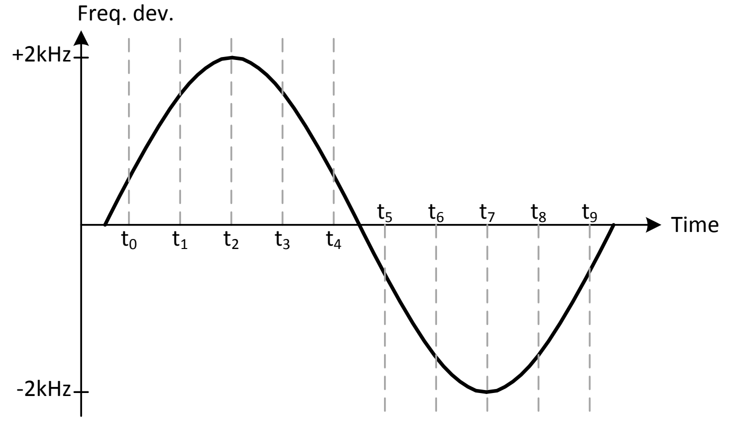


Figure 52. Over-Sampling Modulation Signal

In FSK SPI FAST mode, write the desired FSK steps directly to register R33, FSK_DEV_SPI_FAST. To enable this mode, set
FSK_MODE_SEL1 = 1
FSK_MODE_SEL0 = 1
FSK_EN_F1 = 1

Table 34. FSK SPI FAST Mode Example

TIME	FREQUENCY DEVIATION	CORRESPONDING FSK STEPS(1)	BINARY EQUIVALENT	WRITE TO FSK_DEV_SPI_FAST
t_0	618.034 Hz	518	0000 0010 0000 0110	518
t_1	1618.034 Hz	1357	0000 0101 0100 1101	1357
t_2	2000 Hz	1678	0000 0110 1000 1110	1678
…	…	…	…	…
t_6	–1618.034 Hz	64178	1111 1010 1011 0010	64178
t_7	–2000 Hz	63857	1111 1001 0111 0001	63857
…	…	…	…	…

(1) Synthesizer mode, f_{VCO} = 4800 MHz, f_{OUT} = 480 MHz, f_{PD} = 100 MHz, Prescaler = 2, DEN = 2^{24}, Use Equation 4 and Equation 6 to calculate the step value.

In FSK I2S mode, clock in the desired binary format FSK steps in the FSK_D1 pin.

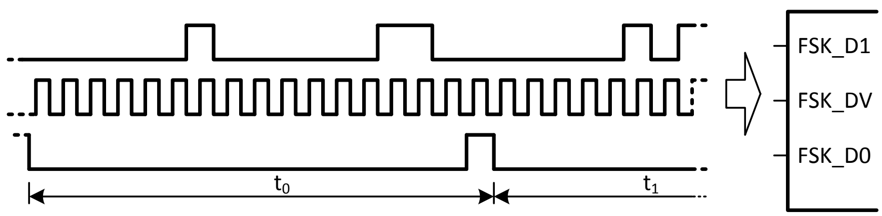


Figure 53. FSK I2S Mode Example

To enable FSK I2S mode, set
FSK_MODE_SEL1 = 1
FSK_MODE_SEL0 = 0
FSK_EN_F1 =1

8.1.2 Frequency and Output Port Switching with TrCtl Pin

Register R0, RXTX_CTRL, and RXTX_POL are used to define the output port switching behavior with the TrCtl pin. To enable switching with TrCtl pin, set RXTX_CTRL=1.

Table 35. TrCtl Pin Usage

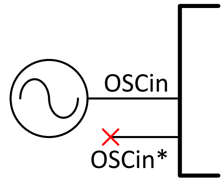
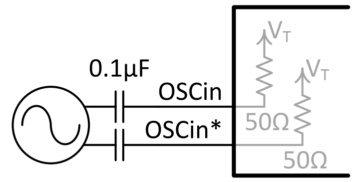
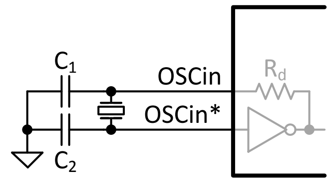
RXTX_CTRL	RXTX_POL	TrCtl PIN	RFoutTx	RFoutRx
1	0	0	Active	
1	0	1		Active
1	1	0		Active
1	1	1	Active	

Register R0, F1F2_CTRL, and F1F2_SEL define the operation of the frequency switching between the two pre-defined frequencies F1 and F2. To switch frequency using the TrCtl pin, set F1F2_CTRL to 1. F1F2_SEL selects the output frequency for the current status. For example, if the current active output frequency is F1, toggling TrCtl pin will change the output frequency to F2. Toggling TrCtl pin again will change the output frequency back to F1.

8.1.3 OSCin Configuration

OSCin supports single-end clock, differential clock as well as crystal. Register R34 defines OSCin configuration.

Table 36. OSCin Configuration

OSCin TYPE	SINGLE-ENDED CLOCK	DIFFERENTIAL CLOCK	CRYSTAL
Connection Diagram			
Register Setting	IPBUF_SE_DIFF_SEL = 0	IPBUF_SE_DIFF_SEL = 1 IPBUFDIFF_TERM = 1	XTAL_EN = 1 XTAL_PWRCTRL = Crystal dependent

Single-ended and differential input clock definitions are as follows:

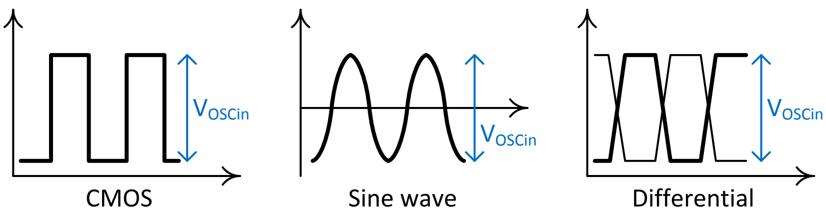


Figure 54. Input Clock Definition

The integrated crystal-oscillator circuit supports a fundamental mode, AT-cute crystal. The load capacitance, C_L, is specific to the crystal, but usually on the order of 18 to 20 pF. While C_L is specified for crystal, the OSCin input capacitance, C_{IN} (1 pF typical), of the device and PCB stray capacitance, C_{STRAY} (approximately 1 to 3 pF), can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (8)$$

Typically, $C_1 = C_2$ for optimum symmetry, so Equation 8 can be rewritten in terms of C_1 only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (9)$$

Finally, solve for C_1:

$$C_1 = 2 * (C_L – C_{IN} – C_{STRAY}) \quad (10)$$

Electrical Characteristics provide crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Over-driving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation. The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR} * (1 + C_o / C_L)^2$$

where

- I_{RMS} is the rms current through the crystal
- R_{ESR} is the maximum equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_o is the minimum shunt capacitance specified for the crystal
- I_{RMS} can be measured using a current probe (for example, Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCin pin with the oscillation circuit active. (11)

The internal configurable resistor, R_d, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_d shorted, then a larger resistor value is mandatory to avoid over-driving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_d shorted, then a zero value for R_d can be used. As a starting point, a suggested value for R_d is 200 Ω.

8.1.4 Register R0 F1F2_INIT, F1F2_MODE usage

These register bits are used to define the calibration behavior. Correct setting is important to ensure that every F1-F2 switching time is optimized. Figure 55 illustrates the usage of these register bits.

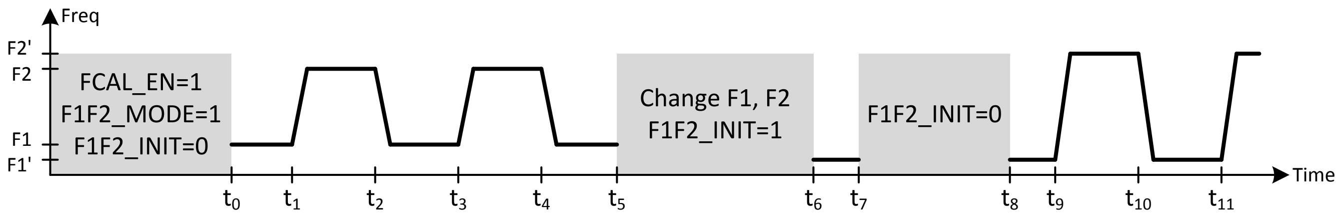


Figure 55. F1F2_INIT, F1F2_MODE Usage

Before t_0: Device initialization

- Power up the device.
- Write all registers to the device.
  - Ensure FCAL_EN = 1 to enable calibration.
  - Set F1F2_MODE = 1 to make both F1 and F2 being calibrated during initialization. If F1F2_MODE = 0, only the output frequency (F1 in this example) will be calibrated, F2 will not be calibrated. Furthermore, if F1F2 switching is triggered by the TrCtl pin, F1F2_MODE must be equal to 1.
  - Set F1F2_INIT = 0. Although the setting of this bit is irrelevant and not important here but if F1F2_INIT = 1, change it back to zero before attempting to change the frequency from F1 to F2.

At t_0: Locked to F1
After initialization, both F1 and F2 are calibrated. The calibration data is stored in the internal memory.

At t_1: Switch to F2.
Since FCAL_EN = 1, calibration will start over again when the output is switching from F1 to F2. F2 calibration begins based on the last calibration data, which is the calibration data obtained at t_0. If the environment (for example, temperature) does not change much, the new calibration data will be similar to the old data. As a result, the calibration time is minimal and therefore, the switching time will be short.

At t_2: Switch back to F1
Again, F1 calibration starts over and begins with the last calibration data as obtained at t_0. Calibration time is again very short, as is the switching time.

At t_3: Switch again to F2
This time, the calibration begins with the calibration data obtained at t_1, which is the last calibration data.

At t_4: Switch back to F1
Calibration begins with the calibration data obtained at t_2, which is the last calibration data.

At t_5: Set new F1, F2 frequency

- Write to the relevant registers to set the new F1 and F2 frequency (for example, change the N-divider values)
- Initiate calibration by re-writing register R0
  - Set F1F2_INIT=1. Both F1' and F2' will be calibrated

At t_6: Locked to F1'
F1' and F2' calibration completed and their calibration data are ready.

At t_7: Release F1F2_INIT bit
This bit has to be reset to zero or otherwise both F1' and F2' will be calibrated every time they are toggling.

At t_8: F1' calibration data is updated
Since F1F2_INIT is located in register R0, when writing F1F2_INIT = 0 to the device, calibration is once again triggered. However, only F1' will be re-calibrated, the calibration data of F2' remains unchanged.

At t_9: Switch to F2'
F2' calibration begins with the calibration data obtained at t_6, which is the last calibration data. Calibration time is again very short, as is the switching time.

At t_{10}: Switch back to F1'
F1' calibration starts over and begins with the last calibration data as obtained at t_8.

At t_{11}: Switch again to F2'
The calibration begins with the calibration data obtained at t_9, which is the last calibration data.

As illustrated above, register F1F2_INIT must be used properly in order to ensure that every F1-F2 switching time is optimized.

8.1.5 FastLock with External VCO

Fastlock may be required in PLL mode where an external VCO with a narrow loop bandwidth is desired. The LMX2571 adopts a new FastLock approach to support the very fast switching time requirement in PLL mode.

There are two control pins in the chip, FLout1 and FLout2. Each pin is used to control a SPST analog switch, S1 and S2. The loop filter value with or without FastLock is the same, except that with FastLock, one more C2 and two SPST switches are needed.

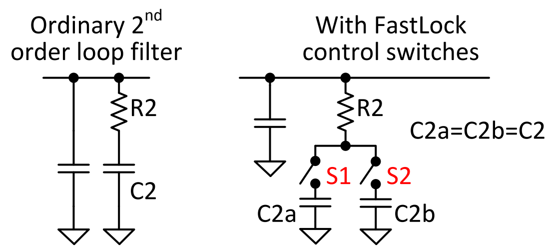


Figure 56. FastLock with SPST Switches

When LMX2571 is locked to F1, FLout1 will close the switch S1. When LMX2571 is locked to F2, either by toggling the TrCtl pin or program register R0, F1F2_SEL, S1 will be released while S2 will be closed by FLout2. Although S1 is released, the charge stored in C2a remains unchanged. Thus, when the output is switched back to F1, the Vtune voltage is almost correct, no (or little) charging or discharging to C2a is required which speeds up the switching time. For example, if Vtune for F1 and F2 are 1 V and 2 V, respectively, without FastLock, when the switching frequency shifts from F1 to F2, C2 will have to be re-charged from 1 V to 2 V — this is a big voltage jump. With FastLock, when S2 is closed, Vtune is almost equal to 2 V because C2b maintains the charge. Only a tiny voltage jump (re-charge) is required to make it reach the final Vtune voltage.

Figure 57 and Figure 58 compare the frequency switching time using different switching methods. In both cases, the loop bandwidth is 4 kHz while f_{PD} is 28 MHz. Figure 57 shows the switching time for a frequency jump from 430 MHz to 480 MHz with SPST switches. Frequency switching is toggled by the TrCtl pin. Switching time is approximately 1 ms. Frequency switching in Figure 58 is done in the traditional way. That is, change the output frequency by writing to the relevant registers such as N-divider values. In this case, because f_{PD} is very much bigger than the loop bandwidth, cycle slipping jeopardizes the switching time to more than 20 ms.

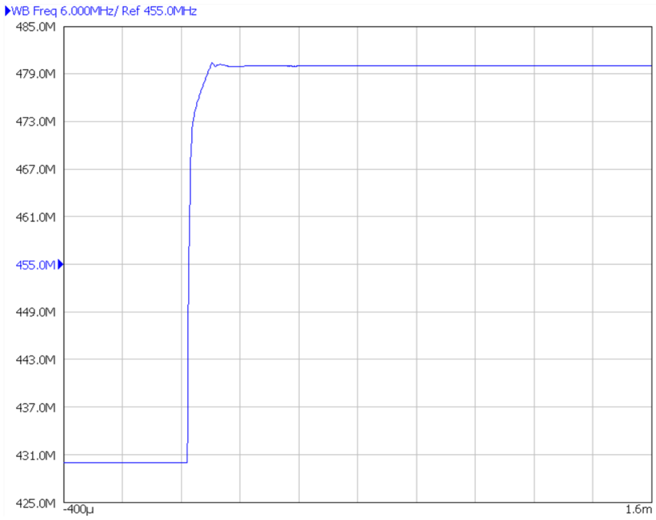


Figure 57. F1F2 Switching With SPST Switches

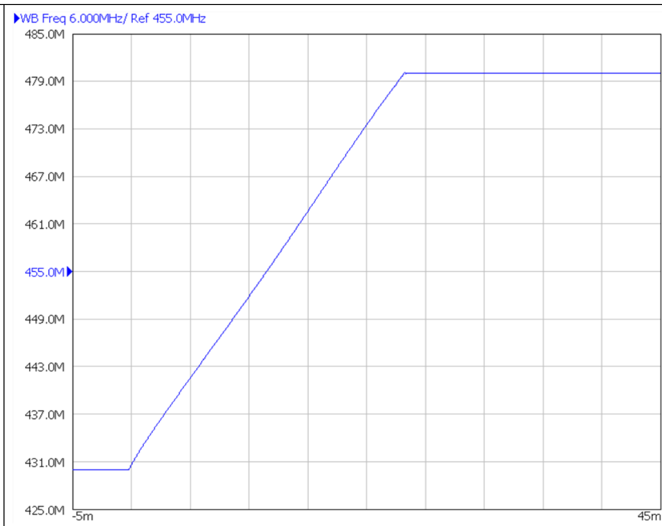


Figure 58. Change F1 Frequency Via SPI Programming

8.1.6 OSCin Slew Rate

A phase-lock loop consists of a clean reference clock, a PLL, and a VCO. Each of these contributes to the total phase noise. The LMX2571 is a high-performance PLL with integrated VCO. Both PLL noise and VCO noise are very good. Typical PLL 1/f noise and noise floor are –124 dBc/Hz and –231 dBc/Hz, respectively. To get the best possible phase-noise performance from the device the quality of the reference clock is very important because it may add noise to the loop. First of all, the phase noise of the reference clock must be good so that the final performance of the system is not degraded. Furthermore, using reference clock with a rather high slew rate (such as a square wave) is highly preferred. Driving the device input with a lower slew rate clock will degrade the device phase noise.

For a given frequency, a sine wave clock has the slowest slew rate, especially when the frequency is low. A CMOS clock or differential clock have much faster slew rates and are recommended. Figure 59 shows a phase-noise comparison with different types of reference clocks. Output frequency is 480 MHz while the input clock frequency is 26 MHz. As one can see there is a 5-dB difference in phase noise when using a clipped sine wave TCXO compared to a differential LVPECL clock. The internal crystal oscillator of the LMX2571 performance is also very good. If temperature compensation is not required, use crystal as the reference clock is a very good price-performance option.

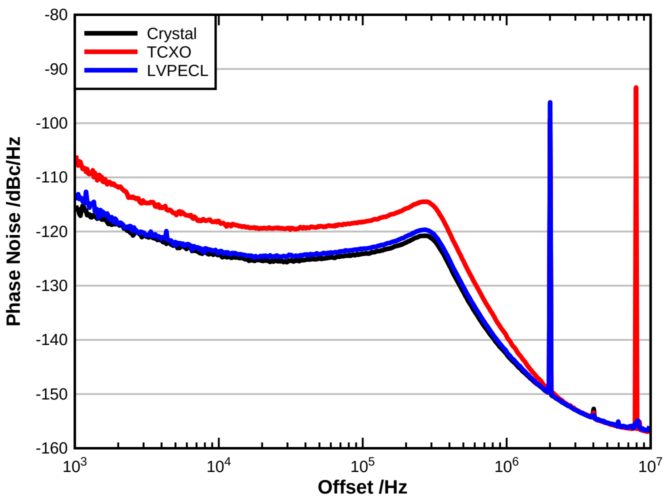


Figure 59. Phase Noise vs Input Clock

8.1.7 RF Output Buffer Power Control

Registers OUTBUF_TX_PWR_Fx and OUTBUF_RX_PWR_Fx are used to set the output power at the RFoutTx and RFoutRx ports. Figure 60 shows a typical output power vs power control bit plot in synthesizer mode. VCO frequency was 4800 MHz, and channel dividers were set to produce the shown output frequencies.

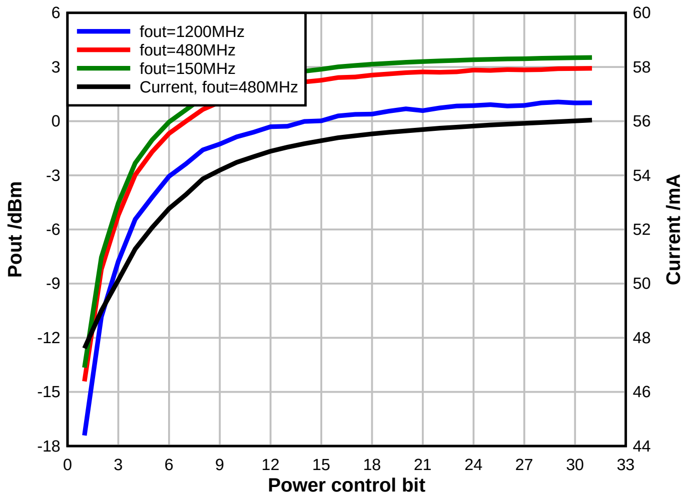
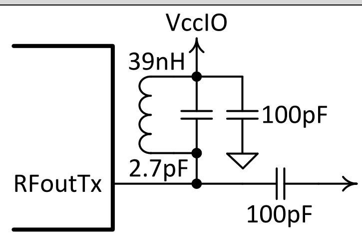
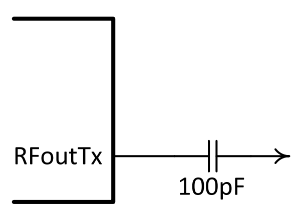


Figure 60. Configurable RF Output Power

8.1.8 RF Output Buffer Type

Registers R35, OUTBUF_TX_TYPE, OUTBUF_RX_TYPE are used to configure the RF output buffer type between open drain and push-pull. Push-pull is easy to use; all that is required is a DC-blocking capacitor at the output. The output waveform is square wave and therefore, harmonics rich. Open-drain output provides an option to reduce the harmonics using an LC resonant pullup network at its output. Table 37 summarizes an example an open-drain vs push-pull application.

Table 37. RF Output Buffer Type

BUFFER TYPE	OPEN DRAIN			PUSH-PULL		
Connection Diagram						
Output Power	470 MHz	480 MHz	490 MHz	470 MHz	480 MHz	490 MHz
f_o	2.7 dBm	2.8 dBm	2.8 dBm	–0.1 dBm	0 dBm	0.1 dBm
$2f_o$	–31 dBc	–30.7 dBc	–30.5 dBc	–30.4 dBc	–30.2 dBc	–30 dBc
$3f_o$	–17.3 dBc	–17.9 dBc	–18.1 dBc	–11.9 dBc	–12.1 dBc	–12.4 dBc
$4f_o$	–39 dBc	–40.4 dBc	–41.6 dBc	–28.5 dBc	–28.4 dBc	–28.1 dBc
$5f_o$	–18.1 dBc	–17.8 dBc	–17.6 dBc	–15.6 dBc	–15.6 dBc	–15.7 dBc
$6f_o$	–27.6 dBc	–27.2 dBc	–28.5 dBc	–29.5 dBc	–29.8 dBc	–29.3 dBc

Clearly, with a proper LC pull up in open drain architecture, the 3^{rd} to 5^{th} harmonics could be reduced.

8.1.9 MULT Multiplier

The main purpose of the multiplier, MULT, in the R–divider is to push the in-band fractional spurs far away from the carrier such that the spurs could be filtered out by the loop filter. In a fractional engine, the fractional spurs appear at a multiple of f_{PD} * N_{frac}. In cases where both f_{PD} and N_{frac} are small, the fractional spurs will appear very close to the carrier. These kinds of spurs are called in-band spurs.

Table 38. MULT Application Example

USE CASE	OSCin /MHz	PRE-DIVIDER	MULT	POST-DIVIDER	f_{PD} /MHz	VCO /MHz	$N_{integer}$	N_{frac}	SPURS /MHz
I	19.2	1	1	1	19.2	460.8	24	0	0
II	19.2	1	1	1	19.2	461	24	0.0104167	0.2
III	19.2	1	5	4	24	461	19	0.2083333	5

In Case I, the VCO frequency is an integer multiple of the f_{PD}, so N_{frac} is zero and there are no spurs. However, in Case II, the spur appears at an offset of 200 kHz. If this spur cannot be reduced by other typical spur-reduction techniques such as dithering, user can enable the MULT to overcome this problem. If the MULT is enabled as depicted in Case III, the spurs can be pushed to an offset of 5 MHz. In this case, the MULT together with the Post-divider changes the phase detector to a little bit higher frequency. As a consequence, the spurs are pushed further away from the carrier and are reduced more by the loop filter.

Another use case of MULT is to make higher phase-detector frequency. For example, if OSCin is 20 MHz, user can set MULT to 5 to make f_{PD} go to 100 MHz. As a result, the N-divider value will be reduced by 5 times; therefore, the PLL phase noise is reduced. A wide loop bandwidth can then be used to reduce the VCO noise. Consequently, the synthesizer close-in phase noise would be very good.

The MULT multiplier is an active device in nature, whenever it is enabled, it will add noise to the loop. For best phase noise performance, it is recommended to set MULT not greater than 6.

To use the MULT, beware of the restriction as indicated in the *Electrical Characteristics* table and Table 15.

8.1.10 Integrated VCO

The integrated VCO is composed of 3 VCO cores. The approximate frequency ranges for the three VCO cores with their gains is as follows:

Table 39. Approximate VCO Ranges and VCO Gain

VCO CORE	TYPICAL FREQUENCY RANGE (MHz)		TYPICAL VCO GAIN (MHz/V)		
	LOW	HIGH	LOW	MID	HIGH
VCOL	4200	4700	46	52	61
VCOM	4560	5100	50	56	65
VCOH	4920	5520	55	63	73

8.2 Typical Applications

8.2.1 Synthesizer Duplex Mode

In this example, the internal VCO is being used. The PLL will be put in fractional mode to support 4FSK direct digital modulation using FSK PIN mode. Both frequency (F1, F2) switching as well as RF output port switching is toggled by the TrCtl pin. MULT multiplier in the R-divider will be used to reduce spurs.

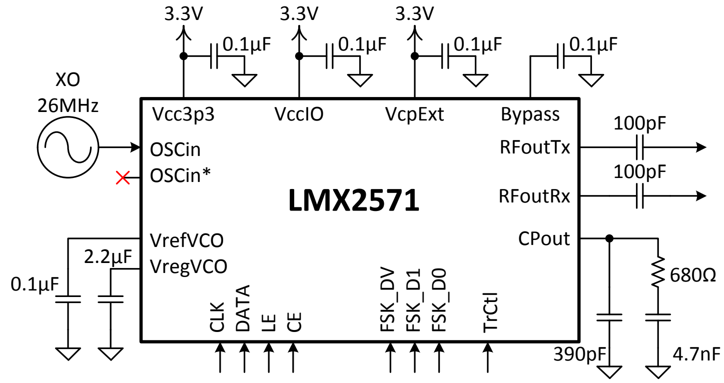


Figure 61. Typical Synthesizer Duplex Mode Application Schematic

8.2.1.1 Design Requirements

OSCin frequency = 26 MHz, LVCMOS
RFoutTx frequency = 902 MHz
RFoutRx frequency = 928 MHz
Frequency switching time ≤ 500 µs
4FSK modulation on TX, baud rate = 20 kSPs
Frequency deviation = ±10 kHz and ±30 kHz
FSK error ≤ 1 %
Spurs ≤ –72 dBc
Lock detect is required to indicate lock status
Output power < 1 dBm

8.2.1.2 Detailed Design Procedure

First of all, calculate all the frequencies in each functional block.

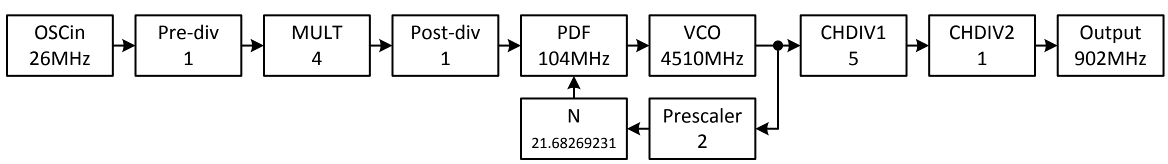


Figure 62. F1 Frequency Plan

Assign F1 frequency to be 902 MHz. With CHDIV1 = 5 and CHDIV2 = 1, the total division is 5. As a result, the VCO frequency will be 902 * 5 = 4510 MHz, which is within the VCO tuning range.

OSCin is 26 MHz, put Pre-divider = 1 to meet the MULT input frequency range requirement.

To meet the maximum MULT output frequency requirement, possible MULT values are 3 to 5. Play around the allowable MULT values and Post-divider values to get the optimum phase noise and spurs performance. Assuming MULT = 4 and Post-divider = 1 returns the best performance, then f_{PD} = 104 MHz.

N-divider = 21.68269231, that means $N_{integer}$ = 21 while N_{frac} = 0.68269231. To use the direct digital modulation feature, put fractional denominator, DEN = 0. The actual DEN value is, in fact, equal to 2^{24} = 16777216. So the fractional numerator, NUM, is equal to N_{frac} * DEN = 11453676.

Typical Applications (continued)

Use Equation 4 and Equation 6 to calculate the required FSK steps. For +10 kHz frequency deviation, the FSK step value is equal to [10000 * 16777216 / (104 * 10^6)] * (5 * 1 / 2) = 4033. For –10 kHz frequency deviation, the FSK step value is equal to 2's complement of 4033 = 61502. Similarly, the FSK step values for ±30 kHz frequency deviation are 12099 and 53436.

All the required configuration values for F2, 928 MHz can be calculated in the similar fashion and are summarized as follows:

Table 40. Frequency Plan Summary

CONFIGURATION PARAMETER	F1 (902 MHz)	F2 (928 MHz)
Pre-divider	1	1
MULT	4	4
Post-divider	1	1
PDF	104 MHz	104 MHz
VCO	4510 MHz	4640 MHz
N-divider	21.68269231	22.30769231
$N_{integer}$	21	22
DEN	0	0
NUM	11453676	5162220
CHDIV1	5	5
CHDIV2	1	1
FSK_DEV0	4033	
FSK_DEV1	12099	
FSK_DEV2	61502	
FSK_DEV3	53436	

Assume here that the base charge pump current = 1250 µA, CP Gain = 1x and 3rd order Delta Sigma Modulator without dithering is adopted in both frequency sets. The register settings are summarized as follows:

Table 41. Register Settings Summary

CONFIGURATION PARAMETERS	REGISTER BIT	COMMON SETTING	F1 SPECIFIC SETTING	F2 SPECIFIC SETTING
VCO calibration	FCAL_EN	1 = Enabled		
Lock detect	SDO_LE_SEL	1 = Lock detect output		
	LD_EN	1 = Enabled		
OSCin buffer type	IPBUF_SE_DIFF_SEL	0 = SE input buffer		
Dithering	DITHERING	0 = Disabled		
Charge pump gain	CP_GAIN	1 = 1x		
Base charge pump current	CP_IUP	8 = 1250 µA		
	CP_IDN	8 = 1250 µA		
MULT settling time	MULT_WAIT	520 = 20 µs		
Output buffer type	OUTBUF_RX_TYPE	1 = Push pull		
	OUTBUF_TX_TYPE	1 = Push pull		
Output buffer auto mute	OUTBUF_AUTOMUTE	0 = Disabled		
TrCtl pin polarity	RXTX_POL	0 = Active LOW = TX		
TX RX switching mode	RXTX_CTRL	1 = TrCtl pin control		
Enable F1 F2 initialization	F1F2_MODE	1 = Enabled		
F1 F2 switching mode	F1F2_CTRL	1 = Control by TrCtl pin		
Pre-divider	PLL_R_PRE_F1		1	
	PLL_R_PRE_F2			1
MULT multiplier	MULT_F1		4	
	MULT_F2			4

Table 41. Register Settings Summary (continued)

CONFIGURATION PARAMETERS	REGISTER BIT	COMMON SETTING	F1 SPECIFIC SETTING	F2 SPECIFIC SETTING
Post-divider	PLL_R_F1		1	
	PLL_R_F2			1
ΔΣ modulator order	FRAC_ORDER_F1		3 = 3rd order	
	FRAC_ORDER_F2			3 = 3rd order
PFD delay	PFD_DELAY_F1		5 = 8 clock cycles	
	PFD_DELAY_F2			5 = 8 clock cycles
CHDIV1 divider	CHDIV1_F1		1 = Divide by 5	
	CHDIV1_F2			1 = Divide by 5
CHDIV2 divider	CHDIV2_F1		0 = Divide by 1	
	CHDIV2_F2			0 = Divide by 1
Internal 3rd pole loop filter	LF_R3_F1		4 = 800 Ω	
	LF_R3_F2			4 = 800 Ω
Internal 4th pole loop filter	LF_R4_F1		4 = 800 Ω	
	LF_R4_F2			4 = 800 Ω
Output port selection	OUTBUF_TX_EN_F1		1 = TX port enabled	
	OUTBUF_RX_EN_F2			1 = RX port enabled
Output power control	OUTBUF_TX_PWR_F1		6	
	OUTBUF_RX_PWR_F2			6
FSK mode	FSK_MODE_SEL1 FSK_MODE_SEL0	00 = FSK PIN mode		
FSK level	FSK_LEVEL	2 = 4FSK		
Enable FSK modulation	FSK_EN_F1		1 = Enabled	
FSK deviation at 00	FSK_DEV0_F1		4033 = +10 kHz	
FSK deviation at 01	FSK_DEV1_F1		12099 = +30 kHz	
FSK deviation at 10	FSK_DEV2_F1		61502 = -10 kHz	
FSK deviation at 11	FSK_DEV3_F1		53436 = -30 kHz	
Fractional denominator	PLL_DEN_F1[23:16]		0	
	PLL_DEN_F1[15:0]		0	
	PLL_DEN_F2[23:16]			0
	PLL_DEN_F2[15:0]			0
Fractional numerator	PLL_NUM_F1[23:16]		174	
	PLL_NUM_F1[15:0]		50412	
	PLL_NUM_F2[23:16]			78
	PLL_NUM_F2[15:0]			50412
$N_{integer}$	PLL_N_F1		21	
	PLL_N_F2			22
Prescaler	PLL_N_PRE_F1		0 = Divide by 2	
	PLL_N_PRE_F2			0 = Divide by 2

8.2.1.3 Synthesizer Duplex Mode Application Curves

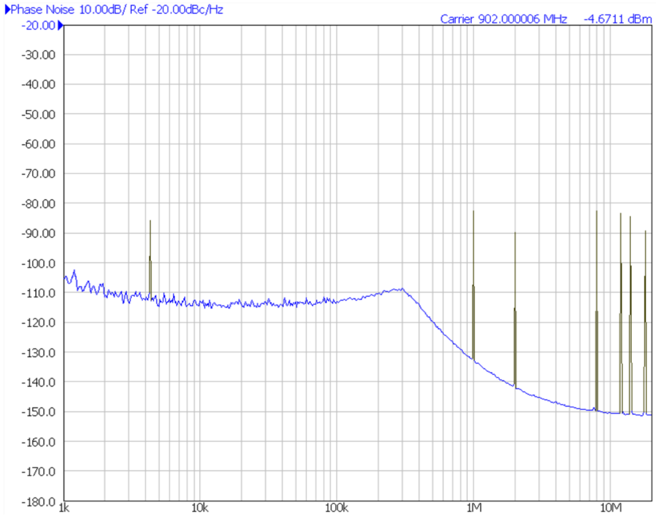


Figure 63. F1 (TX) Phase Noise and Spurs

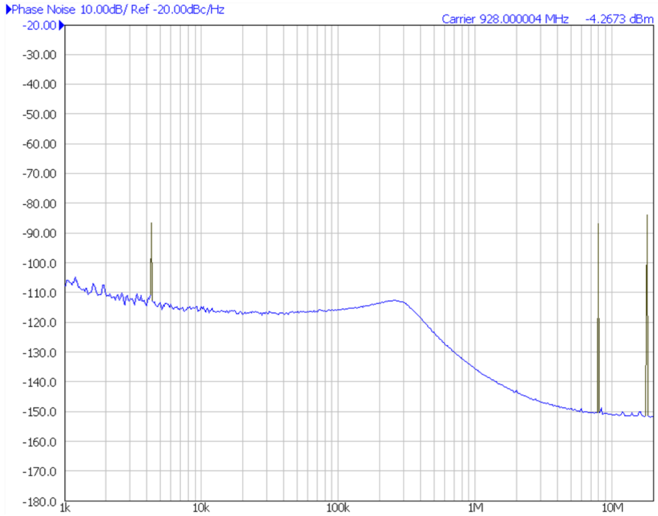


Figure 64. F2 (RX) Phase Noise and Spurs

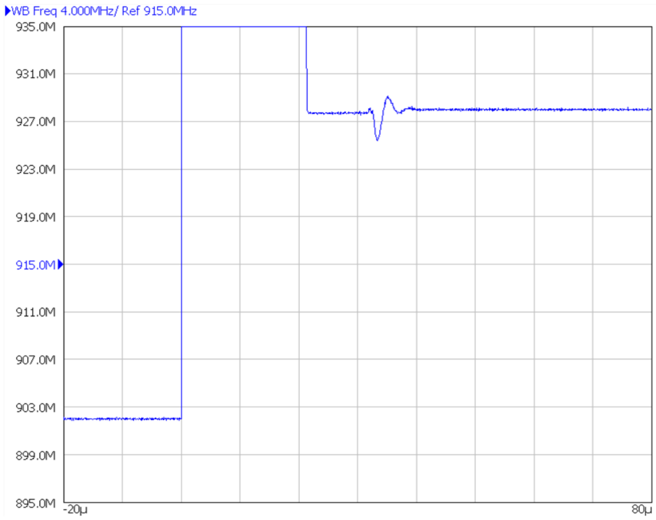


Figure 65. F1 (TX) to F2 (RX) Switching

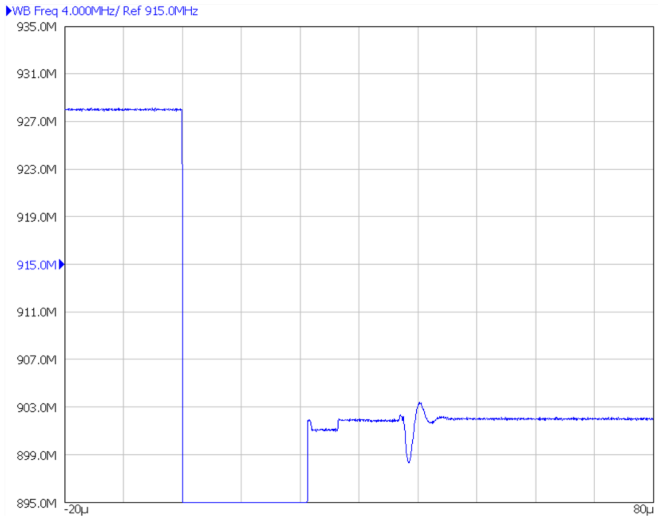


Figure 66. F2 (RX) to F1 (TX) Switching

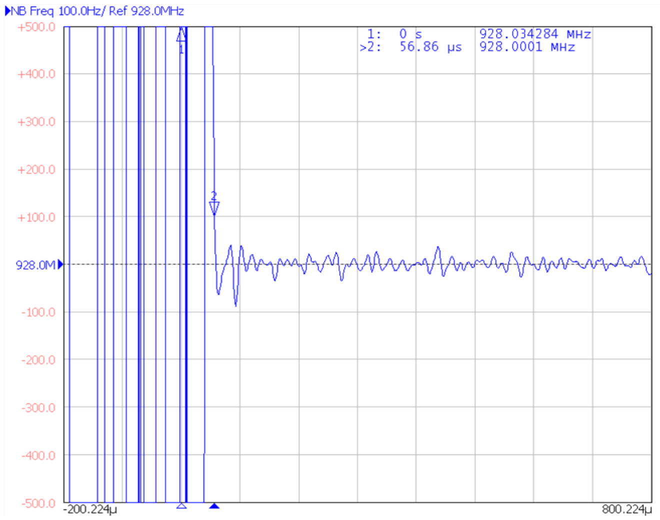


Figure 67. F1 to F2 Switching Time

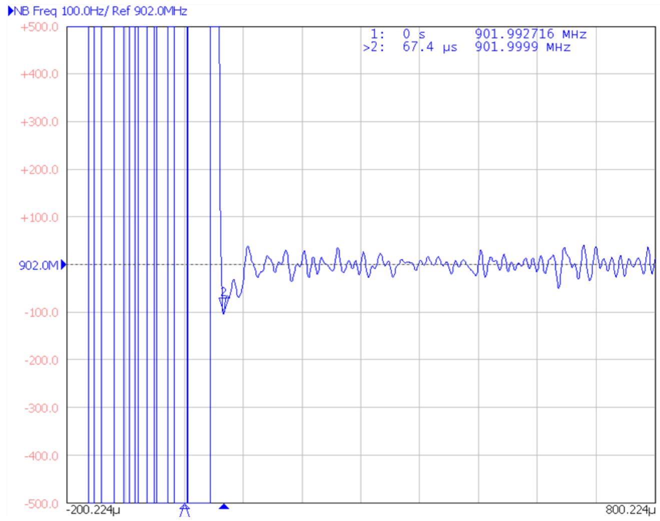


Figure 68. F2 to F1 Switching Time

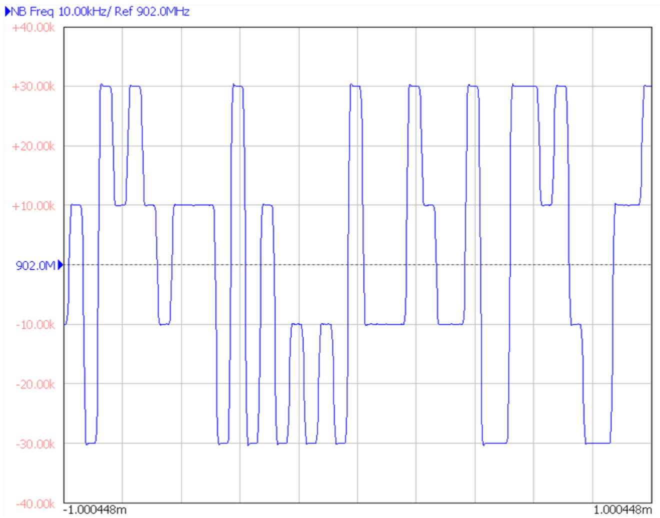


Figure 69. 4FSK Modulation

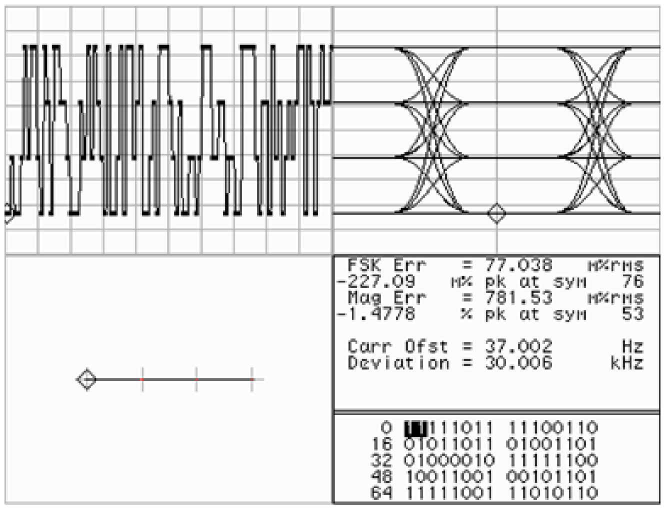


Figure 70. 4FSK Modulation Quality

8.2.2 PLL Duplex Mode

In this example, the internal VCO will be bypassed, and the device is used to lock to an external VCO. TI's dual SPST analog switch, TS5A21366 is used to facilitate FastLock between two frequencies.

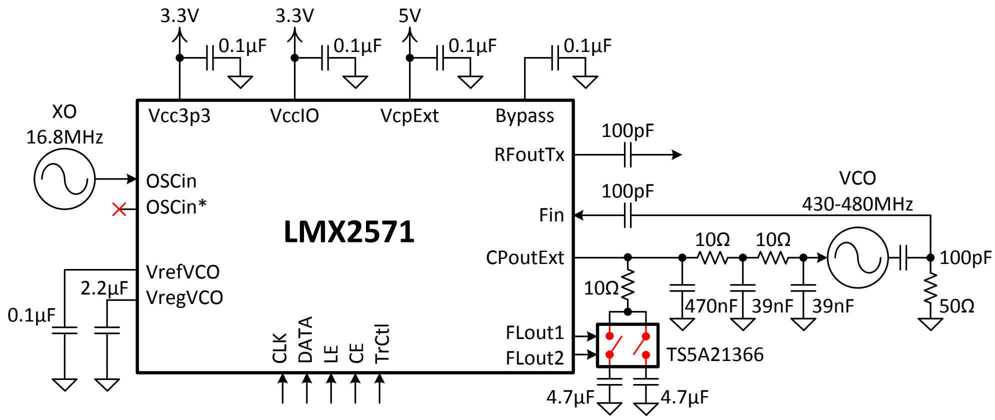


Figure 71. Typical PLL Duplex Mode Application Schematic

8.2.2.1 Design Requirements

OSCin frequency = 16.8 MHz, LVCMOS
F1 frequency = 430 MHz
F2 frequency = 480 MHz
Frequency switching time ≤ 1.5 ms within 100-Hz frequency tolerance

8.2.2.2 Detailed Design Procedure

Again, we need to figure out all the frequencies in each functional block first.

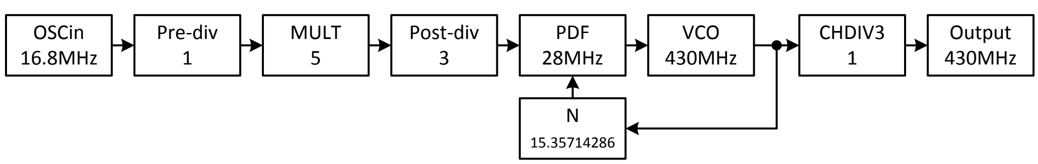


Figure 72. Frequency Plan in PLL Duplex Mode

Follow the previous example to determine all the necessary configurations. Table 42 is the summary in this example.

Table 42. PLL Duplex Mode Frequency Plan Summary

CONFIGURATION PARAMETER	F1 (430 MHz)	F2 (480 MHz)
Pre-divider	1	1
MULT	5	5
Post-divider	3	3
PDF	28 MHz	28 MHz
VCO	430 MHz	480 MHz
N-divider	15.35714286	17.14285714
$N_{integer}$	15	17
DEN	1234567	1234567
NUM	440917	176367

To enable external VCO operation, set the following bits:

Table 43. PLL Duplex Mode Register Settings Summary

CONFIGURATION PARAMETER	REGISTER BITS	SETTING
Charge pump polarity	EXTVCO_CP_POL	0 = Positive
External VCO charge pump gain	EXTVCO_CP_GAIN	1 = 1x
Base charge pump current	EXTVCO_CP_IUP	8 = 1250 µA
	EXTVCO_CP_IDN	8 = 1250 µA
Select PLL mode operation	EXTVCO_SEL_F1, EXTVCO_SEL_F2	1 = External VCO
CHDIV3 divider	EXTVCO_CHDIV_F1, EXTVCO_CHDIV_F2	0 = Bypass

Make sure that register R0, FCAL_EN is set so that FastLock is enabled.

The loop bandwidth had been design to be around 4 kHz, while phase margin is about 40 degrees.

8.2.2.3 PLL Duplex Mode Application Curves

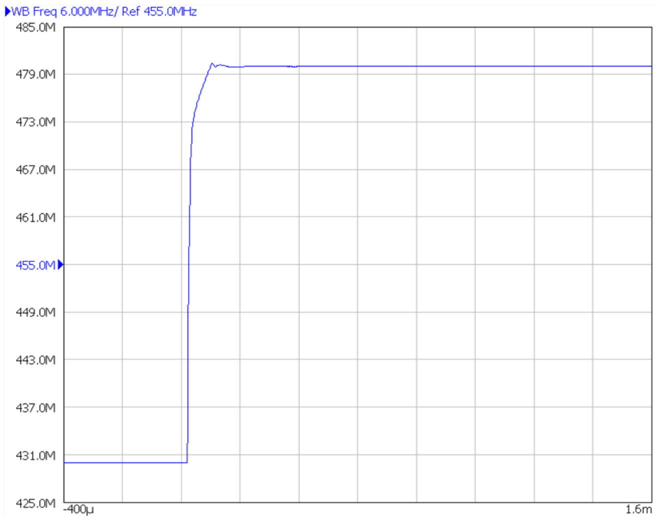


Figure 73. F1 to F2 Switching

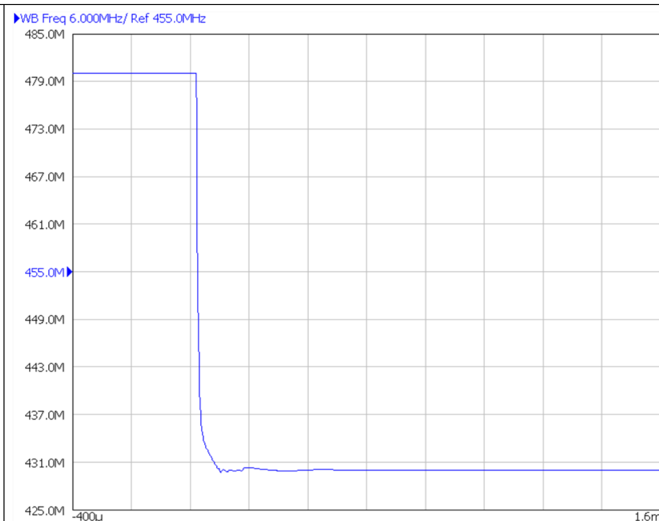


Figure 74. F2 to F1 Switching

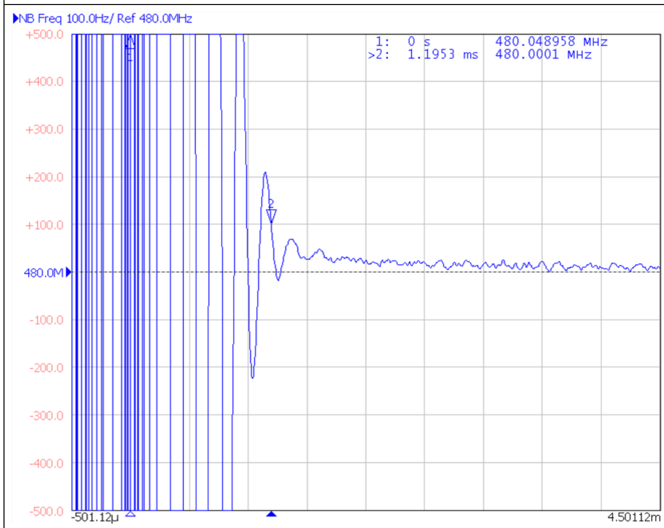


Figure 75. F1 to F2 Switching Time

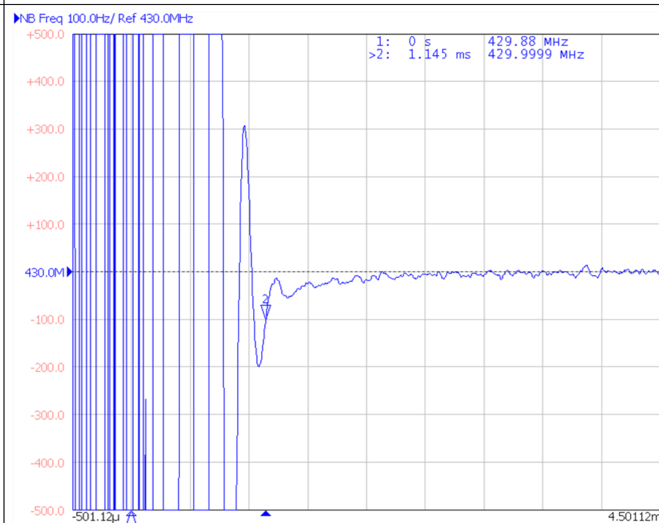


Figure 76. F2 to F1 Switching Time

8.2.3 Synthesizer/PLL Duplex Mode

This example will demonstrate the device's capability in switching two frequencies using internal and external VCO. VCO switching is toggled by the TrCtl pin. Direct digital FSK modulation is enabled in TX using FSK I2S mode.

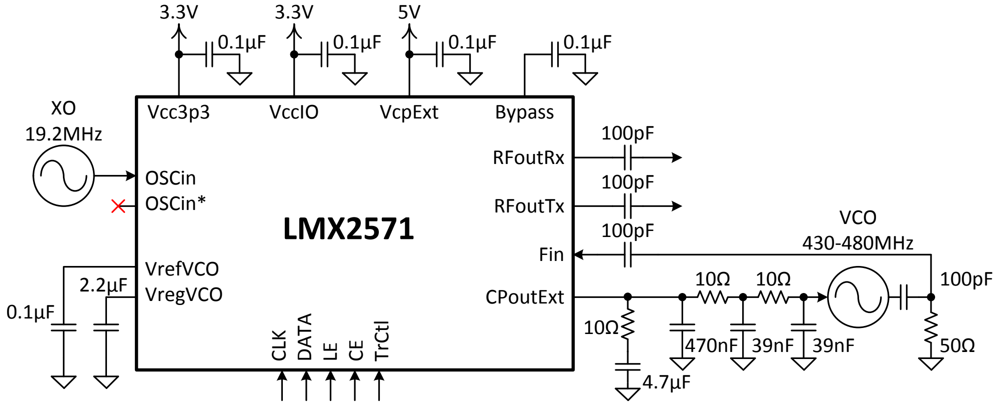


Figure 77. Typical Synthesizer/PLL Duplex Mode Application Schematic

8.2.3.1 Design Requirements

OSCin frequency = 19.2 MHz, LVCMOS
RFoutRX frequency = 440 MHz, external VCO = F1
RFoutTx frequency = 540 MHz, internal VCO = F2
Frequency switching time ≤ 1.5 ms within 100-Hz frequency tolerance
Arbitrary FSK modulation to simulate analog FM modulation (10 times and 20 times over-sampling rate)
FM modulation frequency = 1 kHz
Frequency deviation = ±2000 Hz
Spurs ≤ –72 dBc

8.2.3.2 Detailed Design Procedure

Frequency plans in TX and RX paths are as follows:

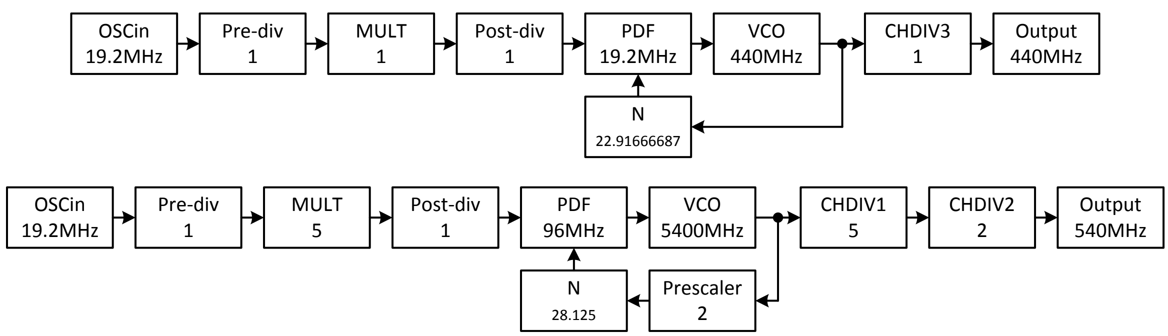


Figure 78. TX and RX Frequency Plans

Follow the previous examples to determine all the necessary configurations. To enable FSK I2S mode, set

FSK_MODE_SEL1=1
FSK_MODE_SEL=0
FSK_EN_F2=1

8.2.3.3 Synthesizer/PLL Duplex Mode Application Curves

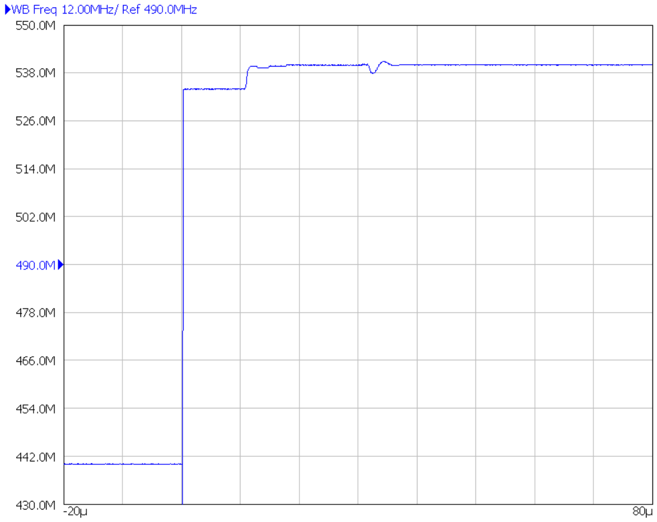


Figure 79. External VCO to Internal VCO Switching

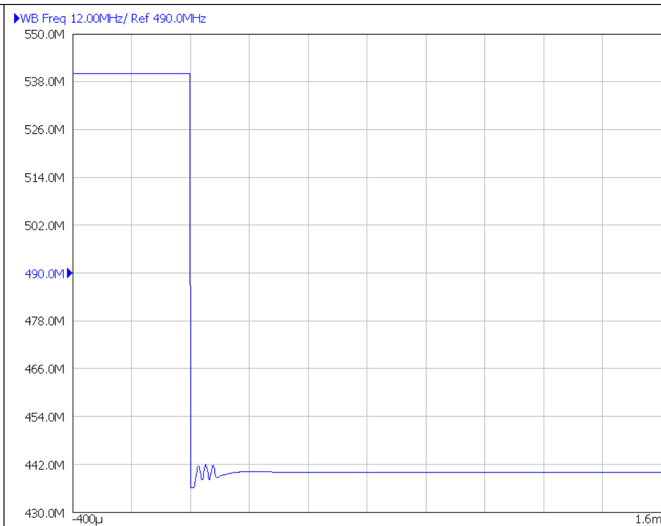


Figure 80. Internal VCO to External VCO Switching

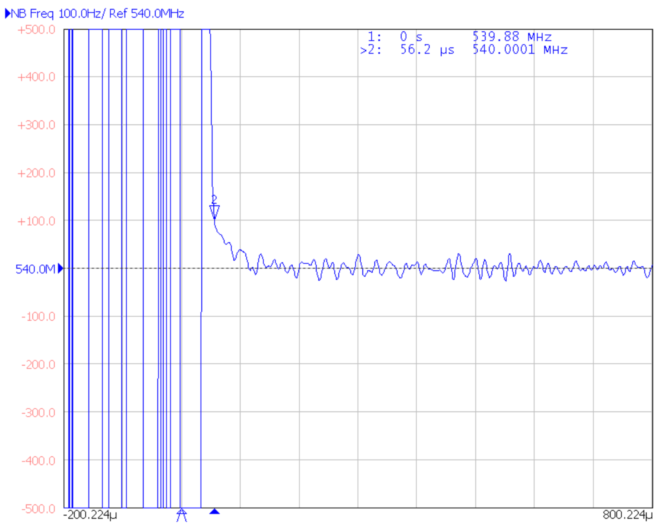


Figure 81. External VCO to Internal VCO Switching Time

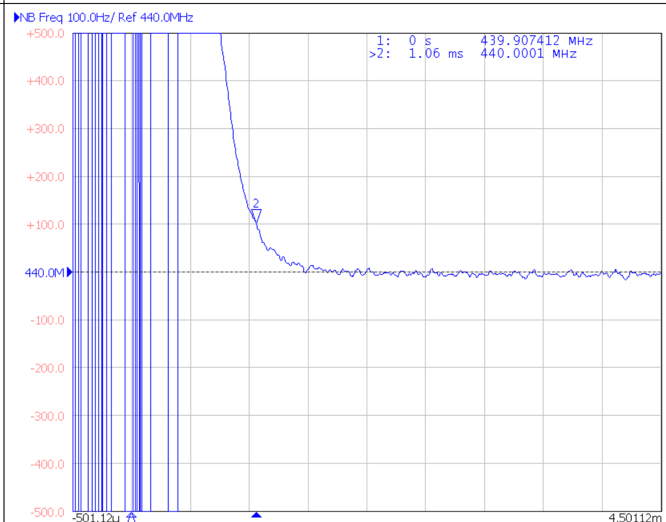


Figure 82. Internal VCO to External VCO Switching Time

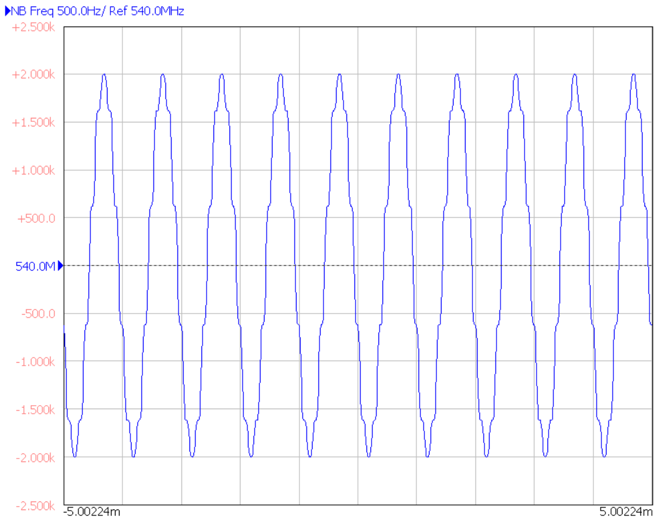


Figure 83. Simulated FM Modulation (10 times over-sampling)

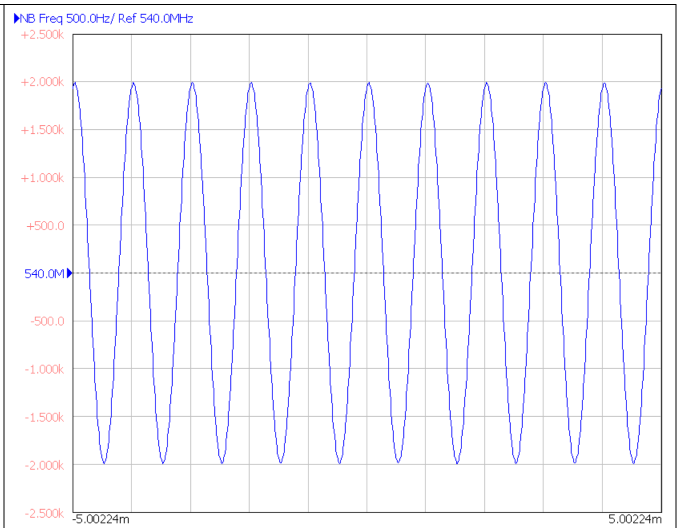


Figure 84. Simulated FM Modulation (20 times over-sampling)

8.3 Do's and Don'ts

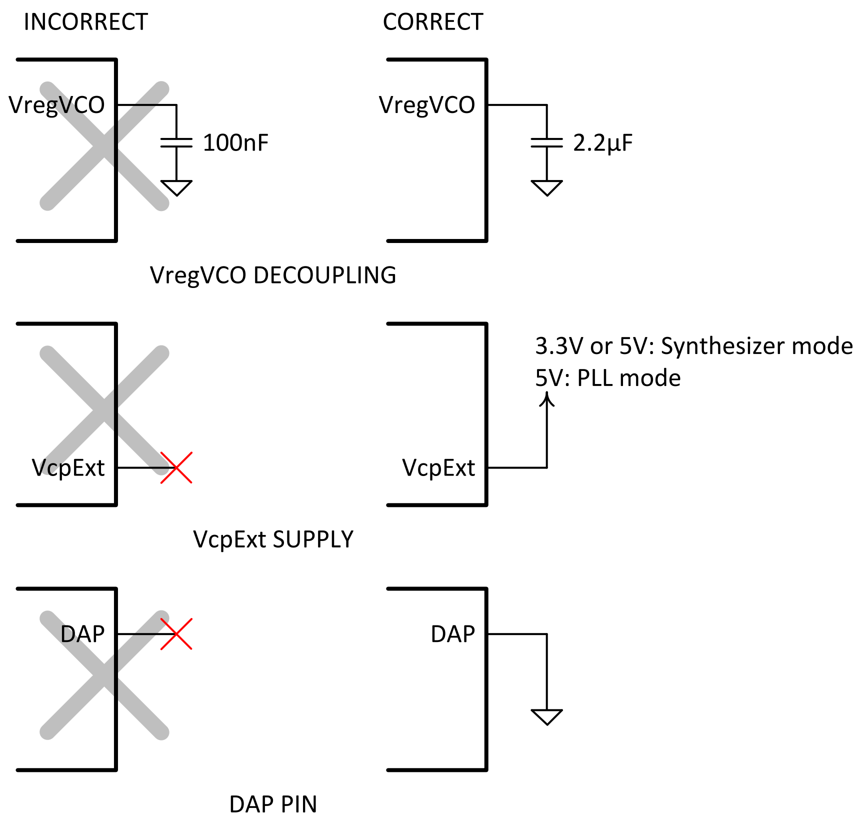


Figure 85. Do's and Don'ts

9 Power Supply Recommendations

It is recommended to place 100 nF capacitor close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins may reduce spurs to a small degree.

VcpExt is the power supply pin for the 5-V charge pump. In PLL mode, the 5-V charge pump is active and a 5 V is required at VcpExt pin. **In synthesizer mode, although the 5-V charge pump is not active, either a 3.3-V or 5-V supply is still needed at this pin.**

Because LMX2571 has integrated LDOs, the requirement to external power supply is relaxed. In addition to LDO, LMX2571 is able to operate with DC-DC converter. The switching noise from the DC-DC converter would not affect performance of the LMX2571. Table 44 lists some of the suggested DC-DC converters.

Table 44. Recommended DC-DC Converters

PART NUMBER	TOPOLOGY	V_{IN}	V_{OUT}	I_{OUT}	SWITCHING FREQUENCY
TPS560200	Buck	4.5 V to 17 V	0.8 V to 6.5 V	500 mA	600 kHz
TPS62050	Buck	2.7 V to 10 V	0.7 V to 6 V	800 mA	1 MHz
TPS62160	Buck	3 V to 17 V	0.9 V to 6 V	1000 mA	2.25 MHz
TPS562200	Buck	4.5 V to 17 V	0.76 V to 7 V	2000 mA	650 kHz
TPS63050	Buck Boost	2.5 V to 5.5 V	2.5 V to 5.5 V	500 mA to 1 A	2.5 MHz

10 Layout

10.1 Layout Guidelines

See *EVM instructions* for details. In general, the layout guidelines are similar to most other PLL devices. The followings are some guidelines specific to the device.

- It may be beneficial to separate main ground and OSCin ground, crosstalk spurs might be reduced.
- Don't route any traces that carry switching signal close to the charge pump traces and external VCO.
- When using FSK I2S mode on this device, care should be taken to avoid coupling between the I2S clock and any of the PLL circuit.

10.2 Layout Example

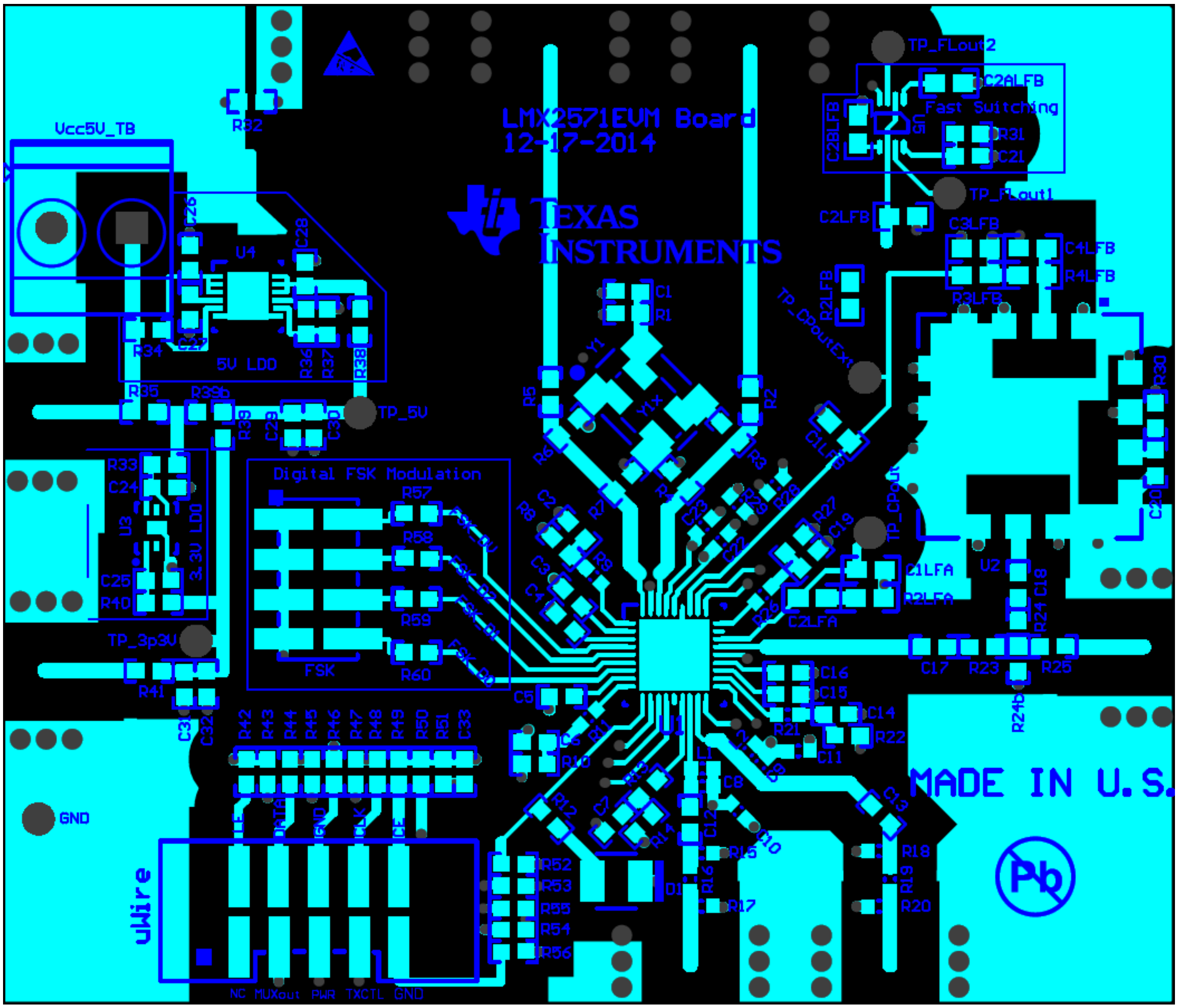


Figure 86. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Texas Instruments has several software tools to aid in the development process including CodeLoader for programming, Clock Design Tool for loop filter and phase noise/spur simulation, and the Clock Architect for a system solution finder. All these tools are available at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

SPRA953 Semiconductor and IC Package Thermal Metrics

TS5A21366 0.75-Ω Dual SPST Analog Switch with 1.8-V Compatible Input Logic

TPS560200 4.5V to 17V Input, 500mA Synchronous Step Down SWIFT™ Converter

TPS62050 800-mA Synchronous Step-Down Converter

TPS62160 3V-17V 1A Step-Down Converters with DCS-Control

TPS562200 4.5 V to 17 V Input, 2-A Synchronous Step-Down Voltage Regulator in SOT-23

TPS63050 Tiny Single Inductor Buck Boost Converter

11.3 Trademarks

PLLatinum is a trademark of Texas Instruments.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2571NJKR	ACTIVE	WQFN	NJK	36	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LMX2571	Samples
LMX2571NJKT	ACTIVE	WQFN	NJK	36	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LMX2571	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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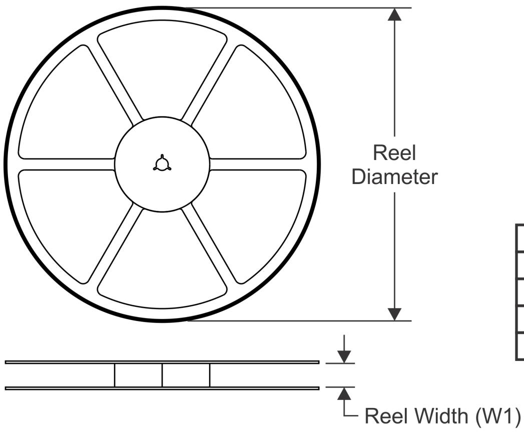
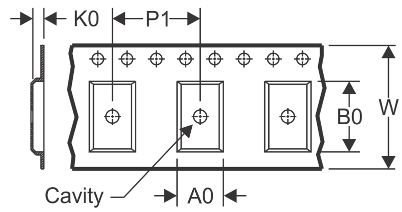
TAPE AND REEL INFORMATION

REEL DIMENSIONS

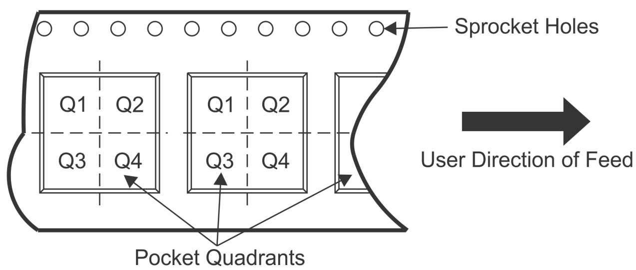


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

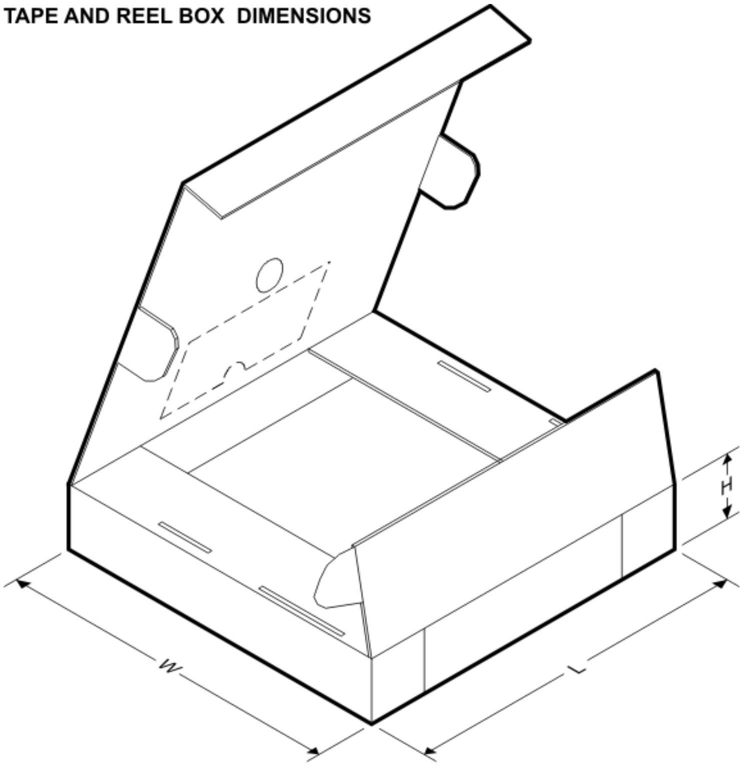
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2571NJKR	WQFN	NJK	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMX2571NJKT	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

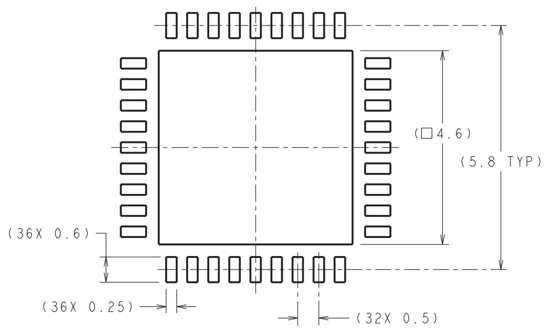
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

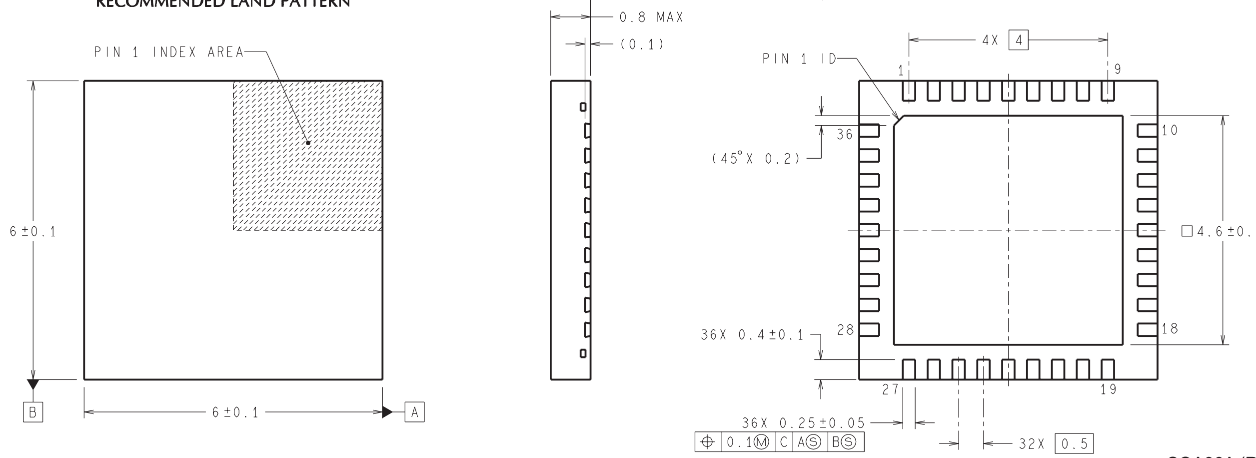
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2571NJKR	WQFN	NJK	36	2500	367.0	367.0	38.0
LMX2571NJKT	WQFN	NJK	36	250	213.0	191.0	55.0

NJK0036A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



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