LTC2348/LTC2347/LTC2343: 16-/18-Bit, Octal, Quad and Dual 200ksps/400ksps/600ksps SAR ADCs

DESCRIPTION

Demonstration circuit 2094A shows the proper way to drive the LTC®2348 family of ADCs. The LTC2348/LTC2347/LTC2343 are low noise, high speed, simultaneous sampling 16-/18-bit successive approximation register (SAR) ADCs. The following text refers to the LTC2348-18 but applies to all parts in the family, the only differences being the number of bits, number of channels and the maximum sample rate. The LTC2348-18 has a flexible SoftSpan™ interface that allows conversion-by-conversion control of the input voltage span on a per-channel basis. An internal 2.048V reference and 2X buffer simplify basic operation while an external reference can be used to increase the input range and the SNR of the ADC.

The DC2094 demonstrates the DC and AC performance of the LTC2348-18 in conjunction with the DC590/DC2026 and DC890 data collection boards. Use the DC590/DC2026 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The DC2094 is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. A suggested driver circuit for the analog inputs is also presented.

Design files for this circuit board are available at http://www.linear.com/demo/DC2094A

ASSEMBLY OPTIONS

Table 1. DC2094A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE (ksps)	NUMBER OF CHANNELS	NUMBER OF BITS	MAX CLK IN FREQUENCY (MHz)	CLK IN/ fs RATIO
DC2094A-A	LTC2348-18	200	8 Simultaneous	18	60	300
DC2094A-B	LTC2347-18	400	4 Simultaneous	18	67.2	168
DC2094A-C	LTC2343-18	600	2 Simultaneous	18	61.2	102
DC2094A-D	LTC2348-16	200	8 Simultaneous	16	60	300
DC2094A-E	LTC2347-16	400	4 Simultaneous	16	67.2	168
DC2094A-F	LTC2343-16	600	2 Simultaneous	16	61.2	102

DC2094A CONNECTION DIAGRAM

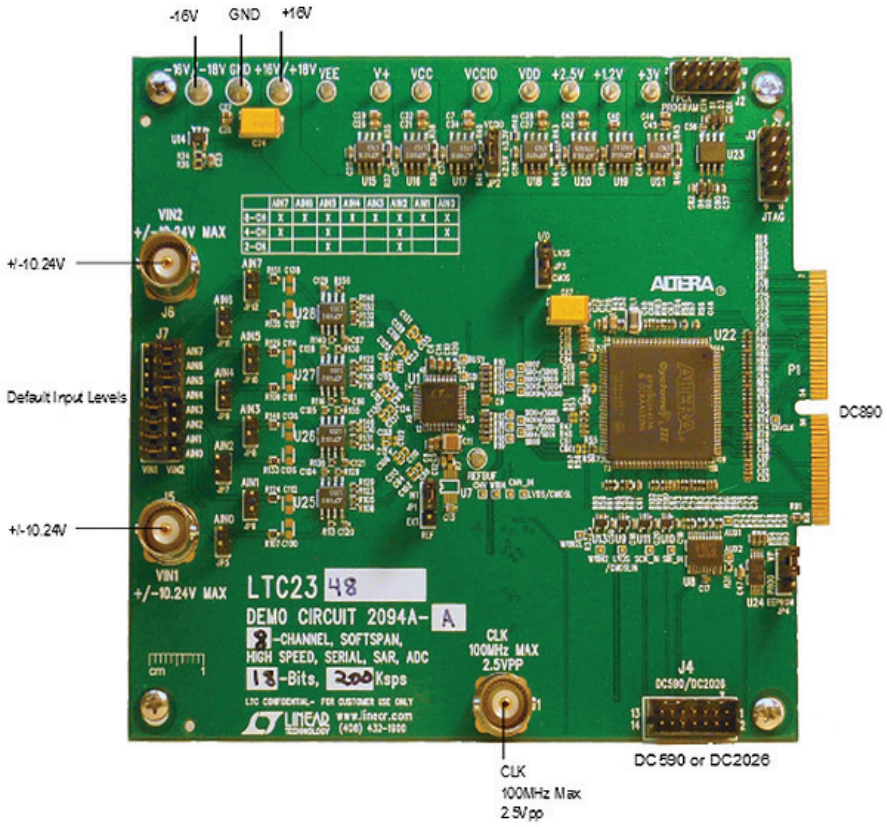


Figure 1. DC2094A Connection Diagram

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set to their default settings as described in the DC2094A Jumpers section of this manual. The default connections configure the ADC to use the onboard reference and regulators to generate all the required bias voltages. The analog inputs by default are DC coupled. Connect the DC2094A to a DC890 USB High Speed Data Collection Board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply ±16V to the indicated terminals. Then apply a low jitter signal source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0-AIN7 inputs. Observe the recommended input voltage range for each analog input. Connect a low jitter $2.5V_{P-P}$ sine wave or square wave to connector J1. See Table 1 for the appropriate clock frequency. Note that J1 has a 50Ω termination resistor to ground.

Run the PScope™ software (Pscope.exe version K79 or later), which can be downloaded, from www.linear.com/designtools/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2094A and configure itself automatically.

Click the Collect button (see Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC890 QUICK START PROCEDURE

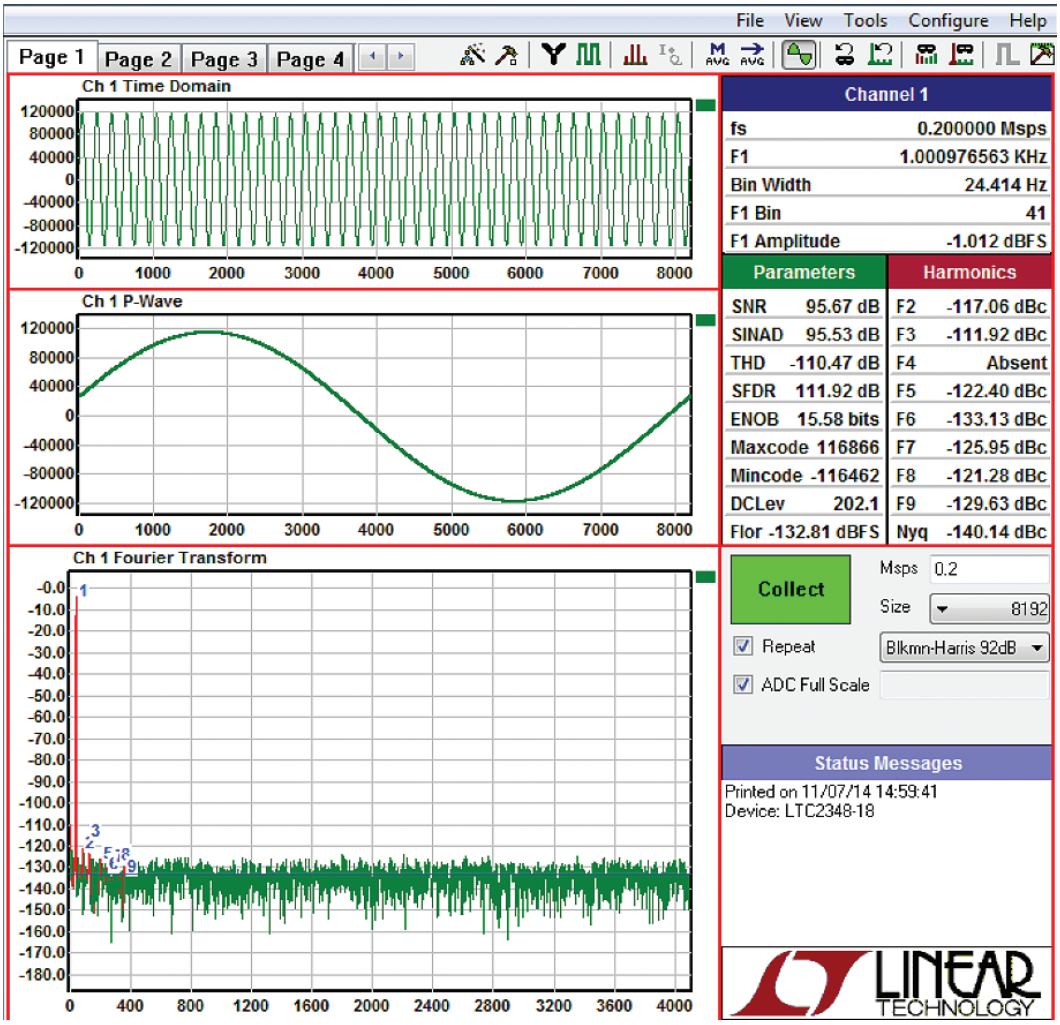


Figure 2. PScope Screen Shot

DC590/DC2026 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2094A, make sure that VCCIO (JP6 of the DC590, JP3 of the DC2026) of the DC590/DC2026 is set to 3.3V before connecting the DC590/DC2026 to the DC2094A.

To use the DC590/DC2026 with the DC2094A, it is necessary to apply ±16V and ground to the ±16V and GND terminals of the DC2094A. Connect the DC590/DC2026 to a host PC with a standard USB A/B cable. Connect the DC2094A to a DC590/DC2026 USB serial controller using the supplied 14-conductor ribbon cable. Apply a signal source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0-AIN7 inputs. No Clock is required on J1 when using the DC590/DC2026. The clock signal is provided by the DC590/DC2026.

Run the QuikEval™ software (quikeval.exe version K105 or later), which is available from www.linear.com/designtools/software. The correct control panel will be loaded automatically. Click the COLLECT button (Figure 6) to begin reading the ADC.

DC2094A SETUP

DC POWER

The DC2094A requires ±16VDC and draws +175mA/–12mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The ±16VDC input voltage powers the ADC through LT1763 regulators, which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and opamps.

CLOCK SOURCE

You must provide a low jitter $2.5V_{P-P}$ sine or square wave to the clock input, J1. The clock input is AC coupled so the DC level of the clock signal is not important. A generator such as the Rohde & Schwarz SMB100A high speed clock source is recommended to drive the clock input. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore, it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. The ratio of clock frequency to conversion rate is shown in Table 1. If the clock input is to be driven with logic, it is recommended that the 49.9Ω termination resistor (R4) be removed. Driving R4 with discreet logic may result in slow rising edges. These slow rising edges may compromise the SNR of the converter in the presence of high-amplitude higher frequency input signals.

DATA OUTPUT

Parallel data output from this board (0V to 2.5V by default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of P1 to latch the data. The data should be latched using the negative edge of this signal. The data output signal levels at P1 can also be increased to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving JP2 to the 3.3V position.

Reference

The default reference is the LTC2348-18 internal 4.096V reference. Alternatively, if a higher reference voltage is desired, the LTC6655-5 reference (U7) can be used by setting the REF jumper (JP1) to the EXT position and installing a 0Ω resistor in the R7 position. This should result in better SNR performance but may slightly degrade the THD performance of the LTC2348-18.

Analog Inputs

All eight inputs have the same driver circuitry. An example of the default driver circuit for the analog inputs of the LTC2348-18 on the DC2094A is shown in Figure 3. The circuit of Figure 3 provides a pseudo-differential output to Channel 2 and Channel 3 of the LTC2348-18 with a maximum ±10.24V single-ended input voltage. Alternatively, the two single-ended channels shown can be combined to form a fully differential driver. In the circuit of Figure 3 this is done by removing R131 and changing R141 to 0Ω. At this point both AIN2 and AIN3 must be driven to ±5.12V to achieve a full-scale input voltage for AIN2+ and AIN2– of the LTC2348-18. Changing R146 and R142 in a similar way would also allow AIN3+ and AIN3– of the LTC2348-18 to be driven fully differentially. Fully differential drive should provide a slight improvement in THD performance.

DC2094A SETUP

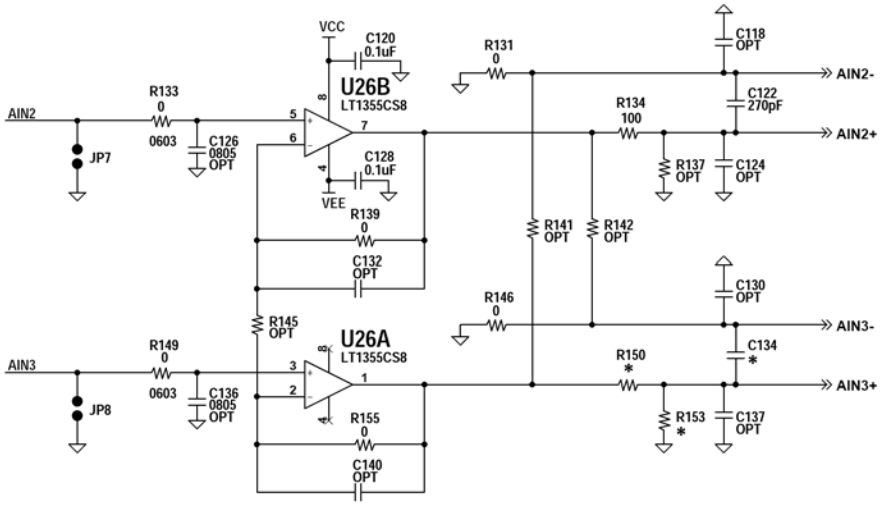


Figure 3. ±10.24V Pseudo-Differential DC Coupled Driver

DC890 DATA COLLECTION

For SINAD, THD or SNR testing a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A is used to drive the clock input. This demo board is tested in house by attempting to duplicate the FFT plot shown in Typical Performance Characteristics section of the LTC2348-18 data sheet. This involves using a 60MHz clock source, along with a sinusoidal generator at a frequency of approximately 1kHz. The input signal level is approximately –1dBFS. A typical FFT obtained with DC2094A is shown in Figure 2. Note that to calculate the real SNR, the signal level (F1 amplitude = –1.012dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 2 this means that the actual SNR would be 96.68dB instead of the 95.67dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 96.5dB, which is fairly close to the typical number for this ADC.

To change the default settings for the LTC2348-18 in PScope, click on the Set Demo Bd Options button in the PScope tool bar shown in Figure 4. This will open the Configure Channels menu of Figure 5. In this menu it is possible to set the input signal range and gain compression setting for each channel. There is also a button to return PScope to the default DC2094A settings, which are optimized for the default hardware settings of the DC2094A.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with an input frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine

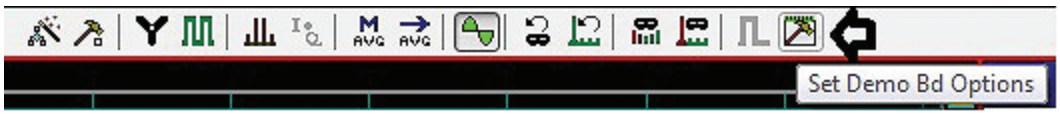


Figure 4. PScope Tool Bar

DC890 DATA COLLECTION

wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

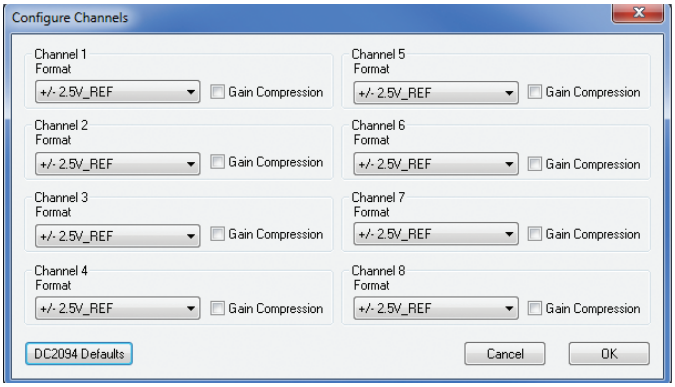


Figure 5. PScope Configuration Menu

DC590/DC2026 DATA COLLECTION

Due to the relatively low and somewhat unpredictable sample rate of the DC590/DC2026, its usefulness is limited to noise measurement and data collection of slowly moving signals. A typical data capture and histogram are shown in Figure 6. To change the default settings for the LTC2348-18 in QuikEval click on the Channel Config. button. This will open the ConfigDialog menu of Figure 7. In this menu it is possible to set the input signal range and gain compression setting for each sequence. There is also a button to return QuikEval to the default DC2094A settings, which are optimized for the default hardware settings of the DC2094A.

LAYOUT

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2094A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2348-18. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

COMPONENT SELECTION

When driving a low noise, low distortion ADC such as the LTC2348-18, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self-heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2348-18 should have low distortion, low noise and a fast settling time such as the LT1355.

DC590/DC2026 DATA COLLECTION

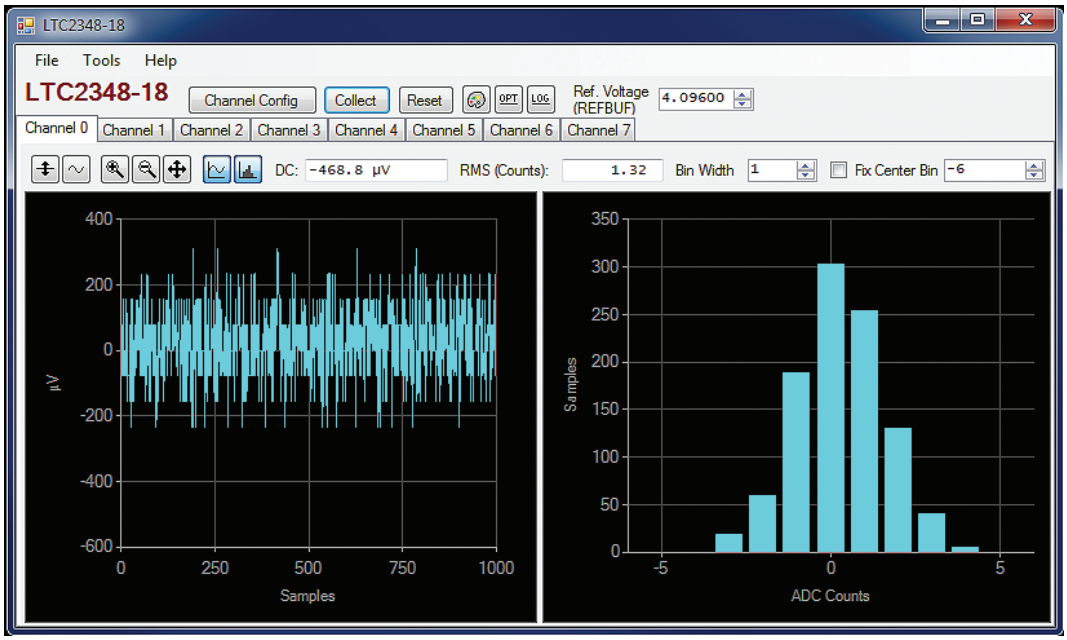


Figure 6. QuikEval Screen Shot

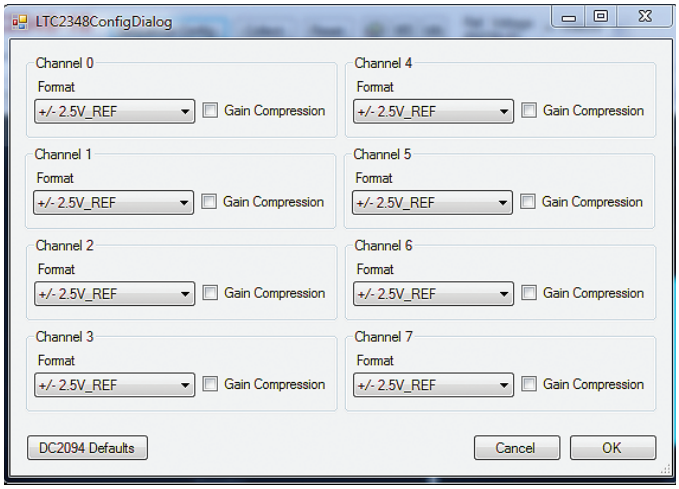


Figure 7. QuikEval Configuration Menu

DC2094A JUMPERS

DEFINITIONS

JP1 – REF selects INT or EXT reference for the ADC. The default setting is INT.

JP2 – VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890, which is the default setting. Use 3.3V to interface to the DC2026.

JP3 – I/O selects LVDS or CMOS logic levels. The default setting is CMOS. LVDS is for future use only.

JP4 – EEPROM is for factory use only. The default position is WP.

JP6 to JP12 – AIN0-AIN7 can be used to short individual AIN inputs to ground or can be used drive the individual AIN inputs. The default is to leave these open.

DC2094A CONNECTORS

DEFINITIONS

P1 – DC890 interface is used to communicate with the DC890 controller.

J1 – CLK provides the master clock for the DC2094A when interfaced to the DC890.

J2 – FPGA PROGRAM is used to program the FPGA. This is for factory use only.

J3 – JTAG is for factory use only.

J4 – DC590/DC2026 interface is used to communicate with the DC2026 Linduino controller or DC590.

J5 and J6 – Provide analog input voltages to AIN0-AIN7 of the ADC.

J7 – Routes the signals of J5 and J6 to AIN0-AIN7.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	13	C1-C3, C5-C9, C14-C16, C21, C47	CAP., X7R, 0.1µF, 25V, 10%, 0603	MURATA, GRM188R71E104KA01D
2	0	C4, C94, C95, C102, C103, C106-C109, C113, C115-C119, C124, C125, C130-C133, C137, C139-C141	CAP., 0402	OPT
3	2	C10, C12	CAP., X5R, 2.2µF, 25V, 20%, 0603	TDK, C1608X5R1E225M080AB
4	1	C11	CAP., X7R, 47µF, 10V, 10%, 1210	MURATA, GRM32ER71A476KE15L
5	8	C13, C25, C28, C30, C33, C36, C41, C44	CAP., X7R, 1µF, 50V, 10%, 0603	TAIYO YUDEN, UMK107AB7105KA-T
6	9	C23, C27, C29, C32, C35, C38, C40, C43, C46	CAP., X5R, 10µF 25V, 20%, 0603	MURATA, GRM188R61E106MA73D
7	37	C17-C20, C22, C48-C69, C73, C84, C85, C90-C92, C97, C105, C120, C128	CAP., X7R, 0.1µF, 50V, 10%, 0402	MURATA, GRM155R71H104KE14D
8	1	C24	CAP., TANT, 47µF 25V, 20%, 7343	AVX, TPSD476M025R0250
9	6	C26, C31, C34, C37, C42, C45	CAP., X7R, 0.01µF, 50V, 10%, 0603	MURATA, GRM188R71H103KA01D
10	1	C39	CAP., X5R, 3.3µF 25V, 20%, 0603	TDK, C1608X5R1E335M
11	1	C70	CAP., X5R, 47µF 6.3V, 20%, 0805	SAMSUNG, CL21A476MQCLRNC
12	2	C71, C88	CAP., X5R, 4.7µF, 10V, 10%, 0603	SAMSUNG, CL10A475KP8NNNC
13	3	C72, C83, C89	CAP., X7R, 0.01µF, 16V, 10%, 0402	MURATA, GRM155R71C103KA01D
14	1	C74	CAP., X7R, 1nF, 50V, 10%, 0402	AVX, 04025C102KAT2A
15	3	C75, C76, C77	CAP., X7R, 22nF, 50V, 10%, 0402	MURATA, GRM155R71H223KA12D
16	2	C78, C93	CAP., X7R, 4.7nF, 50V, 10%, 0402	MURATA, GRM155R71H472KA01D
17	4	C79, C80, C81, C82	CAP., C0G, 10pF, 50V, 5%, 0402	MURATA, GRM1555C1H100JA01D
18	1	C86	CAP., X7R, 2.2nF, 50V, 10%, 0402	MURATA, GRM155R71H222KA01D
19	1	C87	CAP., TANT, 470µF 10V, 20%, 7343	AVX, TPSE477M010R0050
20	0	C100, C101, C112, C114, C126, C127, C136, C138	CAP., 0805	OPT
21	2	C111, C122	CAP., NP0, 270pF, 50V, 2%, 0402	MURATA, GRM1555C1H271GA01D
22	4	D1, D2, D3, D4	DIODE, SCHOTTKY 30V 0.1A, SOD323	DIODES INC., BAT54WS-7-F
23	9	E1, E2, E4, E7-E12	TESTPOINT, TURRET, 0.064" pbf	MILL-MAX, 2308-2-00-80-00-00-07-0
24	3	E3, E5, E6	TESTPOINT, TURRET, 0.094" pbf	MILL-MAX, 2501-2-00-80-00-00-07-0
25	4	JP1, JP2, JP3, JP4	JMP, 1X3, 0.100", HD1X3-100	WÜRTH ELEKTRONIK, 61300311121
26	4	JP7, JP8, JP9, JP10	HEADER, 1X2, 0.100", HD1X2-100	SAMTEC, TSW-102-07-L-S
27	3	J1, J5, J6	CONN BNC FEM JACK PC MNT STRGHT, BNC5	AMPHENOL CONNEX, 112404
28	2	J2, J3	HEADER, 2X5, 0.100", HD2X5-100	WÜRTH ELEKTRONIK, 61301021121
29	1	J4	CONN., 14 Pin, 2mm	MOLEX, 87831-1420
30	1	J7	HEADER, 3X8, 0.100", HD3X8-100	SAMTEC, TSW-108-07-L-T
31	1	L1	FERRITE BEAD, 1206	MURATA, BLM31PG391SN1L
32	10	R1, R5, R21, R22, R36, R37, R39, R41, R44, R46	RES., CHIP, 1k, 1/10W, 1% 0603	YAGEO, RC0603FR-071KL
33	15	R2, R3, R6, R8, R10-R20	RES., CHIP, 33Ω, 1/10W, 5% 0603	YAGEO, RC0603JR-0733RL
34	1	R4	RES., CHIP, 49.9Ω, 1/4W, 1% 1206	YAGEO, RC1206FR-0749R9L
35	0	R7	RES., 0603	OPT
36	5	R9, R109, R125, R133, R149	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603FR-070RL

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
37	0	R23, R50, R51, R53, R54, R56, R57, R114, R115, R117-R119, R121, R128, R137, R141, R142, R143-R145, R147	RES., 0402	OPT
38	40	R24-R31, R33, R49, R52, R62-R90	RES., CHIP, 33Ω, 1/16W, 5% 0402	YAGEO, RC0402JR-0733RL
39	17	R32, R47, R48, R55, R58, R105, R106, R116, R120, R122, R130-R132, R139, R146, R148, R155	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
40	2	R34, R38	RES., CHIP, 11.5k, 1/10W, 1% 0603	YAGEO, RC0603FR-0711K5L
41	1	R35	RES., CHIP, 5.62k, 1/10W, 1% 0603	YAGEO, RC0603FR-075K62L
42	1	R40	RES., CHIP, 1.07k, 1/10W, 1% 0603	YAGEO, RC0603FR-071K07L
43	1	R42	RES., CHIP, 1.58k, 1/10W, 1% 0603	YAGEO, RC0603FR-071K58L
44	1	R43	RES., CHIP, 3.09k, 1/10W, 1% 0603	YAGEO, RC0603FR-073K09L
45	1	R45	RES., CHIP, 1.43k, 1/10W, 1% 0603	YAGEO, RC0603FR-071K43L
46	11	R59, R60, R95-R103	RES., CHIP, 10k, 1/16W, 5% 0402	YAGEO, RC0402JR-0710KL
47	4	R91, R92, R93, R94	RES., CHIP, 4.99k, 1/10W, 1% 0603	YAGEO, RC0603FR-074K99L
48	1	R104	RES., CHIP, 1k, 1/16W, 5% 0402	YAGEO, RC0402JR-071KL
49	2	R126, R134	RES., CHIP, 100Ω, 1/16W, 1% 0402	YAGEO, RC0402FR-07100RL
50	4	U2, U3, U5, U13	IC., INVERTER UHS SINGLE, SC70-5	FAIRCHILD, NC7SZ04P5X
51	1	U4	IC., D-TYPE POS TRG SNGL, US8	ON SEMI., NL17SZ74USG
52	5	U6, U9, U10, U11, U12	IC., BUS SWITCH SPST SGL LV, SC70-5	FAIRCHILD, NC7SZ66P5X
53	1	U7	IC., 0.25ppm NOISE, LOW DRIFT PRECISION REF., MS8	LINEAR TECH., LTC6655BHMS8-5
54	1	U8	IC., I/O EXPANDER I^2C 8B, SSOP20	NXP, PCF8574TS/3, 118
55	1	U14	IC., 200mA LDO MICROPWR REGULATORS, SOT23-5	LINEAR TECH., LT1964ES5-SD
56	5	U15, U16, U17, U18, U21	IC., 500mA LDO MICROPWR REGULATORS, SO8	LINEAR TECH., LT1763CS8
57	1	U19	IC, LINEAR REGULATOR, SO8	LINEAR TECH., LT3021ES8-1.2
58	1	U20	IC., 500mA LDO MICROPWR REGULATORS, SO8	LINEAR TECH., LT1763CS8-2.5
59	1	U22	IC, CYCLONE III FPGA 5K, EQFP144	ALTERA, EP3C5E144C7N
60	1	U23	IC, CONFIG DEVICE 4MBIT, SO8	ALTERA, EPCS4SI8N
61	1	U24	IC., SERIAL EEPROM, TSSOP8	MICROCHIP, 24LC024-I/ST
62	2	U26, U27	IC, DUAL 12MHz, OP AMP, SO8	LINEAR TECH., LT1355CS8
63	4	MH1-MH4	STAND-OFF, NYLON, 0.25"	KEYSTONE, 8831(SNAP ON)
64	12	SHUNTS AS ASSY DWG (JP1-JP4, J7)	SHUNT, 0.1" CENTER	WÜRTH ELEKTRONIK, 60900213421

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2094A-A Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	4	C96, C104, C121, C129	CAP., X7R, 0.1µF, 50V, 10%, 0402	TAIYO YUDEN, UMK105B7104KV-FR
3	6	C98, C135, C99, C110, C123, C134	CAP., NP0, 270pF, 50V, 2%, 0402	MURATA, GRM1555C1H271GA01D
4	4	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	SAMTEC, TSW-102-07-L-S
5	6	R61, R113, R129, R140, R151, R156	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
6	6	R108, R152, R110, R123, R136, R150	RES., CHIP, 100Ω, 1/16W, 1% 0402	YAGEO, RC0402FR-07100RL
7	4	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603FR-070RL
8	0	R111, R154, R112, R127, R138, R153	RES., 0402	OPT
9	1	U1	I.C., 8-CH, LQFP48LX-7X7	LINEAR TECH., LTC2348ILX-18
10	2	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	LINEAR TECH., LT1355CS8
DC2094A-B Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	4	C96, C104, C121, C129	CAP., X7R, 0.1µF, 50V, 10%, 0402	TAIYO YUDEN, UMK105B7104KV-FR
3	2	C98, C135	CAP., NP0, 270pF, 50V, 2%, 0402	MURATA, GRM1555C1H271GA01D
4	0	C99, C110, C123, C134	CAP., 0402	OPT
5	4	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	SAMTEC, TSW-102-07-L-S
6	10	R61, R113, R129, R140, R151, R156, R112, R127, R138, R153	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
7	4	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603FR-070RL
8	2	R108, R152	RES., CHIP, 100Ω, 1/16W, 1% 0402	YAGEO, RC0402FR-07100RL
9	0	R110, R123, R136, R150, R111, R154	RES., 0402	OPT
10	1	U1	I.C., 4-CH, LQFP48LX-7X7	LINEAR TECH., LTC2347ILX-18
11	2	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	LINEAR TECH., LT1355CS8

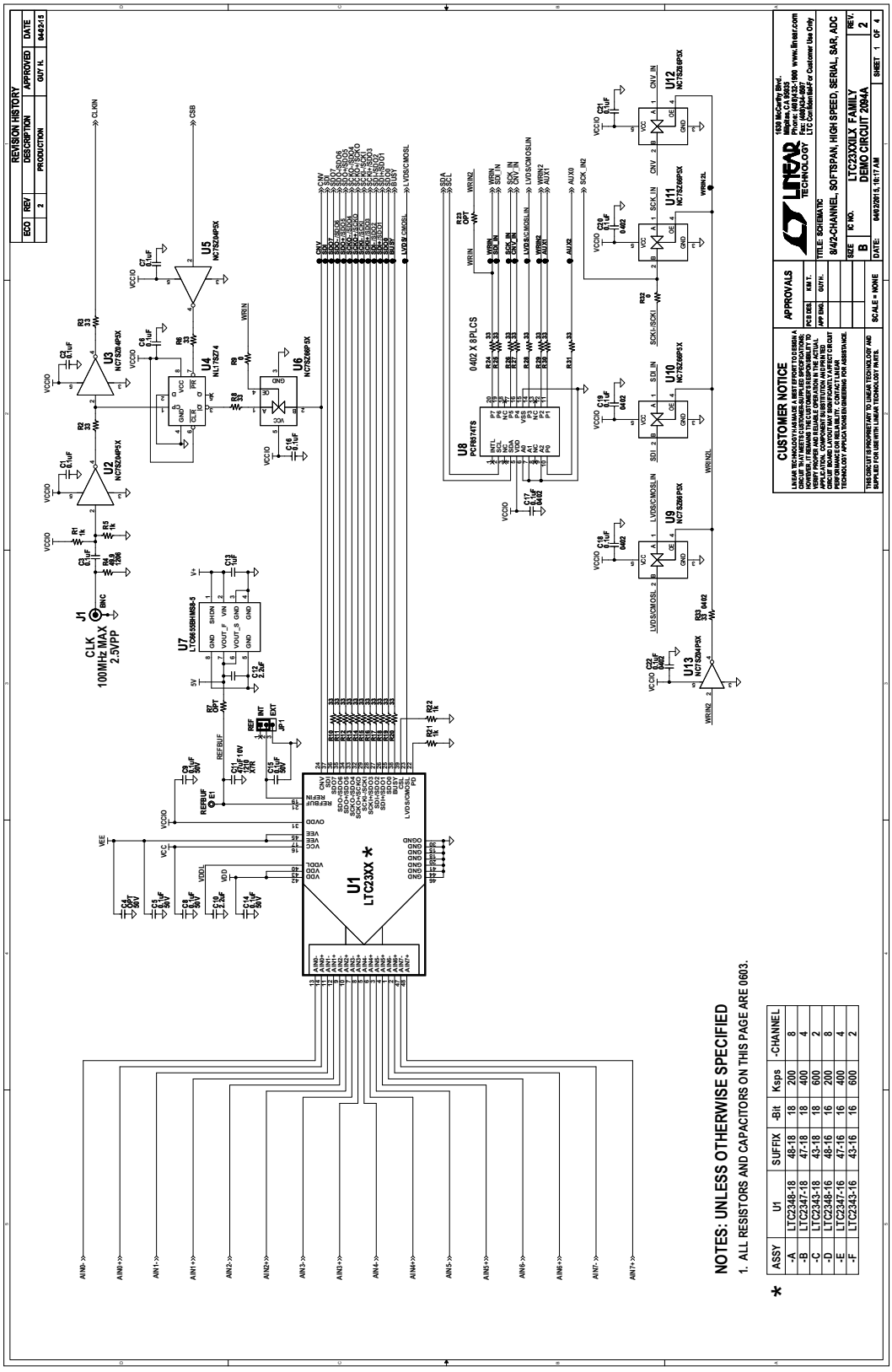
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2094A-C Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	0	C96, C104, C121, C129, C98, C135, C99, C110, C123, C134	CAP., X7R, 0.1µF, 50V, 10%, 0402	OPT
3	0	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	OPT
4	7	R61, R111, R154, R112, R127, R138, R153	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
5	0	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	OPT
6	0	R108, R152, R113, R129, R140, R151, R156, R110, R123, R136, R150	RES., 0402	OPT
7	1	U1	I.C., 2-CH, LQFP48LX-7X7	LINEAR TECH., LTC2343ILX-18
8	0	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	OPT
DC2094A-D Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	4	C96, C104, C121, C129	CAP., X7R, 0.1µF, 50V, 10%, 0402	TAIYO YUDEN, UMK105B7104KV-FR
3	6	C98, C135, C99, C110, C123, C134	CAP., NP0, 270pF, 50V, 2%, 0402	MURATA, GRM1555C1H271GA01D
4	4	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	SAMTEC, TSW-102-07-L-S
5	0	R61, R111, R154, R112, R127, R138, R153	RES., 0402	OPT
6	4	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603FR-070RL
7	6	R108, R152, R110, R123, R136, R150	RES., CHIP, 100Ω, 1/16W, 1% 0402	YAGEO, RC0402FR-07100RL
8	5	R113, R129, R140, R151, R156	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
9	1	U1	I.C., 8-CH, LQFP48LX-7X7	LINEAR TECH., LTC2348ILX-16
10	2	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	LINEAR TECH., LT1355CS8

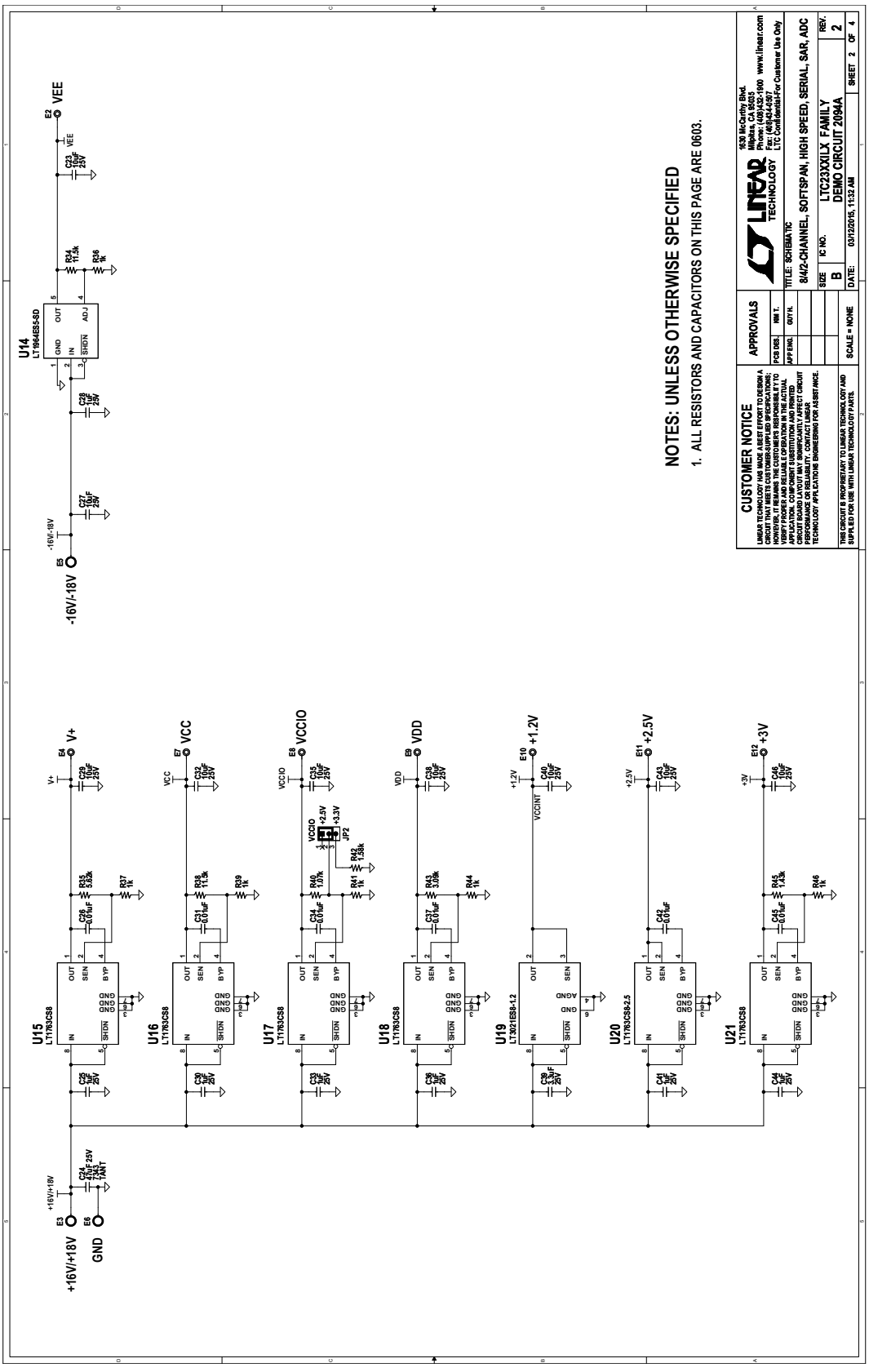
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2094A-E Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	4	C96, C104, C121, C129	CAP., X7R, 0.1µF, 50V, 10%, 0402	TAIYO YUDEN, UMK105B7104KV-FR
3	2	C98, C135	CAP., NP0, 270pF, 50V, 2%, 0402	MURATA, GRM1555C1H271GA01D
4	0	C99, C110, C123, C134	CAP., 0402	OPT
5	4	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	SAMTEC, TSW-102-07-L-S
6	0	R61, R110, R123, R136, R150, R111, R154	RES., 0402	OPT
7	4	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603FR-070RL
8	2	R108, R152	RES., CHIP, 100Ω, 1/16W, 1% 0402	YAGEO, RC0402FR-07100RL
9	9	R112, R127, R138, R153, R113, R129, R140, R151, R156	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
10	1	U1	I.C., 4-CH, LQFP48LX-7X7	LINEAR TECH., LTC2347ILX-16
11	2	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	LINEAR TECH., LT1355CS8
DC2094A-F Required Circuit Components				
1	1		DC2094A-GENERAL BOM	
2	0	C96, C104, C121, C129, C98, C135, C99, C110, C123, C134	CAP., X7R, 0.1µF, 50V, 10%, 0402	OPT
3	0	JP5, JP6, JP11, JP12	HEADER, 1X2, 0.100", HD1X2-100	OPT
4	0	R61, R113, R129, R140, R151, R156, R108, R152, R110, R123, R136, R150	RES., 0402	OPT
5	0	R107, R124, R135, R151	RES., CHIP, 0Ω, 1/10W, 0603	OPT
6	6	R111, R154, R112, R127, R138, R153	RES., CHIP, 0Ω, 1/10W, 0402	YAGEO, RC0402FR-070RL
7	1	U1	I.C., 2-CH, LQFP48LX-7X7	LINEAR TECH., LTC2343ILX-16
8	0	U25, U28	IC, DUAL 12MHz, OP AMP, SO8	OPT

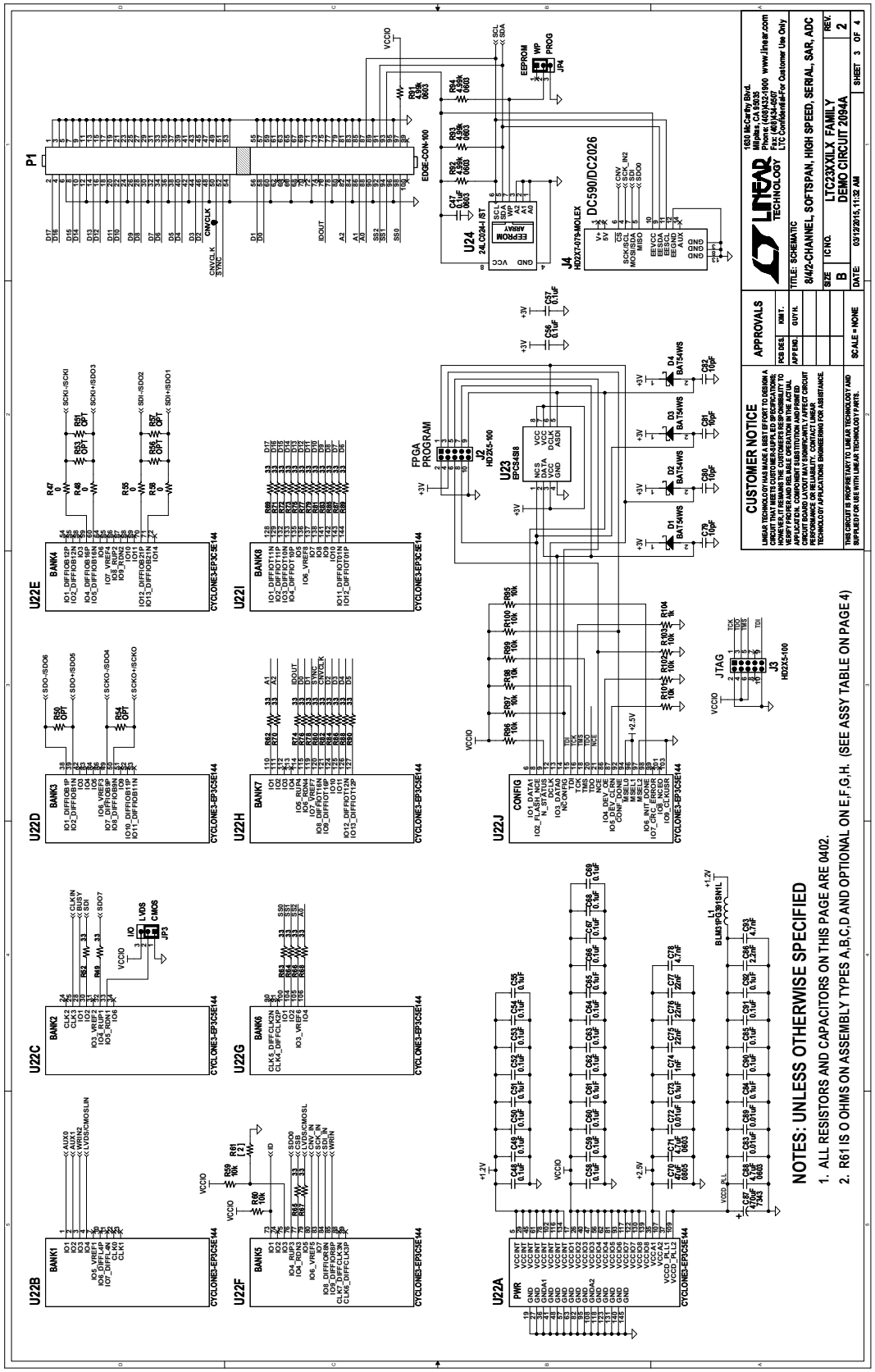
SCHEMATIC DIAGRAM



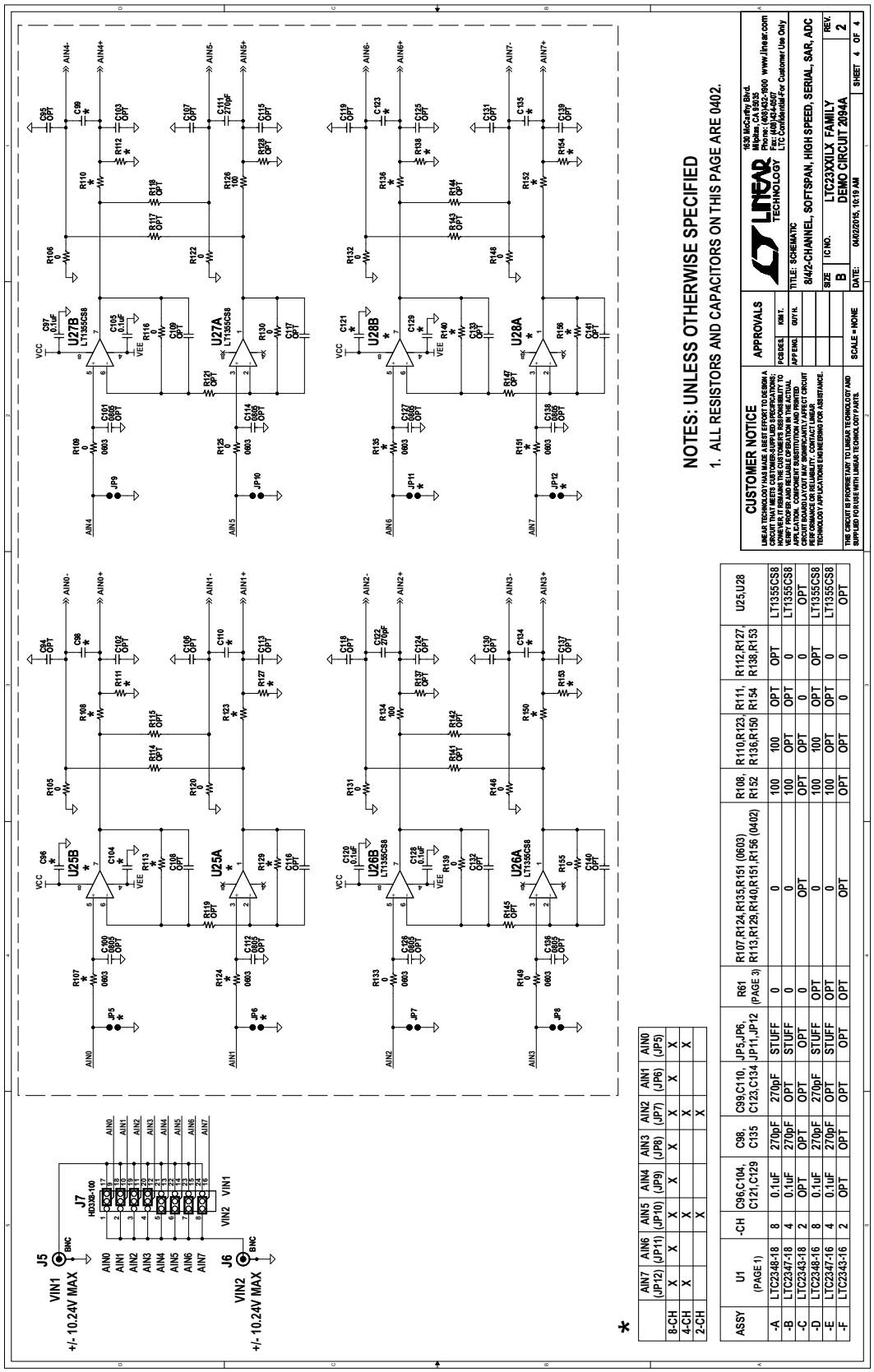
SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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	AIN7 (JP12)	AIN6 (JP11)	AIN5 (JP10)	AIN4 (JP9)	AIN3 (JP8)	AIN2 (JP7)	AIN1 (JP6)	AIN0 (JP5)
8-CH	X	X	X	X	X	X	X	X
4-CH	X		X			X		X
2-CH			X			X		

ASSY	U1 (PAGE 1)	-CH	C96,C104, C121,C129	C98, C135	C99,C110, C123,C134	JP5,JP6, JP11,JP12	R61 (PAGE 3)	R107,R124,R135,R151 (0603) R113,R129,R140,R156 (0402)	R108, R152	R110,R123, R136,R150	R111, R154	R112,R127, R138,R153	U25,U28
-A	LTC2348-18	8	0.1uF	270pF	STUFF	0		0	100	100	OPT	OPT	LT1355CS8
-B	LTC2347-18	4	0.1uF	270pF	OPT	STUFF	0		100	OPT	OPT	0	LT1355CS8
-C	LTC2343-18	2	OPT	OPT	OPT	OPT	0	OPT	OPT	OPT	0	0	OPT
-D	LTC2348-16	8	0.1uF	270pF	STUFF	OPT	0	0	100	100	OPT	OPT	LT1355CS8
-E	LTC2347-16	4	0.1uF	270pF	OPT	STUFF	OPT	0	100	OPT	OPT	0	LT1355CS8
-F	LTC2343-16	2	OPT	OPT	OPT	OPT	OPT	OPT	OPT	OPT	0	0	OPT

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