

# ACNT-H61L

Low Power 10 MBd Digital CMOS Optocoupler  
in 14.2 mm Creepage/Clearance Stretched SO8 Package



## Data Sheet

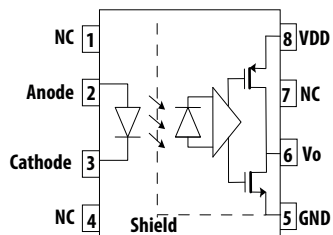
### Description

The ACNT-H61L is a stretched wide optically coupled optocoupler that combines a light-emitting diode and an integrated high gain photo detector to address low power need for isolated interface. The optocoupler consumes extremely low power, at maximum 2 mA across temperature. The LED forward current operates from 4.5 mA.

This optocoupler supports both 3.3 V and 5 V supply voltage with guaranteed AC and DC operational parameters from temperature range -40 °C to +105 °C. The output of the detector IC is a CMOS output. The internal Faraday shield provides a guaranteed common mode transient immunity specification of 20 kV/μs.

ACNT-H61L of 14.2 mm creepage/clearance and high voltage insulation capability suit for isolated communicate logic interface and control in high-voltage power systems such as 690 V<sub>AC</sub> drives, renewable inverters, medical equipment.

### Functional Diagram



### TRUTH TABLE (POSITIVE LOGIC)

| LED | OUTPUT V <sub>o</sub> |
|-----|-----------------------|
| ON  | L                     |
| OFF | H                     |

A 0.1 μF bypass capacitor must be connected between pins V<sub>DD</sub> and GND

### Features

- Low I<sub>DD</sub> power supply consumption: 2 mA max.
- Input current capability: 4.5 mA min.
- Package: Stretched SO-8
- 20 kV/μs minimum Common Mode Rejection (CMR) at V<sub>CM</sub> = 1000 V
- High Speed: 10 MBd min.
- Guaranteed AC and DC performance over wide temperature: -40 °C to +105 °C
- Safety Approval (Pending)
  - UL 1577 recognized - 7500 V<sub>rms</sub> for 1 minute
  - CSA Approval
  - IEC/EN 60747-5-5 V<sub>IORM</sub> = 2262 V<sub>peak</sub> for Reinforced Insulation

### Applications

- Communication Interface: RS-485, CAN Bus
- Digital isolation for A/D, D/A conversion
- High-voltage power systems, e.g., 690 V drives
- Renewable energy inverters
- Medical imaging and patient monitoring

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.

## Ordering Information

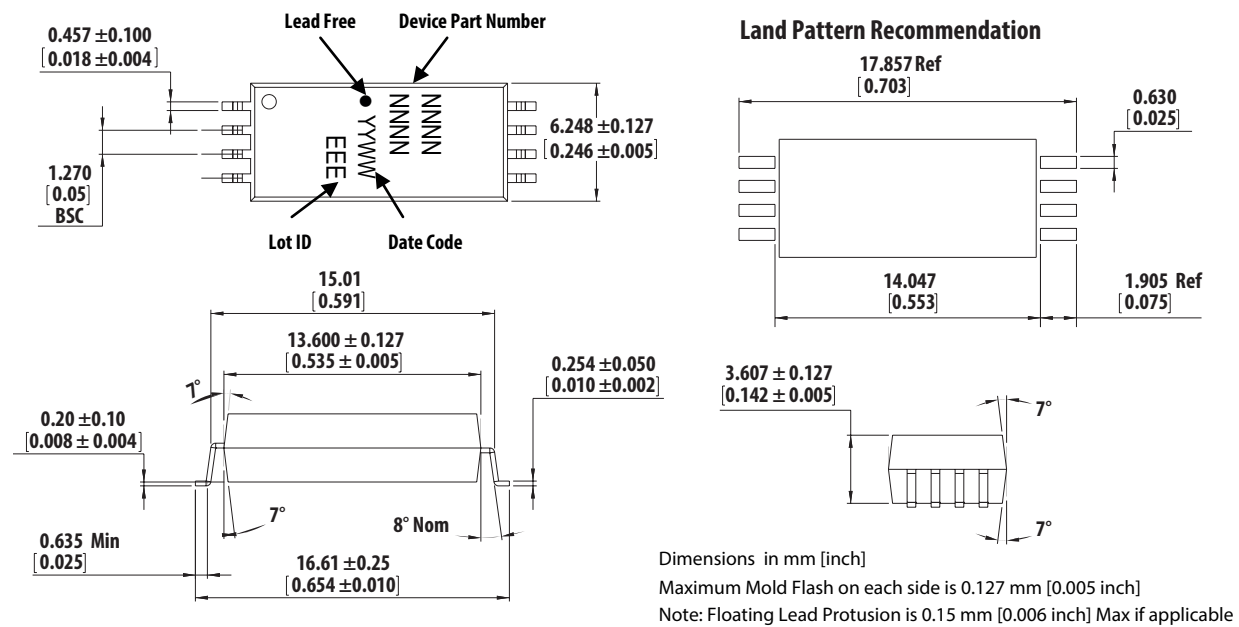
ACNT-H61L is UL Recognized with 7500 V<sub>rms</sub> for 1 minute per UL 1577.

| Part Number | Option         |               | Surface Mount | Tape & Reel | UL 1577 | IEC/EN 60747-5-5 | Quantity      |
|-------------|----------------|---------------|---------------|-------------|---------|------------------|---------------|
|             | RoHS Compliant | Package       |               |             |         |                  |               |
| ACNT-H61L   | -000E          | 14.2 mm       | X             |             | X       | X                | 80 per tube   |
|             | -500E          | Stretched S08 | X             | X           | X       | X                | 1000 per reel |

To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

## Package Outline Drawing

### ACNT-H61L Stretched S0-8 Package



## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

The ACNT-H61L is pending approval by the following organizations:

| IEC/EN 60747-5-5 |   |
|------------------|---|
| <b>UL</b>        | Approval under UL 1577, component recognition program up to V <sub>ISO</sub> = 7500 V <sub>RMS</sub> File E55361. |
| <b>CSA</b>       | Approval under CSA Component Acceptance Notice #5, File CA 88324.   |

## Insulation and Safety Related Specifications

| Parameter  | Symbol | ACNT-H61L | Unit | Conditions   |
|--|--------|-----------|------|--|
| Minimum External Air Gap<br>(External Clearance)     | L(101) | 14.2      | mm   | Measured from input terminals to output terminals, shortest distance through air.  |
| Minimum External Tracking<br>(External Creepage)     | L(102) | 14.2      | mm   | Measured from input terminals to output terminals, shortest distance path along body.  |
| Minimum Internal Plastic Gap<br>(Internal Clearance) |        | 0.5       | mm   | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance<br>(Comparative Tracking Index)  | CTI    | >300      | V    | DIN IEC 112/VDE 0303 Part 1  |
| Isolation Group                                      |        | IIIa      |      | Material Group (DIN VDE 0110, 1/89, Table 1)   |

## IEC/EN 60747-5-5 Insulation Characteristics\*

| Description   | Symbol          | Characteristic   | Unit        |
|---|-----------------|------------------|-------------|
| Installation classification per DIN VDE 0110/39, Table 1<br>for rated mains voltage $\leq 600 V_{rms}$<br>for rated mains voltage $\leq 1000 V_{rms}$ |                 | I – IV<br>I – IV |             |
| Climatic Classification   |                 | 40/105/21        |             |
| Pollution Degree (DIN VDE 0110/39)  |                 | 2                |             |
| Maximum Working Insulation Voltage  | $V_{IORM}$      | 2262             | $V_{peak}$  |
| Input to Output Test Voltage, Method b*<br>$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC     | $V_{PR}$        | 4241             | $V_{peak}$  |
| Input to Output Test Voltage, Method a*<br>$V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC          | $V_{PR}$        | 3619             | $V_{peak}$  |
| Highest Allowable Overvoltage<br>(Transient Overvoltage $t_{ini} = 60$ sec)   | $V_{IOTM}$      | 12000            | $V_{peak}$  |
| Safety-limiting values – maximum values allowed in the event of a failure.  |                 |                  |             |
| Case Temperature  | $T_S$           | 150              | $^{\circ}C$ |
| Input Current   | $I_{S, INPUT}$  | 400              | mA          |
| Output Power  | $P_{S, OUTPUT}$ | 1000             | mW          |
| Insulation Resistance at $T_S$ , $V_{IO} = 500$ V   | RS              | $> 10^9$         | $\Omega$    |

\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

## Absolute Maximum Ratings

| Parameter                         | Symbol        | Min   | Max          | Units | Condition                                      |
|-----------------------------------|---------------|---|--------------|-------|--|
| Storage Temperature               | $T_S$         | -55   | 125          | °C    |  |
| Operating Temperature             | $T_A$         | -40   | 105          | °C    |  |
| Reverse Input Voltage             | $V_R$         |   | 5            | V     |  |
| Supply Voltage                    | $V_{DD}$      |   | 6.5          | V     |  |
| Average Forward Input Current     | $I_F$         | -   | 10           | mA    |  |
| Peak Forward Input Current        | $I_{F(TRAN)}$ | -   | 1            | A     | <1 $\mu$ s Pulse Width, <300 pulses per second |
|                                   |               |   | 80           | mA    | <1 $\mu$ s Pulse Width, <10% Duty Cycle        |
| Output Current                    | $I_O$         |   | 10           | mA    |  |
| Output Voltage                    | $V_O$         | -0.5  | $V_{DD}+0.5$ | V     |  |
| Input Power Dissipation           | $P_I$         |   | 20           | mW    |  |
| Output Power Dissipation          | $P_O$         |   | 22           | mW    |  |
| Lead Solder Temperature           | TLS           | 260°C for 10 sec., 1.6 mm below seating plane |              |       |  |
| Solder Reflow Temperature Profile |               | Refer to Solder Reflow Profile section        |              |       |  |

## Recommended Operating Conditions

| Parameter                 | Symbol       | Min | Max | Units   |
|---------------------------|--------------|-----|-----|---------|
| Operating Temperature     | $T_A$        | -40 | 105 | °C      |
| Input Current, Low Level  | $I_{FL}$     | 0   | 250 | $\mu$ A |
| Input Current, High Level | $I_{FH}$     | 4.5 | 8   | mA      |
| Power Supply Voltage      | $V_{DD}$     | 2.7 | 5.5 | V       |
| Forward Input Voltage     | $V_{F(OFF)}$ |     | 0.8 | V       |

## Electrical Specifications (DC)

Over recommended temperature ( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ), supply voltage ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ). All typical specifications are at  $V_{DD} = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$

| Parameter                           | Symbol                    | Min            | Typ      | Max  | Units | Test Conditions  | Figure |
|-------------------------------------|---------------------------|----------------|----------|------|-------|--|--------|
| Input Forward Voltage               | $V_F$                     | 1.20           | 1.38     | 1.85 | V     | $I_F = 7\text{ mA}$  | 1, 2   |
| Input Reverse Breakdown Voltage     | $BV_R$                    | 7              |          |      | V     | $I_R = 10\text{ }\mu\text{A}$  |        |
| Logic High Output Voltage           | $V_{OH}$                  | $V_{DD} - 0.1$ | $V_{DD}$ |      | V     | $I_F = 0\text{ mA}$ , $V_I = 0\text{ V}$ ,<br>$I_O = -20\text{ }\mu\text{A}$               |        |
|                                     |                           | $V_{DD} - 1.0$ | $V_{DD}$ |      | V     | $I_F = 0\text{ mA}$ , $V_I = 0\text{ V}$ ,<br>$I_O = -3.2\text{ mA}$                       |        |
| Logic Low Output Voltage            | $V_{OL}$                  |                | 0.02     | 0.1  | V     | $I_F = 7\text{ mA}$ , $V_I = 5\text{ V} / 3.3\text{ V}$ ,<br>$I_O = 20\text{ }\mu\text{A}$ |        |
|                                     |                           |                | 0.2      | 0.4  | V     | $I_F = 7\text{ mA}$ , $V_I = 5\text{ V} / 3.3\text{ V}$ ,<br>$I_O = 3.2\text{ mA}$         |        |
| Input Threshold Current             | $I_{TH}$                  |                | 0.7      | 3.8  | mA    |  | 3      |
| Logic Low Output Supply Current     | $I_{DDL}$                 |                | 1        | 2    | mA    |  | 4      |
| Logic High Output Supply Current    | $I_{DDH}$                 |                | 1        | 2    | mA    |  | 5      |
| Input Capacitance                   | $C_{IN}$                  |                | 20       |      | pF    | $f = 1\text{ MHz}$ , $V_F = 0\text{ V}$  |        |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ |                | -1.5     |      | mV/°C | $I_F = 7\text{ mA}$  |        |

## Switching Specifications (AC)

Over recommended temperature ( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ), supply voltage ( $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ). All typical specifications are at  $V_{DD} = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$

| Parameter   | Symbol    | Min | Typ | Max | Units             | Test Conditions  |
|---|-----------|-----|-----|-----|-------------------|--|
| Propagation Delay Time to Logic Low Output <sup>[1]</sup>                 | $t_{PHL}$ |     | 40  | 100 | ns                | $I_F = 7\text{ mA}$ , $V_I = 3.3 / 5\text{ V}$ , $C_L = 15\text{ pF}$ , CMOS Signal Levels.  |
| Propagation Delay Time to Logic High Output <sup>[1]</sup>                | $t_{PLH}$ |     | 40  | 100 | ns                | Figure 6, 7, 8, 9  |
| Pulse Width   | $t_{PW}$  | 100 |     |     | ns                |  |
| Pulse Width Distortion <sup>[2]</sup>                                     | PWD       |     | 5   | 40  | ns                |  |
| Propagation Delay Skew <sup>[3]</sup>                                     | $t_{PSK}$ |     |     | 40  | ns                |  |
| Output Rise Time (10% – 90%)  | $t_R$     |     | 10  |     | ns                |  |
| Output Fall Time (90% - 10%)  | $t_F$     |     | 10  |     | ns                |  |
| Static Common Mode Transient Immunity at Logic High Output <sup>[4]</sup> | $ CM_H $  | 20  | 35  |     | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$ , $I_F = 0\text{ mA}$ , $V_I = 0\text{ V}$ , $C_L = 15\text{ pF}$ , CMOS Signal Levels.                        |
| Static Common Mode Transient Immunity at Logic Low Output <sup>[5]</sup>  | $ CM_L $  | 20  | 35  |     | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$ , $I_F = 7\text{ mA}$ , $V_I = 5\text{ V} / 3.3\text{ V}$ , $C_L = 15\text{ pF}$ , CMOS Signal Levels.         |
| Dynamic Common Mode Transient Immunity <sup>[6]</sup>                     | CMRD      |     | 35  |     | kV/ $\mu\text{s}$ | $V_{CM} = 1000\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$ , $I_F = 7\text{ mA}$ , $V_I = 5\text{ V} / 3.3\text{ V}$ , 10MBd datarate, the absolute increase of PWD <10ns |

## Package Characteristics

All typical at  $T_A = 25\text{ }^\circ\text{C}$ .

| Parameter                | Symbol    | Min  | Typ       | Max | Units            | Test Conditions                                       |
|--------------------------|-----------|------|-----------|-----|------------------|---|
| Input-Output Insulation  | $V_{ISO}$ | 7500 |           |     | V <sub>rms</sub> | RH < 50% for 1 min. $T_A = 25\text{ }^\circ\text{C}$  |
| Input-Output Resistance  | $R_{I-O}$ |      | $10^{12}$ |     | $\Omega$         | $V_{I-O} = 500\text{ V}$                              |
| Input-Output Capacitance | $C_{I-O}$ |      | 0.6       |     | pF               | $f = 1\text{ MHz}$ , $T_A = 25\text{ }^\circ\text{C}$ |

Notes:

- $t_{PHL}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_F$ ) on the rising edge of the input pulse to the 50%  $V_{DD}$  of the falling edge of the  $V_O$  signal.  $t_{PLH}$  propagation delay is measured from the 50% ( $V_{in}$  or  $I_F$ ) on the falling edge of the input pulse to the 50% level of the rising edge of the  $V_O$  signal.
- PWD is defined as  $|t_{PHL} - t_{PLH}|$ .
- $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature within the recommended operating conditions.
- $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- $CM_L$  is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.
- CMRD is the maximum tolerable rate of the common mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10ns.

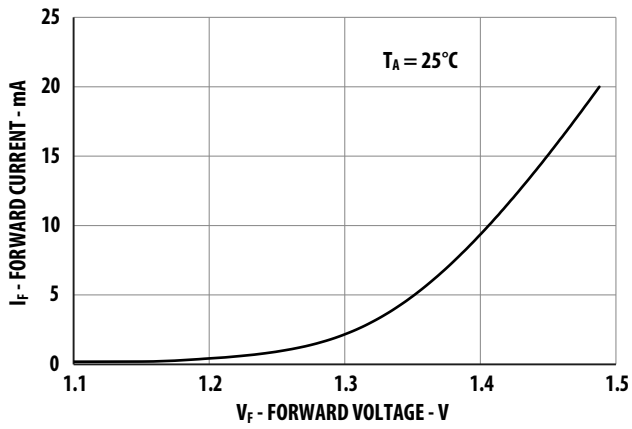


Figure 1. Typical input diode forward characteristic

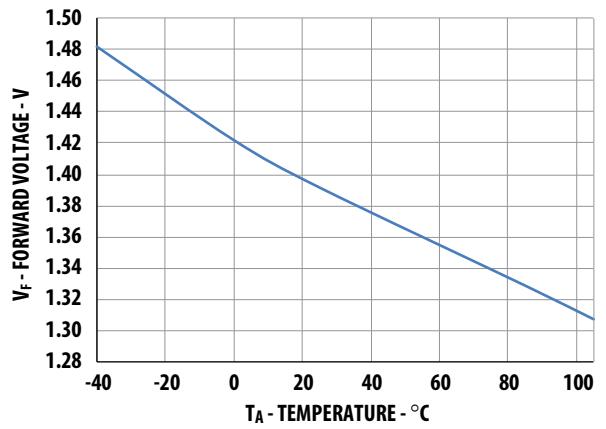


Figure 2. Typical  $V_F$  versus temperature

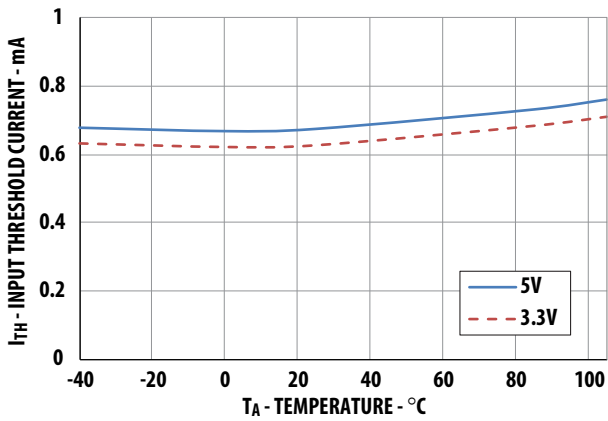


Figure 3. Typical input threshold current  $I_{TH}$  versus temperature

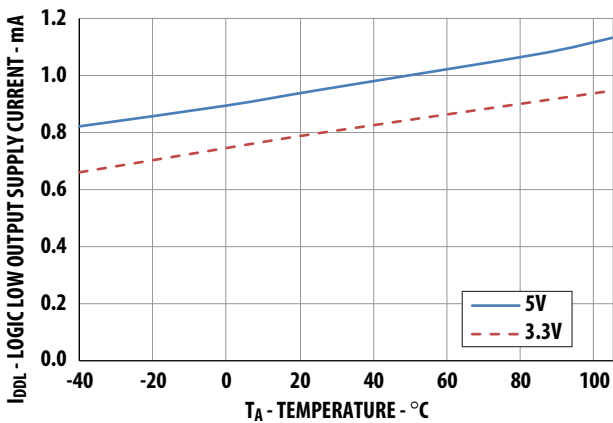


Figure 4. Typical logic low output supply current  $I_{DDL}$  versus temperature

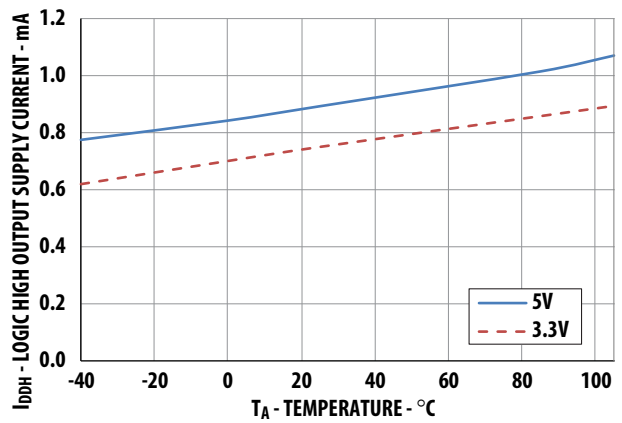


Figure 5. Typical logic high output supply current  $I_{DDH}$  versus temperature

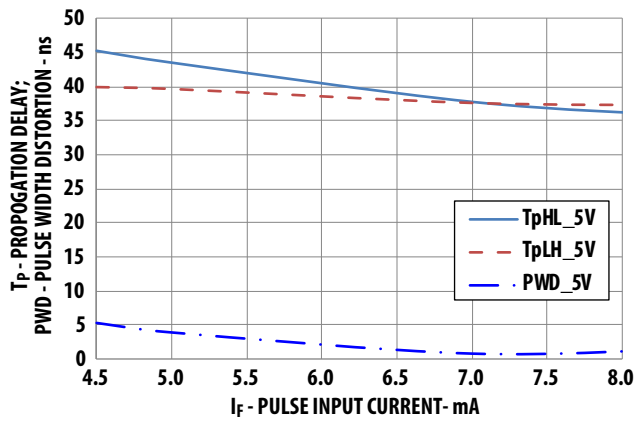


Figure 6. Typical switching speed versus pulse input current at 5V supply voltage

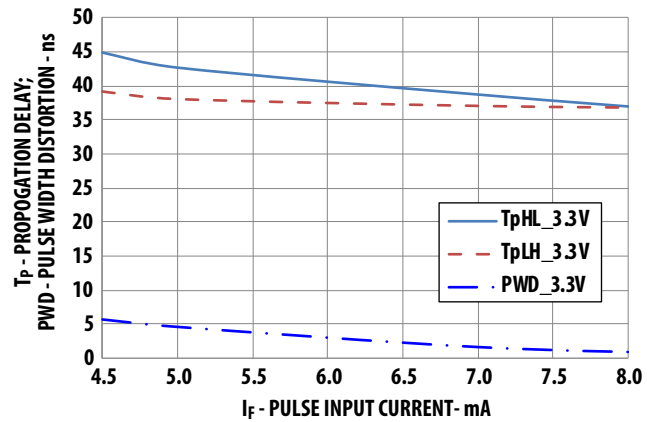


Figure 7. Typical switching speed versus pulse input current at 3.3V supply voltage

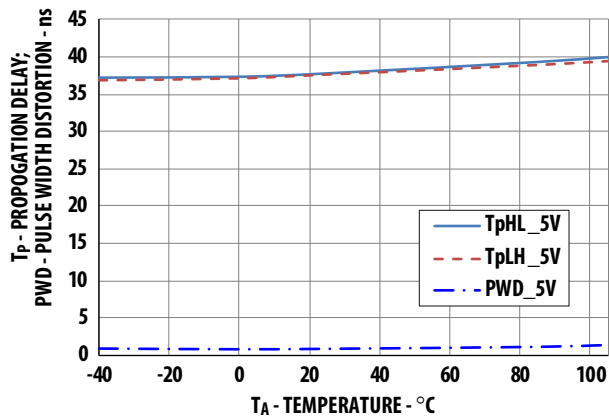


Figure 8. Typical switching speed versus temperature at 5V supply voltage

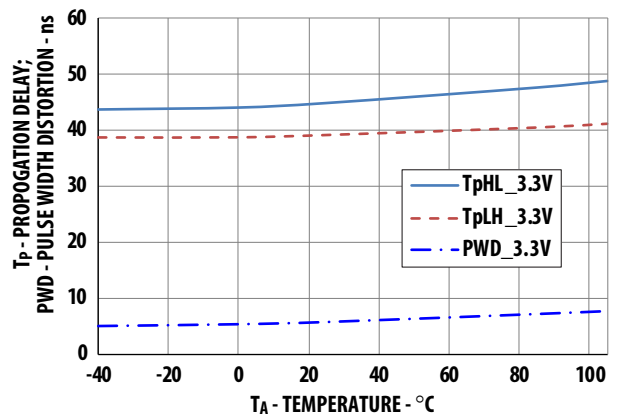


Figure 9. Typical switching speed versus temperature at 3.3V supply voltage

## Bypassing and PC Board Layout

The external components required for proper operation are the input limiting resistors and the output bypass capacitor. Capacitor values should be 0.1  $\mu\text{F}$ .

For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm.

## Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high ( $t_{PLH}$ ) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low ( $t_{PHL}$ ) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 10).

Pulse-width distortion (PWD) results when  $t_{PLH}$  and  $t_{PHL}$  differ in value. PWD is defined as the difference between  $t_{PLH}$  and  $t_{PHL}$  and often PWD is defined as the difference between  $t_{PLH}$  and  $t_{PHL}$ . This parameter determines the

maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD in the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew,  $t_{PSK}$ , is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either  $t_{PLH}$  or  $t_{PHL}$ , for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time,  $t_{PSK}$  is the difference between the shortest propagation delay, either  $t_{PLH}$  or  $t_{PHL}$ , and the longest propagation delay, either  $t_{PLH}$  or  $t_{PHL}$ . As mentioned earlier,  $t_{PSK}$  can determine the maximum parallel data transmission rate.

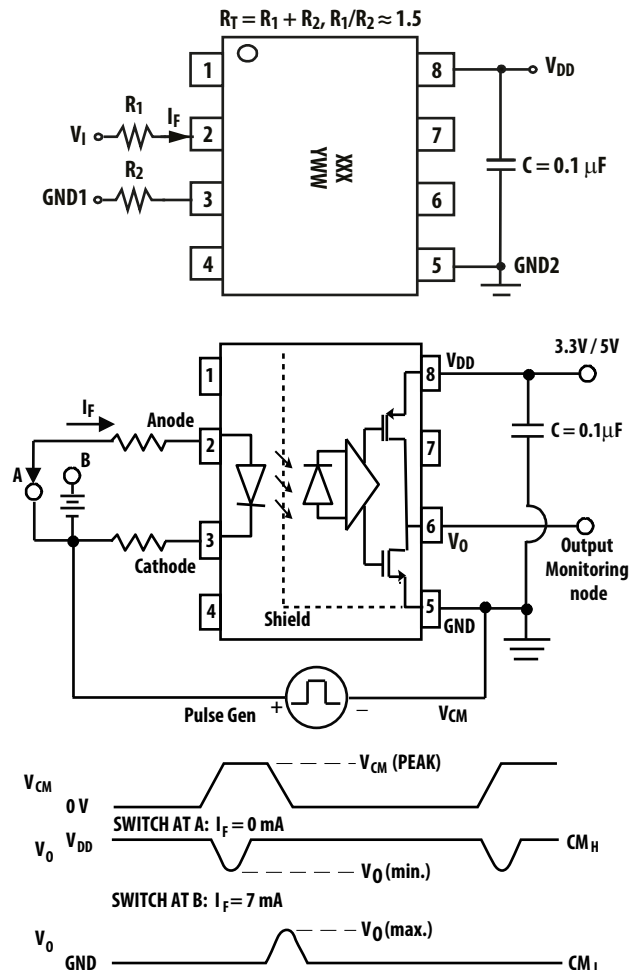


Figure 10. Recommended printed circuit board layout

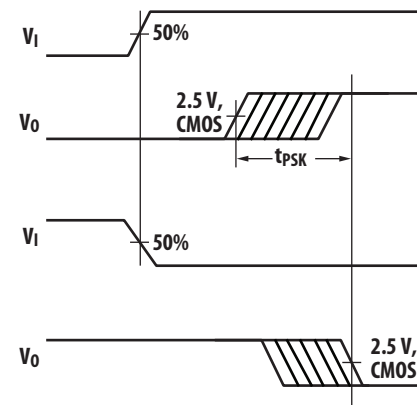


Figure 11. Propagation delay skew waveform

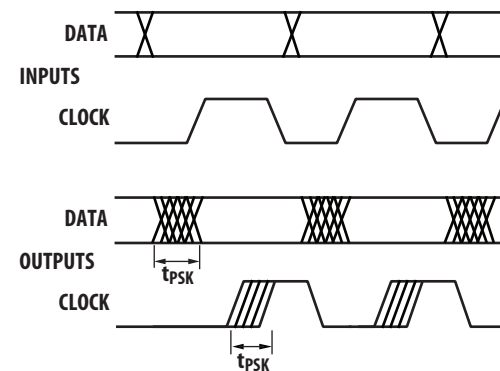


Figure 12. Parallel data transmission example



Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice  $t_{PSK}$ . A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The  $t_{PSK}$  specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

### **Optocoupler CMR performance**

The principal protection against common mode noise comes down to the fundamental isolation properties of the optocoupler, this in turn is directly related to the input-output leakage capacitance of the optocoupler.

To provide maximum protection to circuitry connected to the input or output of the optocoupler the leakage capacitance is minimized by having large separation distances at all points in the optocoupler construction, including the LED/photodiode interface.

In addition to the constructional design, additional circuit design steps are taken to further mitigate the effects of common mode noise. The most important of these is the use of a Faraday shield on the photodetector stage. This Faraday shield is effective in optocouplers because the internal modulation frequency (light) is many orders of magnitude higher than the common mode noise frequency.

### **Application level CMR Performance**

In application, it is desirable that the optocoupler's common mode isolation perform as close as possible to that indicated in the data sheets specifications.

The first step in meeting this goal is to ensure maintaining maximum separation between PCB interconnects on either side of the optocoupler and avoid routing tracks beneath the optocoupler. Nonetheless, it is inevitable that a certain amount of CMR noise will be coupled into the inputs which can potentially result in false-triggering of the input.

This problem is frequently observed in devices with input high input impedance such as CMOS buffered inputs in either optocoupler or alternate isolator technologies. In some cases, this not only causes momentary missing pulses but in some technologies may even cause input circuitry to latch-up.

The ACNT-H61L does not face input latch up issue even at very high CMR levels, such as those experienced in end equipment level tests (for example IEC 61000-4-4) due to the simple diode structure of the LED.

In some cases achieving the rated data sheet CMR performance levels is not possible in the intended application, often because of the practical need to actually connect the isolator input to the output of a dynamically changing signal rather than tying the input statically to VDD1 or GND1.

This specsmanship issue is often observable with alternate isolators utilizing AC encoding techniques.

To address this requirement for clear transparency on the achievable end application performance, the ACNT-H61L optocoupler includes an additional typical performance indication of the dynamic CMR in the electrical parameter table. What this information indicates is the achievable CMR performance whilst the input is being toggled on or off during the occurrence of a CMR transient. The logic output of the optocoupler is mainly controlled by the level of the LED current due to the short transition rise/fall time of the LED current (approximately 10ns), the dynamic noise immunity is essentially the same as the static noise immunity.

To achieve this goal of meeting the maximum inherent CMR capabilities some simple consideration needs to be given to the operation of the LED at the application level.

In particular ensuring that the LED stays either on or off during a CMR transient.

Some common design techniques which are sometimes used to meet this goal:

Keeping LED On:

i) Overdrive the LED with a higher than required forward current.

Keeping LED Off:

i) Reverse bias the LED during the off state.

ii) Minimize the off state impedance across the anode and cathode of the LED during the off state.

All these methods are fully capable of enabling the full CMR capabilities of the ACNT-H61L to be achieved. But they do come at the cost of practical implementation issues or a compromise on power consumption.

An effective method to meet the goal of maintaining the LED status during a CMR event with no other design compromises other than the addition of a single low cost component (resistor).

This CMR optimization method fundamentally makes use of the differential input capability of the LED input. By ensuring the common mode impedance on both the cathode and anode of the LED are balanced, it effectively nullifies the effect of a CMR transient on the LED. This is most easily achieved by splitting the input bias resistor into two (as shown in Figure 10).

### Split resistor configuration

Figure 13 shows the recommended drive circuit for the ACNT-H61L for optimal common-mode rejection performance. Two LED-current setting resistors are used to balance the common mode impedance at LED anode and cathode. Common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 14 shows the parasitic capacitances which exist between LED anode/cathode and output ground ( $C_{LA}$  and  $C_{LC}$ ).

Table 1 indicates the directions of  $I_{LP}$  and  $I_{LN}$  flow depending on the direction of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CML, since the output is in the “low” state) depends upon the amount of LED current drive ( $I_F$ ). For conditions where  $I_F$  is close to the switching threshold ( $I_{TH}$ ), CML also depends on the extent which  $I_{LP}$  and  $I_{LN}$  balance each other. In other words, any condition where common-mode transients cause a momentary decrease in  $I_F$  (i.e. when  $dV_{CM}/dt > 0$  and  $|I_{FP}| > |I_{FN}|$ , referring to Table 1) will cause common-mode failure for transients which are fast enough.

Likewise for common-mode transients which occur when the LED is off (i.e.  $CM_H$ , since the output is “high”), if an imbalance between  $I_{LP}$  and  $I_{LN}$  results in a transient  $I_F$  equal to or greater than the switching threshold of the optocoupler, the transient “signal” may cause the output to spike below 2 V (which constitutes a  $CM_H$  failure).

The balanced  $I_{LED}$ -setting resistors help equalize the common mode voltage change at anode and cathode to reduce the amount by which  $I_{LED}$  is modulated from transient coupling through  $C_{LA}$  and  $C_{LC}$ .

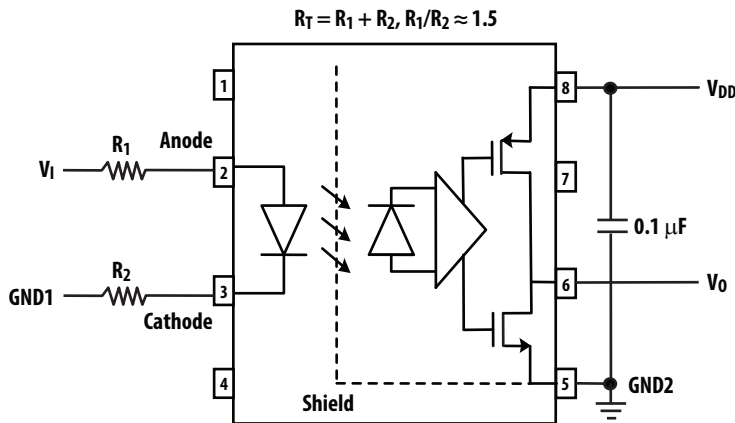


Figure 13. Recommended drive circuit for high-CMR

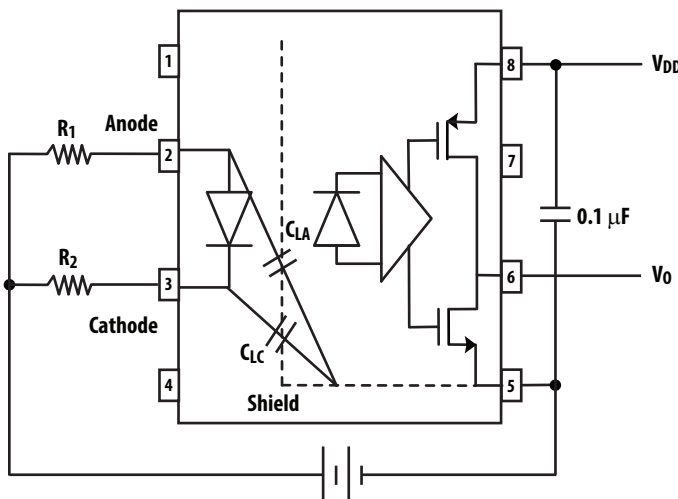


Figure 14. AC equivalent of ACNT-H61L

**Table 1. Effects of Common Mode Pulse Direction on Transient  $I_{LED}$** 

| <b>If <math>dV_{CM}/dt</math> Is:</b> | <b>then <math>I_{LP}</math> Flows:</b>  | <b>and <math>I_{LN}</math> Flows:</b>     | <b>If <math> I_{LP}  &lt;  I_{LN} </math>,<br/>LED <math>I_F</math> Current<br/>Is Momentarily:</b> | <b>If <math> I_{LP}  &gt;  I_{LN} </math>,<br/>LED <math>I_F</math> Current<br/>Is Momentarily:</b> |
|---------------------------------------|---|---|---|---|
| positive ( $>0$ )                     | away from LED<br>anode through $C_{LA}$ | away from LED<br>cathode through $C_{LC}$ | increased   | decreased   |
| negative ( $<0$ )                     | toward LED<br>anode through $C_{LA}$    | toward LED<br>cathode through $C_{LC}$    | decreased   | increased   |

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.  
Data subject to change. Copyright © 2005-2014 Avago Technologies. All rights reserved.  
AV02-4677EN - December 16, 2014

