

ADS5292, 8-Channel, Analog-to-Digital Converter Evaluation Module

This user's guide gives a general overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS5292 analog-to-digital converters (ADC), which collectively are referred to as ADS529x. Use this document in combination with the respective ADC data sheet. The ADS529xEVM provides a platform for evaluating the ADC under various signal, clock, reference, and power supply conditions.

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1 Quick View of Evaluation Setup

Figure 1 shows an overview of the evaluation setup that includes the ADS5292EVM evaluation module (EVM), TSW1250EVM, external equipment, personal computer (PC), and software requirements.

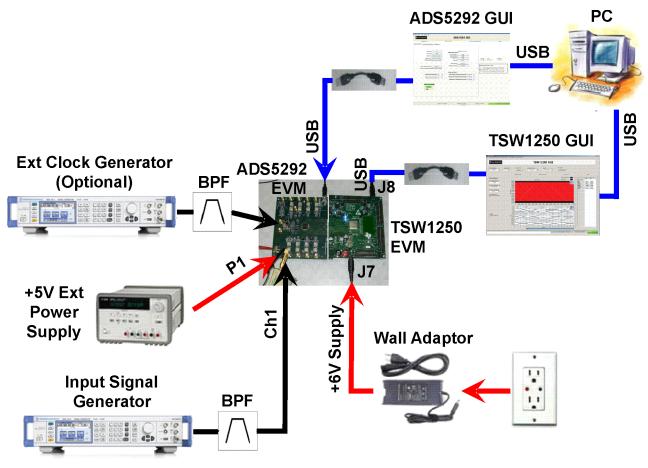


Figure 1. Evaluation Setup

TSW1250EVM: The high-speed LVDS de-serializer board is required for capturing data from the ADS5292EVM and its analysis using the TSW1250 graphical user interface (GUI).

For more information pertaining to be TSW1250EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1250evm.html.

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock (optional) in order to get the desired performance. Additionally, band-pass filters (BPF) are required in signal and clock (optional) paths to attenuate the harmonics and noise from the generators.

Power Supply: A single +5-V supply powers the ADS5292EVM. The supplies for the ADS5292 device are derived from the +5-V supply. The power supply must be able to source up to 1.5 A. A +6-V supply can power the TSW1250EVM using a wall adapter.

USB Interface to PC: The USB connection from the ADS5292EVM and TSW1250EVM to the personal computer (PC) must be set up; Section 3.2 explains the USB driver installation.

ADS5292GUI: Section 3.1 explains the GUI installation procedure and its operation.



Default Configuration

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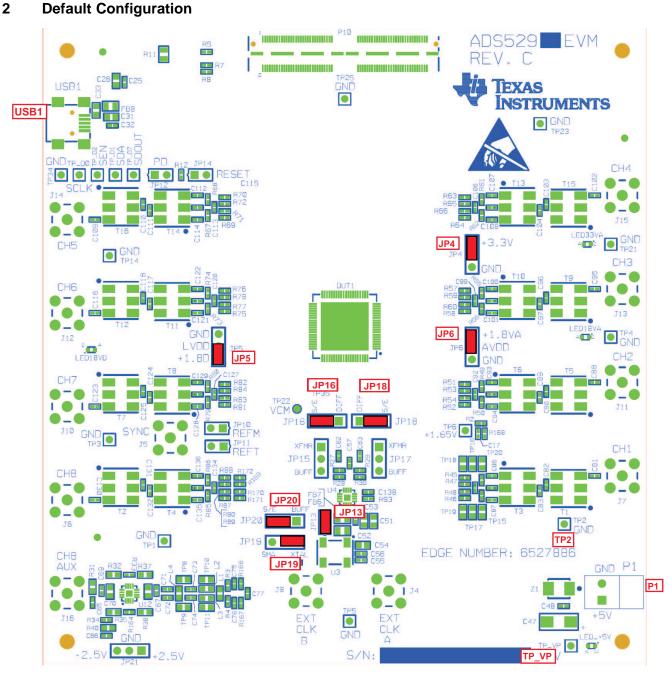
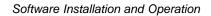


Figure 2. ADS5292EVM Basic Configuration

- 1. The ADS5292EVM basic configuration uses the onboard single-ended clock as the default option. See Section 9.2 for the ADC clock, various-mode jumper settings.
- 2. P1: +5-V Power supplies the connector.
- 3. JP4, JP5, and JP6 are set to enable +3.3V Analog, +1.8VD Digital, and +1.8VA Analog to device, respectively.
- 4. JP13: Enable onboard CMOS clock.
- 5. JP16, JP18, JP19, JP20: ADC clock source selection jumpers.

3 Software Installation and Operation

The ADS5292EVM comes with a software installation CD; run setup.exe to install the software.





3.1 GUI Installation – Mandatory

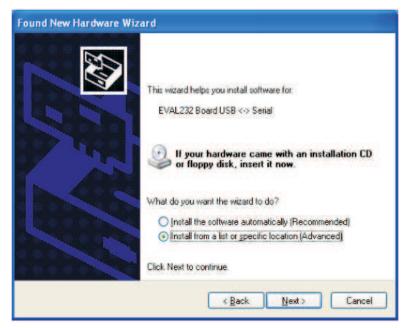
Unzip the installer file in the CD. Run setup.exe to install the GUI.

3.2 USB Interface Driver Installation

- · Connect the USB port of EVM to your PC.
- If the driver has not been installed, then the message *Window Found New Hardware* appears. The Wizard as shown in the following illustration launches. Otherwise, skip Section 3.2 and go to Section 4.
- Select No, not this time from the options. Press Next button

Found New Hardware Wizard		
	Welcome to the Found New Hardware Wizard Windows will search for current and updated software by looking on your computer, on the hardware installation CD, or on the Windows Update Web site (with your permission). Read our privacy policy	
	Can Windows connect to Windows Update to search for software? Yes, this time only Yes, now and every time I connect a device No, not this time Click Next to continue	
	Reack Next > Cancel	

• Select Install from a list or specific location (Advanced) as shown in the following illustration, and then click Next.



• Select Search for the best driver in these locations, and enter the file path for (C:\Program Files\Texas Instruments\ADS 5292\CDM 2.04.06 WHQL Certified) in the combo-box. or browse to it by clicking the



browse button. Once the file path has been entered in the box, click Next to proceed.

• If Windows[™] XP is configured to warn when unsigned (non-WHQL certified) drivers are about to be installed, the following screen is displayed unless installing a Microsoft[™] WHQL-certified Driver. Click on *Continue Anyway* to continue with the installation. If Windows XP is configured to ignore file signature warnings, no message appears.



4 Test Setup

6

To evaluate the ADS5292 device, a TSW1250EVM is required. Figure 3 shows the exact setup of these two boards and external connectors.

- Connect +5-V supply at P1 connector or across TP_VP (+5V) and TP2 (GND).
- Connect USB cable from PC to **USB1** on ADS5292EVM.
- Connect ADS5292EVM to TSW1250EVM using P10 connector.
- Connect USB cable from PC to USB port **J8** of TSW1250EVM.
- Connect +6-V wall adapter to TSW1250EVM at **J7** connector.

For the default configuration as shown in Figure 2, it is unnecessary to have an external sampling clock. The onboard CMOS clock oscillator is used.



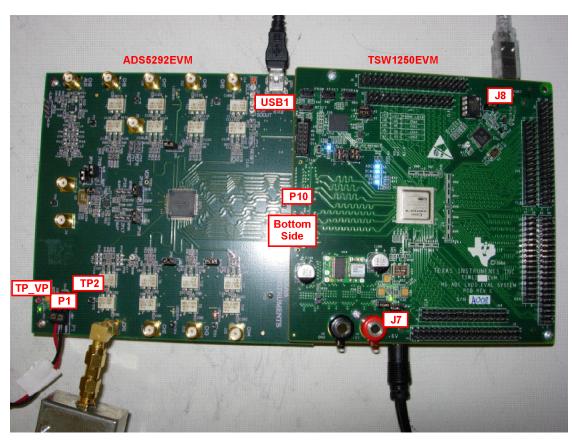


Figure 3. HW Setup With Connection Between TSW1250EVM and ADS5292EVM

5 Power Up ADS5292

After connecting the ADS5292EVM to the TSW1250 using the **P10** connector, +6-V adapter to TSW1250EVM, and +5 V (from the external power supply) to **P1** connector, then power up is complete. Three green LEDs and one orange LED turned on as shown in Figure 4 (also see Figure 13).



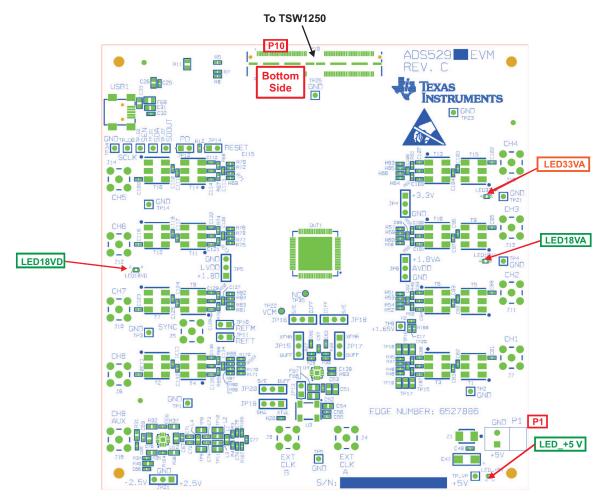


Figure 4. Power-Up Indications

6 Launch ADS5292 GUI

8

After launching the ADS5292 GUI, the GUI appears as is shown in Figure 5. After the GUI is completely launched, the window appears as is displayed in Figure 5. Select the **Top Level** tab to observe the default condition. The bottom status bar indicates *Ready for new command* and green (highlighted). Click on checkbox **PD** twice, and select it for power down to ensure proper software link to the hardware by observing change in current reading (approximately 450 mA to 150 mA) of the external +5-V power supply. For the rest of the test, **PD** must be unchecked. Click on **Soft Reset** button to reset device internally.



MENTS ADS	5 5292 GUI
Bit Window Belp MENTS ADDS Read Me First Interface Dig Sig Proc Dig Sig Proc_FLTR IN/OUTP Map Deb Interface Dig Sig Proc Dig Sig Proc_FLTR IN/OUTP Map Deb Clock Mode Single Ended PDN_COMPLETE PDN_COMPLETE Low Jakter Mode Disabled PDN_PIN_CFG Ext Reference REFT/REFB PDN by Channel FDN_CH1 PDN_CH1 PDN_CH2 PDN_CH2 Data Format Offset Binary MSB_LSB LSB-first PDN_CH4 PDN_CH4 PDN_CH4 PDN_CH4 PDN_CH5 SDR Output Mode Disable SDR Dutput Mode Disable PDN_CH4	SAVE COMMAND SEQUENCE

Figure 5. ADS5292 GUI Launch



Launch ADS5292 GUI

After GUI launch and verification of software communication with EVM, click on button **EN_2WIRE**. This configures the ADC output interface in **2-WIRE LVDS** mode. Also click button **LVDS Output** to set ADC in **12 Bits** mode. Ensure that the **MSB_LSB** button status shows **LSB_First**.

Bit Day of the line Image: Section of the line Read Mc Field Image: Section of the line Image: Section of the line<
High Level Text
Top Level Test Pattern Interface By Sig Proc. PLTR PV(PUDTP Hap Dedug APXY 67 DBAADAT PPA, SARTIAL: PA, SARTIAL: PPA, SARTIAL: PA, SART
PON (7 (100AR)*) PON. 90 Dock Mode Single Ended PON. 17 (100AR)* PON. 90 Dock Mode Bisbled PON. 17 (100AR)* PON. 90 Dock Mode Bisbled PON. 17 (100AR)* PON. 90 Dock Mode Bisbled PON. 17 (100AR)* PON. 90 Dock Mode Disbled PON. 17 (100AR)* PON. 90 Dock Mode Disbled PON. 17 (100AR)* PON. 90 PON. 17 (100AR)* PON. 90 PON. 17 (100AR)* PON. 90 PON. 100 (100 PON. 90 PON. 2010 PON. 2010 PON. 2010 PON. 2010 PON. 2017 PON. 2017 PON. 2016 PON. 2016 PON. 2016 PON. 2017 PON. 2016 PON. 2016 SOR Output Mode Son Hexet Off Son Reset Off Son Reset PON. 2016 YON 50 Uput T2805 Son Reset Off Son Reset Off Son Reset Off



7 Launch TSW1250 GUI

Launch TSW1250 GUI. The **Message** window displays this message to indicate that the setup of the TSW1250EVM and ADS5292EVM is working properly. If a different message or an error message appears, contact TI FAE.

- 1. Select ADS5292_2W, 12bits, from the GUI.
- 2. Select LSB First.
- 3. ADC Sampling Rate (Fs) is fixed at 80 MHz; this is the onboard CMOS clock frequency.
- 4. **ADC Input Frequency** enter 10M and the GUI calculates the real coherent frequency (Fc) to 10.02441406M.

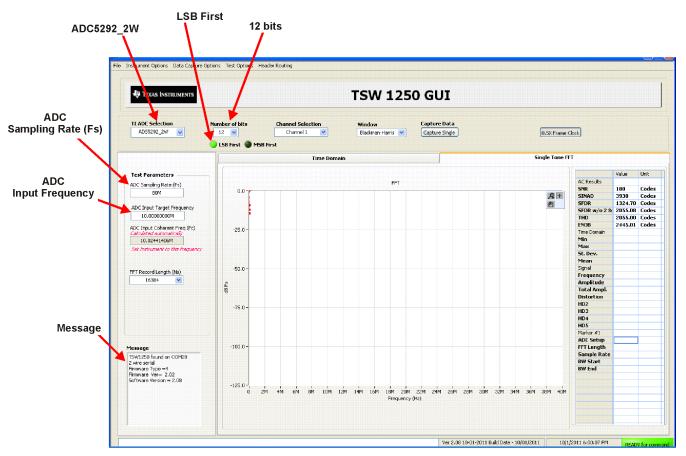


Figure 6. TSW1250 GUI Launch



8 TEST ADS5292

8.1 Step 1: Time Domain

- Select Time Domain page from TSW1250 GUI.
- Uncheck Overlay unwrap waveform.

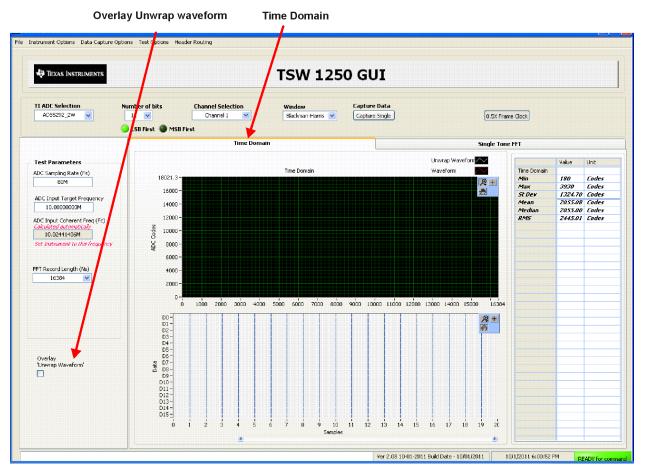


Figure 7. ADS5292 Time Domain Setup



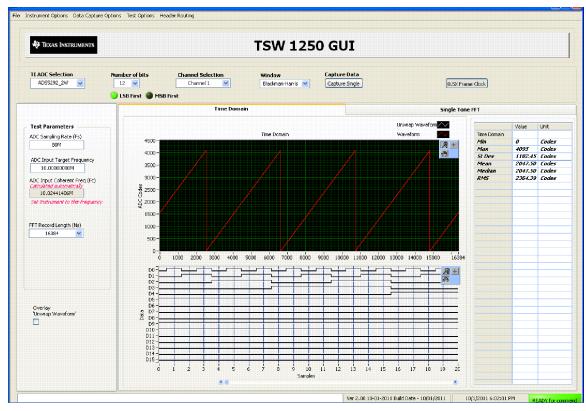
• From ADS5292 GUI, go to Test Pattern page, then select RAMP PATTERN.

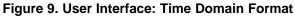
RAMP PATTERN

xas Instruments		ADS 5292 GUI	
Read M	le First		High Level Test
I Test Pattern Interface Dig Sig Pro	oc Dig Sig Proc_FLTR IN/OUT	P Map Debug	SAVE COMMAND SEQUENCE
			Acceleration acceleration and acceleration acceleratio acceleration acceleration acceleration acceleration ac
			COMMAND SEQUENCE PLAY BACK Commands play back
EN PRBS TEST PATTERN	Enable Pattern Mode	None	
PRBS_MODE_2 24-bit pattern	CUSTOM DAT	RAMP PATTERN	Soving List
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PRBS SEED FROM REG	CUSTOM DAT	DESKEW PATTERN	
PRBS SEED		SYNC PATTERN	
Texespense - carrently			
	RAMP_PAT_RES		
		(0x0000-0x3FFF)	Digital Waveform Graph-Write
			address × 42 Data × 8000
			auures n 12 Duci n 0000
			DEVICE PIN CONTROL

Figure 8. ADS5292 Test Pattern

- Press Capture button on TSW1250 GUI. You observe a ramping waveform on the TSW1250 GUI display area as shown in Figure 9.
- Repeat for Channel 2...Channel 8.
- If each channel has the output as shown in the following illustration, you can proceed with the next step; otherwise, contact the TI FAE (Field Application Engineer) to troubleshoot the problem.
- On the ADS5292 GUI, change Test Pattern to None from RAMP PATTERN for next step.





TEXAS INSTRUMENTS	ADS 5292 GUI	
Read Me Fir		High Level Test
EN PRBS TEST PATTERN PRBS_MODE_2 24-bit pattern	Dig Sig Proc_FLTR IN/OUTP Map Debug Enable Pattern Mode RAMP PATTERN Kore CUSTOM DAI / RAMP PATTERN	SAVE COMMAND SEQUENCE Add add/idsta to saving lix Saving lix to a file COMMAND SEQUENCE PLAY BACK Commands play back Saving lix Commands play back Saving lix
PRBS SEED FROM REG	DUAL CUSTOM PATTERN SUBSEC OXTOM PATTERN DESKEW PATTERN SYNC PATTERN SYNC PATTERN	Index Addr Doto
		SCHX ⁻ IMMUMUMUMUMUMUMUMUM SHATA <u>0</u> SH- address <u>© 25</u> Data <u>© 40</u>



8.2 Step 2: Single Tone FFT

- Select Single Tone FFT page at TSW1250 GUI.
- Connect Channel 1 of ADS5292EVM to a signal generator through a BP filter. If no **BP filter** is presented, the result is not good.
- Set Amplitude of the signal generator to 11.5dBm
- Set Frequency of the signal generator to 10.02441406M to match the GUI.
- Change window option to **Hanning**. This is due to the fact that input signal and onboard CMOS clock are noncoherent.
- Press Capture Single button to get the test result.
- Repeat for Channel 2...Channel 8.

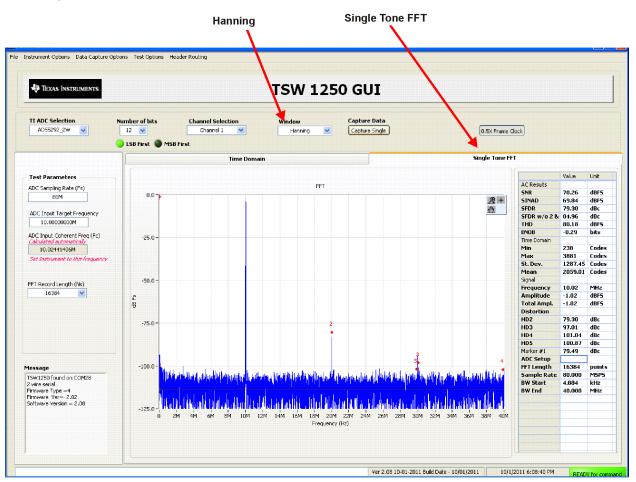


Figure 10. User Interface: Single FFT Format

9 Board Configuration

9.1 Input/Output, Power Supply, and USB

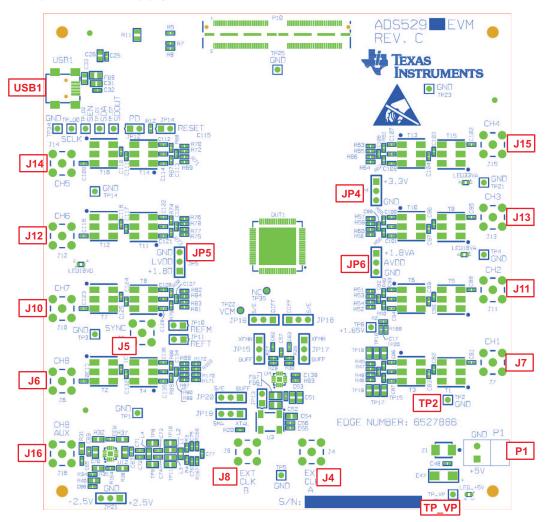


Figure 11. I/O, PWR, and USB Connector

Table 1.	Input/Output,	Power,	and	USB
----------	---------------	--------	-----	-----

Connector	Description
J6,J7,J10J15	Analog Input signals for Ch1-Ch8. Connect to a signal generator. A band-pass filter must be applied between the generator and the SMA to get a better result. (See Figure 3)
J16	It is an alternative input for channel 8. Need to install two resistors (R169 and R170) and remove two resistors(R171 and R172) from J6.
P1/TP_VP	P1 is the +5-V power supply connector. TP_VP is the test point for +5-V power supply.
JP4	Onboard 3.3-V Analog enables. Set up as Figure 2 is a must to use onboard 3.3 V
JP5	Onboard 1.8-V Digital enables. Set up as Figure 2 is a must to use onboard 1.8 V
JP6	Onboard 1.8-V Analog enables. Set up as Figure 2 is a must to use onboard 1.8 V
TP1, TP2, TP3, TP4, TP5, TP14, TP21, TP23, TP25, TP34,	Ground test points.
USB1	USB interface connector

Table 2.	Channel	8	Configuration
	onanioi	-	oonngaraaon

Input Interface Type	Connector	Description
Through Transformer (Default)	J6	In default configuration, R171 and R172 are already populated
Through Amplifier (Not Default)	J16	It is an alternative input for channel 8. Need to install two resistors (R169 and R170) and remove two resistors(R171 and R172) from J6.It uses TI THS4509 single-ended to differential amplifier.



9.2 ADC Clock

Five options are available for the source of the ADC clocks. Refer to Table 3 for details. In Figure 12, ADS5292EVM uses an onboard, single-ended clock as the default option.

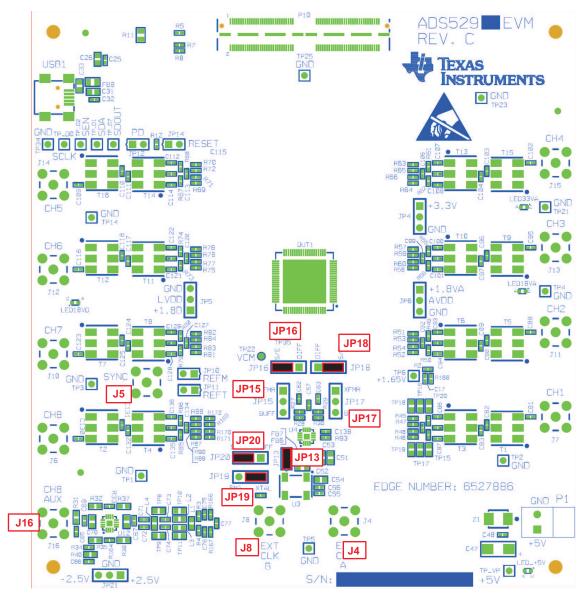


Figure 12. ADS5292EVM Default Clock Jumper Locations

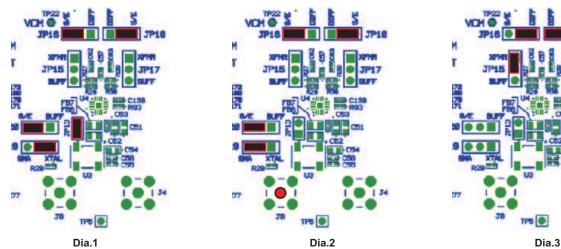
Clock Type		Reference Designator	Jumper Setting	Diagram
	Onboard CMOS Oscillator	JP13, JP19, JP20, JP16, JP18	JP13 (1-2), JP20 (2-3), JP19 (1-2), JP16 (2-3), JP18 (2-3)	Dia. 1 (Default Option)
Single Ended	External CMOS Clock Generator	J8, JP19, JP20, JP16, JP18	JP20 (2-3), JP19 (2-3), JP16 (2-3), JP18 (2-3) and Connect CMOS clock generator output at SMA connector J8.	Dia. 2

Table 3. ADC Clock Various Mode Jumper Settings



TP18

Clock Type		Reference Designator	Jumper Setting	Diagram
	Transformer Based External	JP15, JP17, JP16, JP18, J4	JP15 (1-2), JP16 (1-2), JP17 (1-2), JP18 (1-2), and Connect external Clock source at SMA connector J4	Dia. 3
Differential Clock Signal	Onboard Clock Buffer (CDCLVP1102,U4)	JP13, JP19, JP20, JP15, JP17, JP16, JP18	JP13 (1-2), JP20 (1-2), JP19 (1-2), JP15 (2-3), JP17 (2-3), JP16 (1-2), JP18 (1-2). This configures the onboard CMOS oscillator as clock input to buffer.	Dia. 4
		J8, JP19, JP20, JP15, JP17, JP16, JP18	JP19 (2-3), JP20 (1-2), JP15 (2-3), JP17 (2-3), JP16 (1-2), JP18 (1-2) and Connect External CMOS generator output at SMA connector J8.	Dia. 5
			This configures the external CMOS source as clock input to buffer.	



JP18

M r

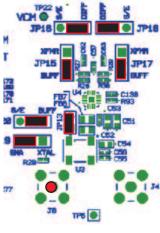
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TP6 💽

Dia.4



Dia.5



Board Configuration

9.3 Light-Emitting Diodes

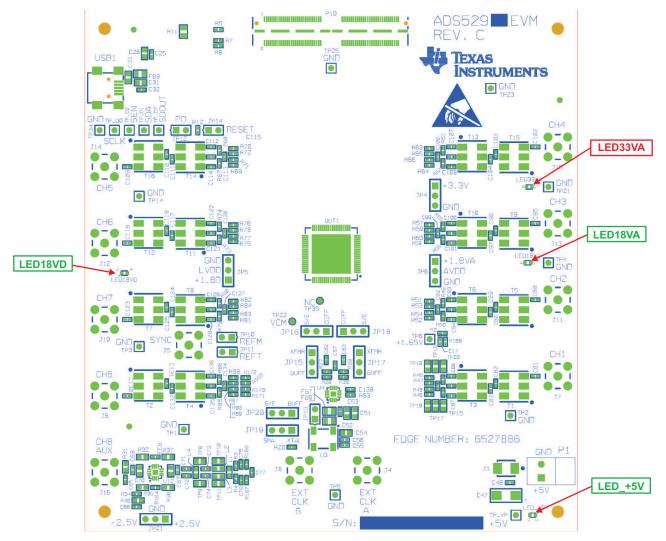


Figure 13. ADS5292EVM LED Location

Table 4. LED Indicators

Reference Designator	Power Supply	Color
LED_+5V	+5 V	Green
LED1.8VA	+1.8 VA	Green
LED1.8VD	+1.8 VD	Green
LED3.3VA	+3.3 VA	Orange



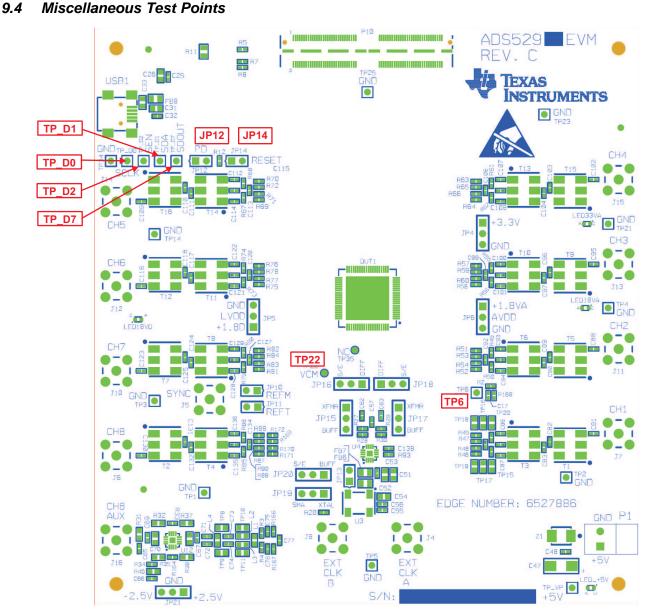


Figure 14. ADS5292EVM Test Point Locations

Reference Designator	Description
TP22	VCM: Common-mode output pin, 0.95-V output
TP6	CDC_VTH: Fixed voltage level (1.65 V)
TP_D0	SCLK: Serial clock input
TP_D1	SDA: Serial data input
TP_D2	SEN: Serial enable chip select
TP_D7	SDOUT: Serial data output
JP14	RESET: Install to reset the device (DUT1) manually
JP12	PD: Install to power down the device (DUT1) manually

10 EVM Schematics

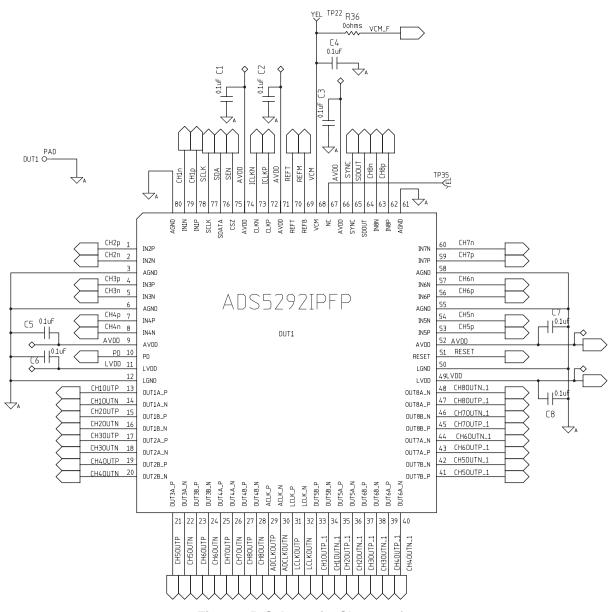
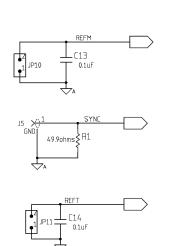
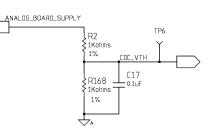
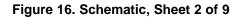


Figure 15. Schematic, Sheet 1 of 9









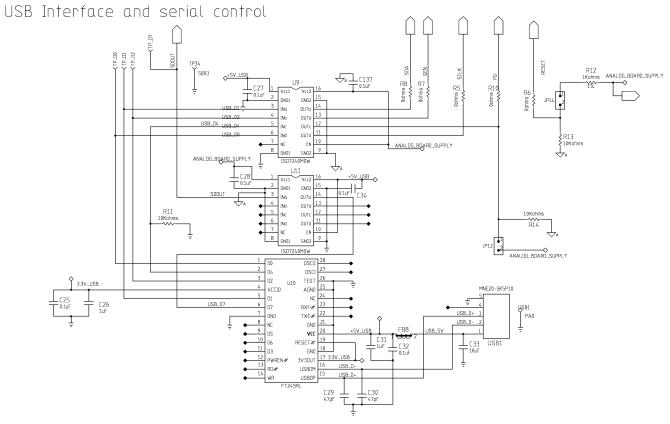


Figure 17. Schematic, Sheet 3 of 9

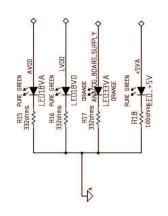
4 [P21 [P24] 42 5001 [5001 [5001] 5001

TP14

TP4

5001

TP2 TP3



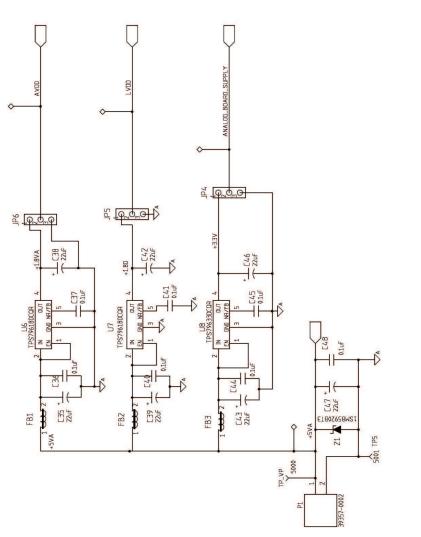
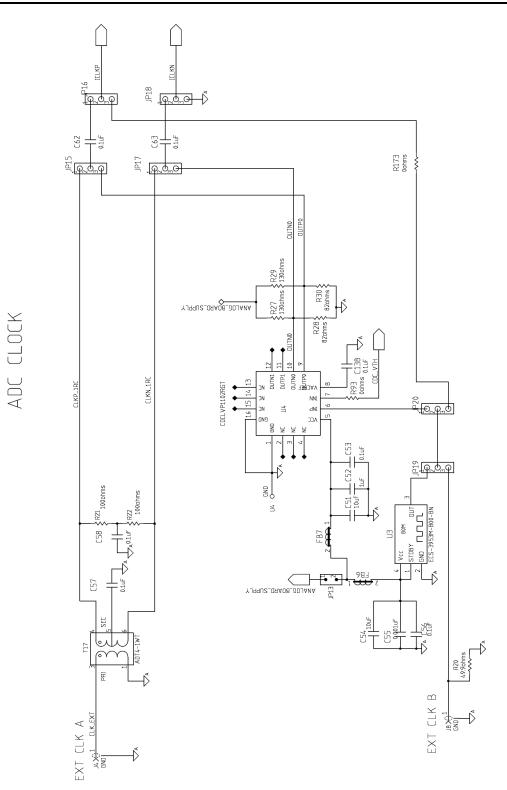


Figure 18. Schematic, Sheet 4 of 9

EVM Schematics







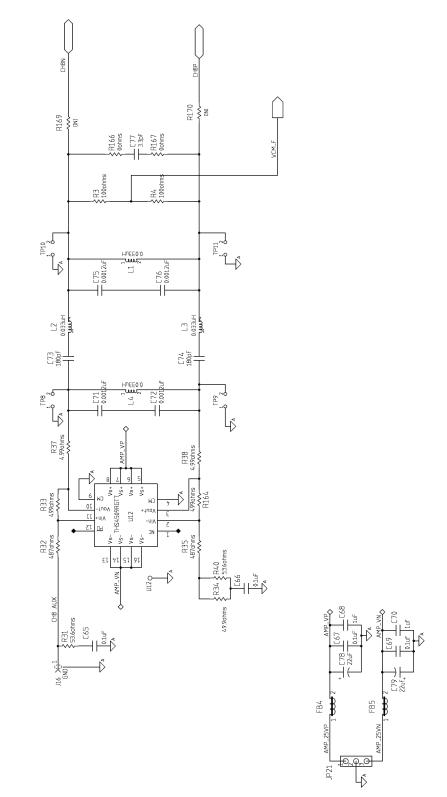


Figure 20. Schematic, Sheet 6 of 9



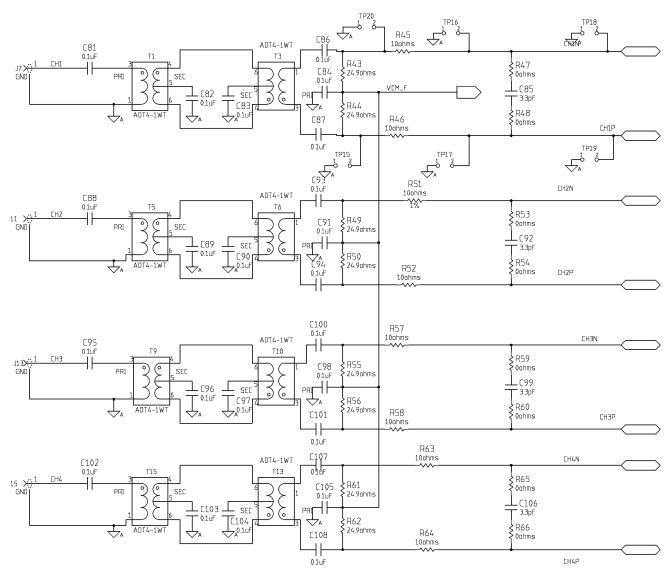


Figure 21. Schematic, Sheet 7 of 9



EVM Schematics

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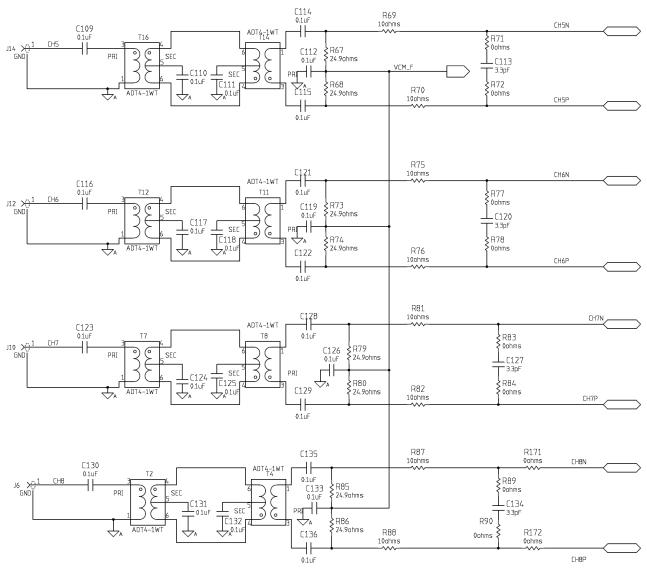
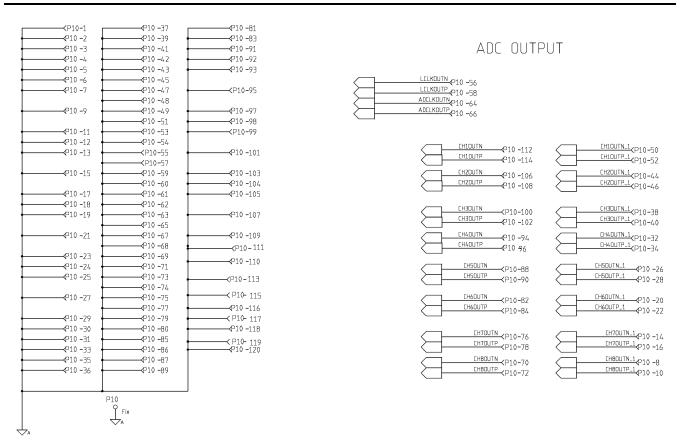
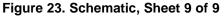


Figure 22. Schematic, Sheet 8 of 9







11 ADS5292EVM Bill of Materials

Table 6. Bill of Materials

QTY	MFR P/N	Description	Value	MFR	REF DES
1	ADS5292IPFP	12-Bit 8-Channel ADC	ADS5292	Texas Instruments	DUT1
17	ADT4-1WT+	RF TRANSFORMER WIDEBAND, 2-775 MHz, 50 Ω	ADT4-1WT+	Mini-Circuits	T1–T17
1	CDCLVP1102RGT	TWO LVPECL OUTPUT CLOCK BUFFER	CDCLVP1102	Texas Instruments	U4
2	CRCW06034R99FKEA	RES 4.99 Ω, 1/10 W, 1% 0603 SMD	4.99 Ω	Vishay/Dale	R37, R38
16	CRCW040210R0FKED	RES 10 Ω, 1/16,W, 1% 0402 SMD	10 Ω	Vishay/Dale	R45, R46, R51, R52, R57, R58, R63, R64, R69, R70, R75, R76, R81, R82, R87, R88
1	CRCW040249R9FKED	RES 49.9 Ω, 1/16,W, 1% 0402 SMD	49.9 Ω	Vishay/Dale	R34
2	CRCW060353R6FKEA	RES 53.6 Ω 1/10W 1% 0603 SMD	53.6 Ω	Vishay/Dale	R31, R40
1	CRCW06030000Z0EA	RES 0 Ω 1/10W 0603 SMD	0 Ω	Vishay/Dale	R36
2	CRCW0603487RFKEA	RES 487 Ω 1/10W 1% 0603 SMD	487 Ω	Vishay/Dale	R32, R35
4	CRCW0402100RFKED	RES 100 Ω 1/16W 1% 0402 SMD	100 Ω	Vishay/Dale	R3, R4, R21, R22
3	CRCW04021K00FKED	RES 1K Ω 1/16W 1% 0402 SMD	1 kΩ	Vishay/Dale	R2, R12, R168
2	CRCW0402499RFKED	RES 499 Ω 1/16W 1% 0402 SMD	499 Ω	Vishay/Dale	R33, R164
3	CRCW080510K0FKEA	RES 10K Ω 1/8W 1% 0805 SMD	10K Ω	Vishay/Dale	R11, R13, R14
7	C0402C104K8PACTU	CAP 0.10UF 10V CERAMIC X5R 0402	0.1 µF	Kemet	C36, C37, C40, C41, C44, C45, C48
1	ECJ-0EB1H102K	CAPACITOR, SMT, 0402, CER, 1000pF, 50V, 10%, X7R	1000 pF	Panasonic	C55
4	ECJ-0EB1H122K	CAPACITOR, SMT, 0402, CER, 1200pF, 50V, 10%, X7R	1200 pF	Panasonic	C71, C72, C75, C76
2	ECJ-0EB1E181K	CAP 180PF 25V CERAMIC X7R 0402	180 pF	Panasonic	C73, C74
2	ECJ-0EC1H390J	CAP 39PF 50V CERAMIC 0402 SMD	39 PF	Panasonic	C29, C30
5	ECJ-1V41E105M	CAP 1UF 25V CERAMIC 0603 X5S	1 µF	Panasonic - ECG	C26, C31, C52, C68, C70
1	ECS-3953M-800-BN	OSC, SMT, 3.3V, 50ppm, -40~85°C, 5nS, 80.000 MHz	OSC 80 MHz	ECS Inc	U3
4	ELJ-RE33NGFA	INDUCTOR 33NH 2% 0603 SMD	33NH	Panasonic	L1–L4
2	ERJ-2GEJ131	RESISTOR, SMT, 0402, THICK FILM, 5%, 1/16W, 130	130 Ω	Panasonic	R27, R29
2	ERJ-2GEJ820	RESISTOR, SMT, 0402, THICK FILM, 5%, 1/16W, 82	82 Ω	Panasonic	R28, R30
27	ERJ-2GE0R00X	RESISTOR/JUMPER, SMT, 0402, 0 Ω, 5%, 1/16W	0 Ω	Panasonic	R5–R8, R10, R47, R48, R53, R54, R59, R60, R65, R66, R71, R72, R77, R78, R83, R84, R89, R90, R93, R166, R167, R171–R173
16	ERJ-2RKF24R9X	RESISTOR, SMT, 0402, 24.9 Ω, 1%, 1/16W	24.9 Ω	Panasonic	R43, R44, R49, R50, R55, R56, R61, R62, R67, R68, R73, R74, R79, R80, R85, R86
2	ERJ-2RKF49R9X	RESISTOR, SMT, 0402, 49.9 Ω, 1%, 1/16W	49.9 Ω	Panasonic	R1, R20
3	ERJ-2RKF1000X	RESISTOR, SMT, 0402, 100 Ω, 1%, 1/10W	100 Ω	Panasonic	R15, R16, R18
1	ERJ-2RKF3320X	RESISTOR, SMT, 0402, 332 Ω, 1%, 1/16W	332 Ω	Panasonic	R17
1	FT245RL	USB FIFO IC INCORPORATE FTDICHIP-ID SECURITY DONGLE	USB	FTDI	U10
9	GRM1555C1H3R3CZ01D	CAP CER 3.3PF 50V C0G 0402	3.3 pF	Murata	C77, C85, C92, C99, C106, C113, C120, C127, C134
8	HI0805R800R-10	FERRITE CHIP POWER 80 Ω SMD	FERRITE	Laird-Signal Integrity Products	FB1–FB8
2	ISO7240MDW	QUAD DIGITAL ISOLATORS	IC DGTL ISOL	Texas Instruments	U9, U11
3	JMK107BJ106MA-T	CAPACITOR, SMT, 0603, CERAMIC, 10µF, 6.3V, 20%, X5R	10 µF	Taiyo Yuden	C33, C51, C54
10	JUMPER-0603(UN)	UNINSTALLED JUMPER, SMT0603	DNI		TP8–TP11, TP15–TP20

TEXAS INSTRUMENTS

		Table 6. Bill of Materials	(continued)			
QTY	MFR P/N	Description	Value	MFR	REF DES	
3	LNJ308G8PRA	LED, SMT, 0603, PURE GREEN, 2.03V	LED	Panasonic	LED18VA, LED18VD, LED_+5V	
1	LNJ808R8ERA	LED, SMT, 0603, ORANGE, 1.8V	LED	Panasonic	LED33VA	
1	897-43-005-00-100001	CONN RECEPT MINI-USB TYPE B SMT	USB Mini B	Mill-Max	USB1	
1	QTH-060-01-L-D-A	HEADER, SMT, 120P, 0.5mm, FEM, 2BANK, RECEPTACLE, 168/198H	CONN	Samtec Inc	P10	
2	TEST POINT YELLOW	NOT INSTALLED	DNI		TP22, TP35	
1	THS4509QRGTRQ1	WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFF AMP, 1900 MHz	IC OPAMP	Texas Instruments	U12	
9	TPSC226K016R0375	10%, 16V, 22µF	22 µF	AVX	C35, C38, C39, C4, C43, C46, C47, C78, C79	
2	TPS79618DCQR	ULTRALOW-NOISE HI PSRR FAST RF 1-A LDO LINEAR REGULATOR, 1.8V	LDO REG	Texas Instruments	U6, U7	
1	TPS79633DCQR	ULTRALOW-NOISE HI PSRR FAST RF 1-A LDO LINEAR	LDO REG	Texas Instruments	U8	
1	1SMB5921BT3G	DIODE ZENER 6.8V 3W SMB	DIODE Zener	ON Semiconductor	Z1	
5	9-146285-0-02	CONN HEADR BRKWAY 0.100 02POS STR	CONN Header	TE Connectivity	JP10–JP14	
10	9-146285-0-03	CONN HEADR BRKWAY 0.100 03POS STR	CONN Header	TE Connectivity	JP4–JP6, JP15–JP21	
12	901-144-8	SMA COAX STRAIGHT PCB CURRENT P/N IS 901-144-8RFX	SMA	Amphenol	J4–J8, J10–J16	
76	0402YD104KAT2A	CAP CERM 0.1µF 10% 16V X5R 0402	0.1 µF	AVX	C1-C8, C13 C14, C17, C25, C27, C28, C32, C34, C53, C56-C58, C6, C63, C65-C67, C93-C98, C100-C105, C107-C112, C114-C119, 121-C126, C128-C133, C135-C138	
1	5000	TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, RED	Test Point,Red	Keystone Electronics	TP_VP	
9	5001	TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, BLACK	Test Point,Black	Keystone Electronics	TP1–TP5, TP14, TP21, TP23, TP25	
5	5002	TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, WHITE	Test Point,White	Keystone Electronics	TP6, TP_D0-TP_D2, TP_D7	
1	5003	TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, ORANGE	Test Point,Orange	Keystone Electronics	TP34	
1	39357-0002	HEADER, THRU, POWER, 2P, 3.5MM, EUROSTYLE	CONN TERMINAL	Molex Connector Corp	P1	
2	RESISTOR (DNI)	NOT INSTALLED	DNI		R169, R170	
4	24436	STANDOFF HEX M3 THR ALUM 18MM	STANDOFF	Keystone	STANDOFF HEX M3 THR ALUM 18MM	
4	29311	SCREW STEEL M3 THR 6MM	SCREW	Keystone	SCREW STEEL M3 THR 6MM	

Table 6. Bill of Materials (continued)



ADS5292EVM Printed-Circuit Board Layout



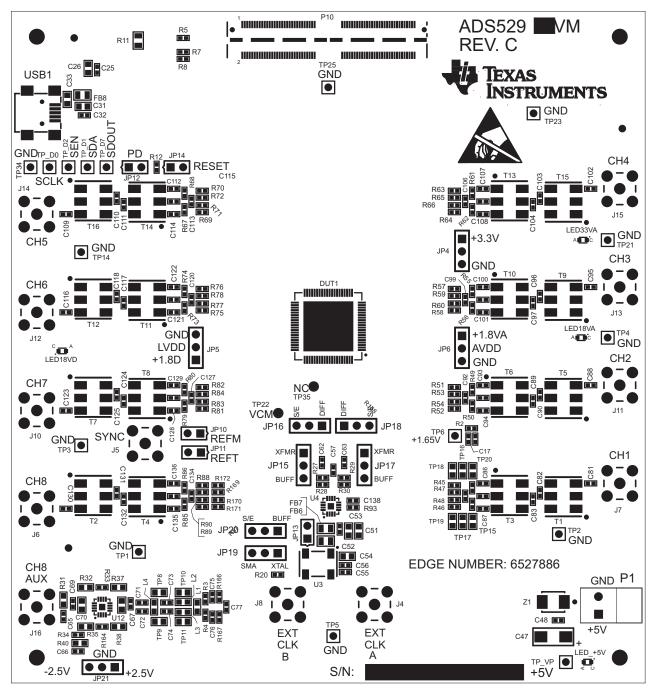


Figure 24. ADS5292EVM Top Layer Assembly Drawing – Top View





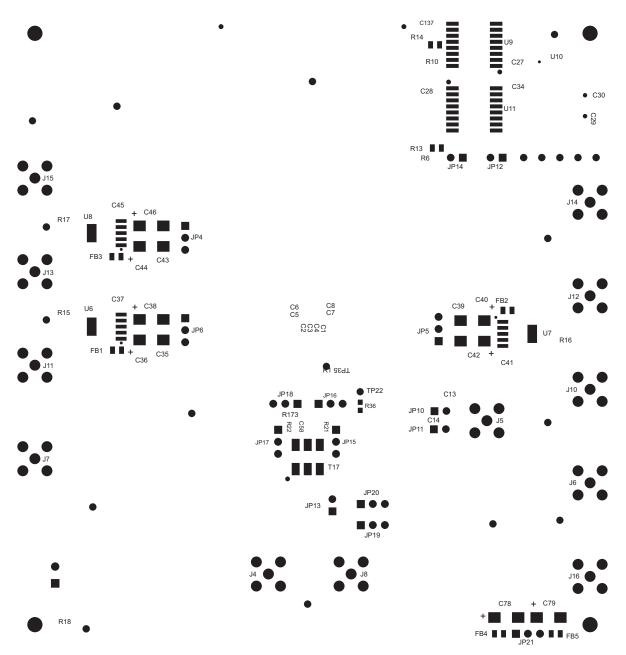


Figure 25. ADS5292EVM Bottom Layer Assembly Drawing – Bottom View



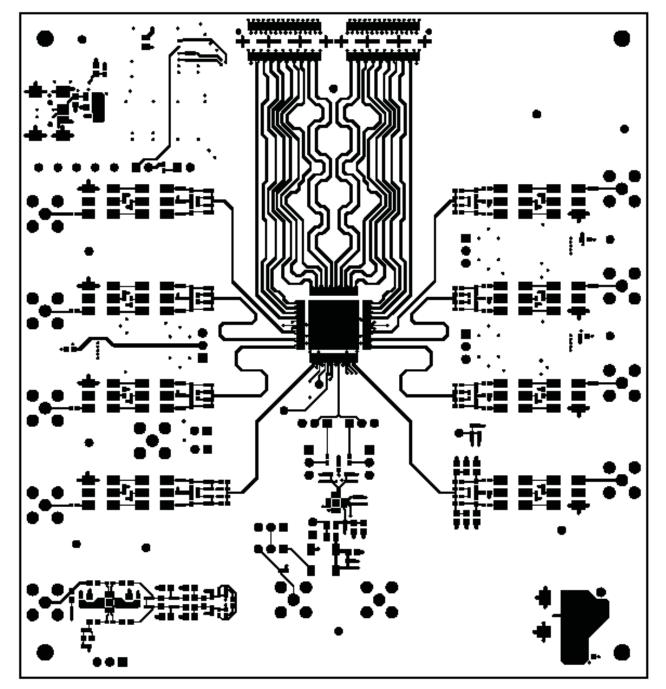


Figure 26. ADS5292EVM Top Layer Copper – Top View



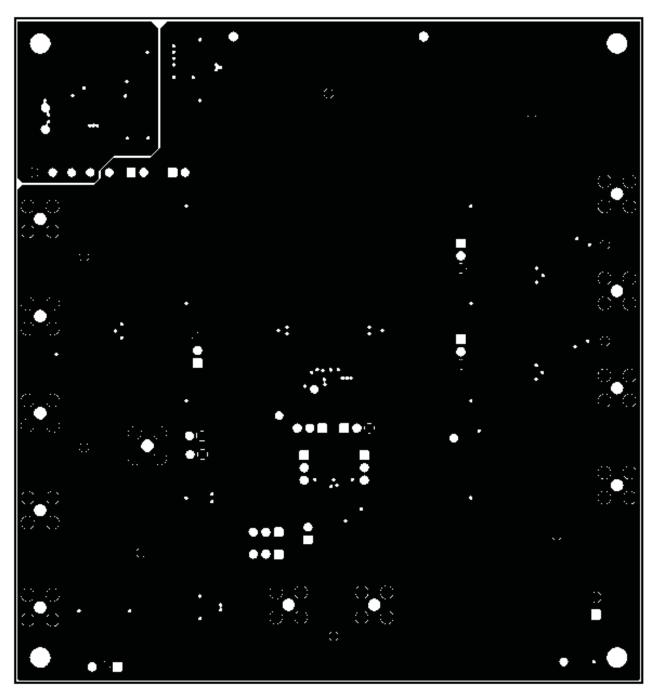


Figure 27. ADS5292EVM Internal Layer 1, Ground – Top View



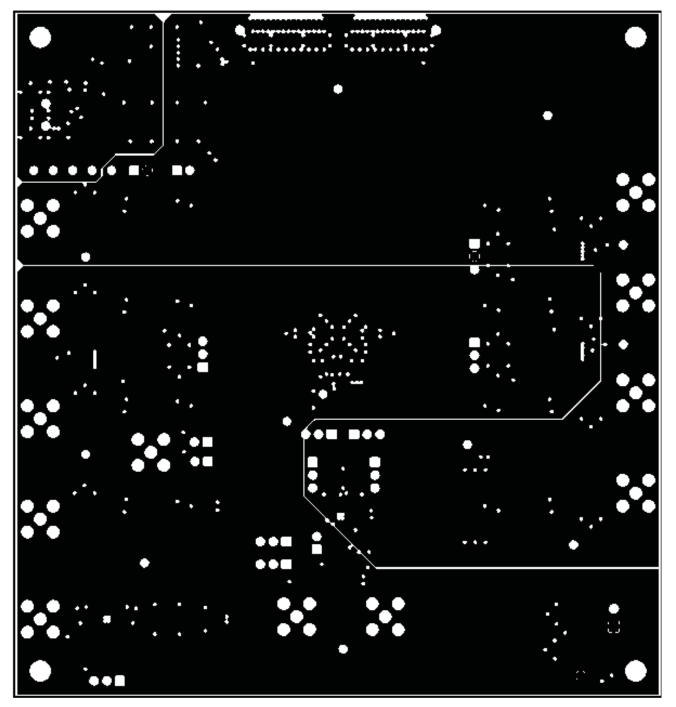


Figure 28. ADS5292EVM Internal Layer 2, Power - Top View



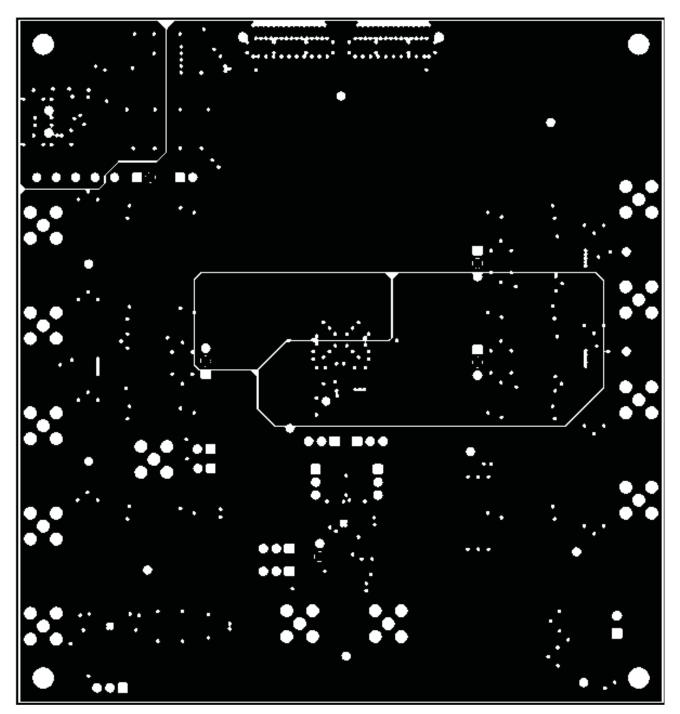


Figure 29. ADS5292EVM Internal Layer 3, Power - Top View



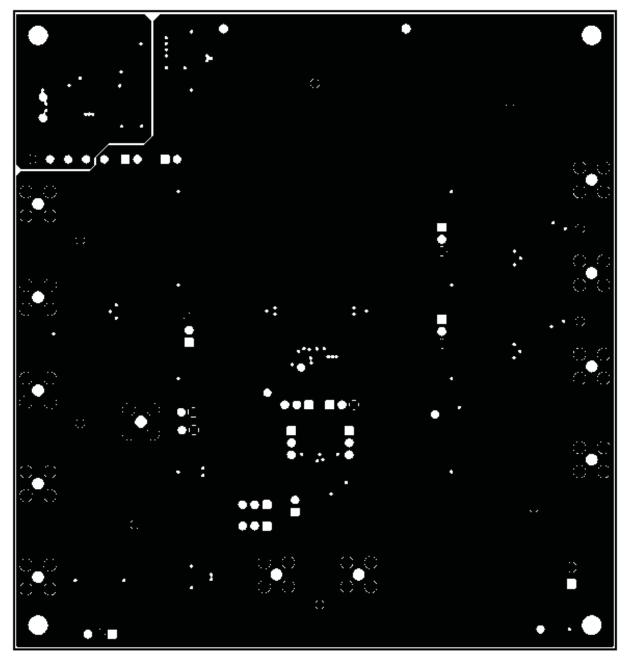


Figure 30. ADS5292EVM Internal Layer 4, Ground – Top View



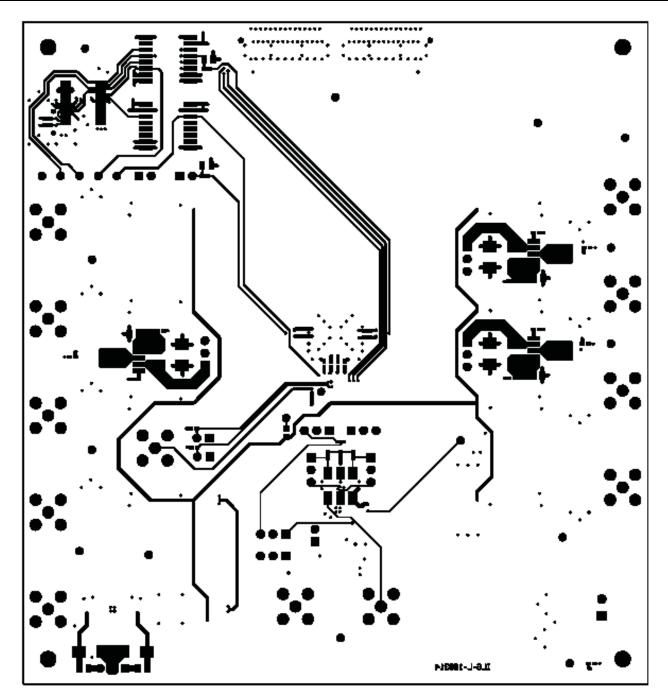


Figure 31. ADS5292EVM Bottom Layer Copper – Top View

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -0.3 V to 5.3 V and the output voltage range of -0.3 V to 3.3 V. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

[Important Notice for Users of this Product in Japan]

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

- Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited (address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

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For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

- 1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
- 2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
- 3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
- 4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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