



PHPT61006PY

100 V, 6 A PNP high power bipolar transistor

21 January 2015

Product data sheet

1. General description

PNP high power bipolar transistor in a SOT669 (LFPAK56) Surface-Mounted Device (SMD) power plastic package.

NPN complement: PHPT61006NY

2. Features and benefits

- High thermal power dissipation capability
- High temperature applications up to 175 °C
- Reduced Printed Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- AEC-Q101 qualified.

3. Applications

- Power management
- Load switch
- Linear mode voltage regulator
- Backlighting applications
- Motor drive
- Relay replacement

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-100	V
I_C	collector current		-	-	-6	A
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse	-	-	-12	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -6$ A; $I_B = -600$ mA; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C; pulsed	-	85	270	m Ω

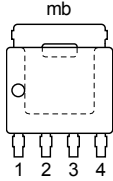
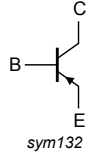


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E	emitter	 <p>LFPAK56; Power-SO8 (SOT669)</p>	
2	E	emitter		
3	E	emitter		
4	B	base		
mb	C	collector		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT61006PY	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PHPT61006PY	1006PAB

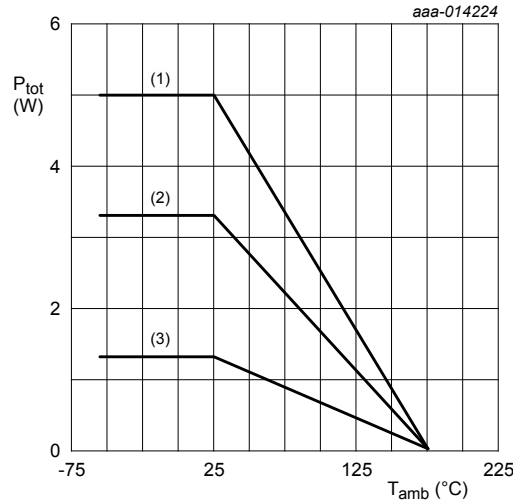
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-100	V
V_{CEO}	collector-emitter voltage	open base		-	-100	V
V_{EBO}	emitter-base voltage	open collector		-	-8	V
I_C	collector current			-	-6	A
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse		-	-12	A
I_B	base current			-	-1	A
I_{BM}	peak base current	$t_p \leq 1$ ms; pulsed		-	-2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	1.3	W
			[2]	-	3.3	W
			[3]	-	5	W
			[4]	-	25	W
T_j	junction temperature			-	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
 [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated mounting pad for collector 6 cm².
 [3] Device mounted on an ceramic Printed-Circuit Board (PCB), Al₂O₃, standard footprint.
 [4] Power dissipation from junction to mounting base.



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 6 cm²
- (3) FR4 PCB, standard footprint

Fig. 1. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	115	K/W
			[2]	-	-	45	K/W
			[3]	-	-	30	K/W
R _{th(j-mb)}	thermal resistance from junction to mounting base			-	-	6	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for collector 6 cm².
- [3] Device mounted on an ceramic Printed-Circuit Board (PCB), Al₂O₃, standard footprint.

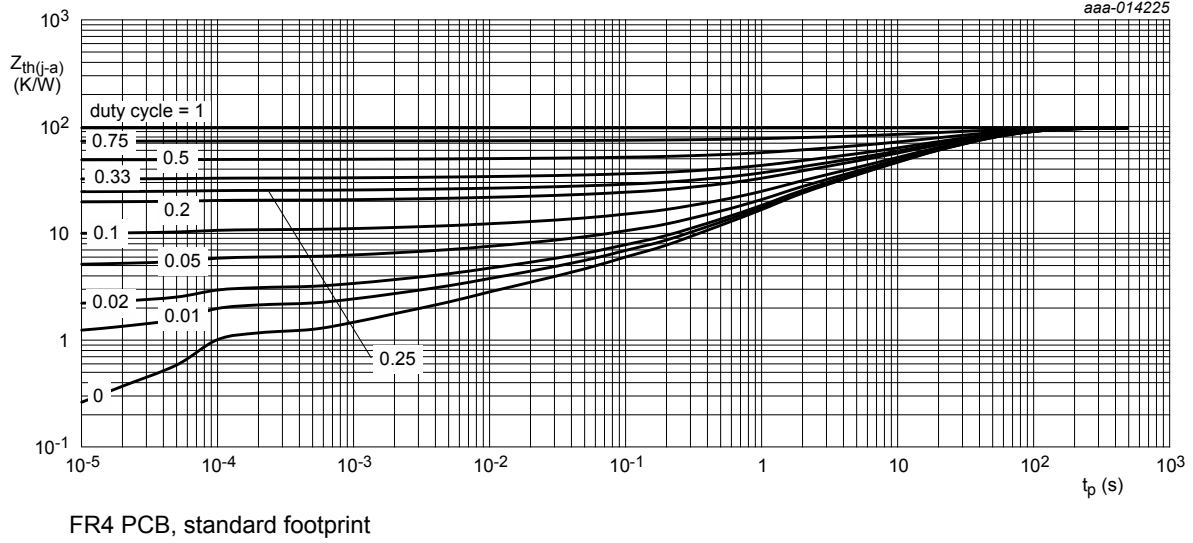


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

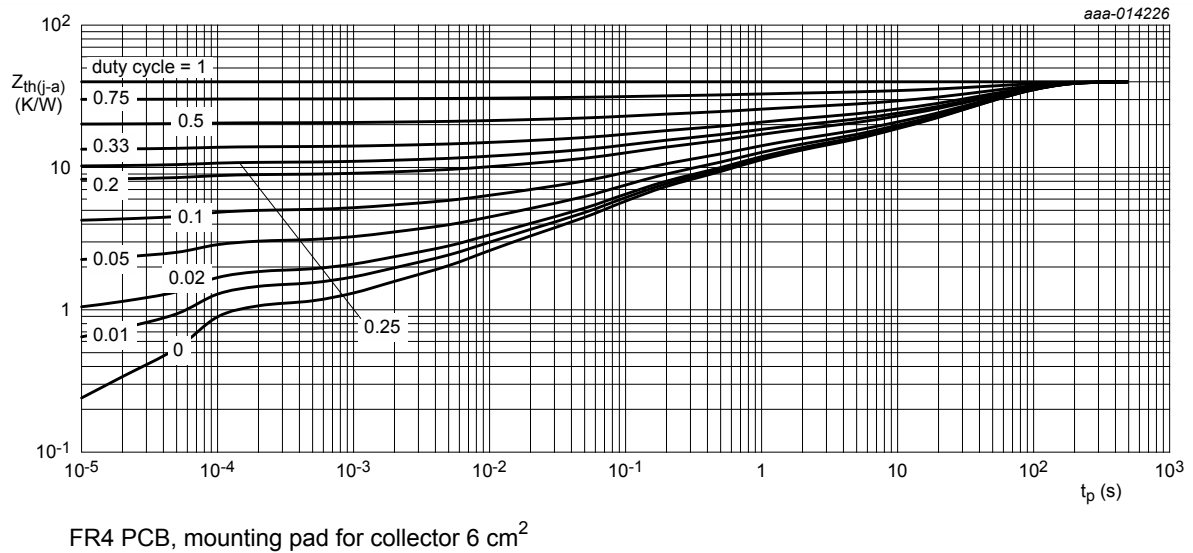


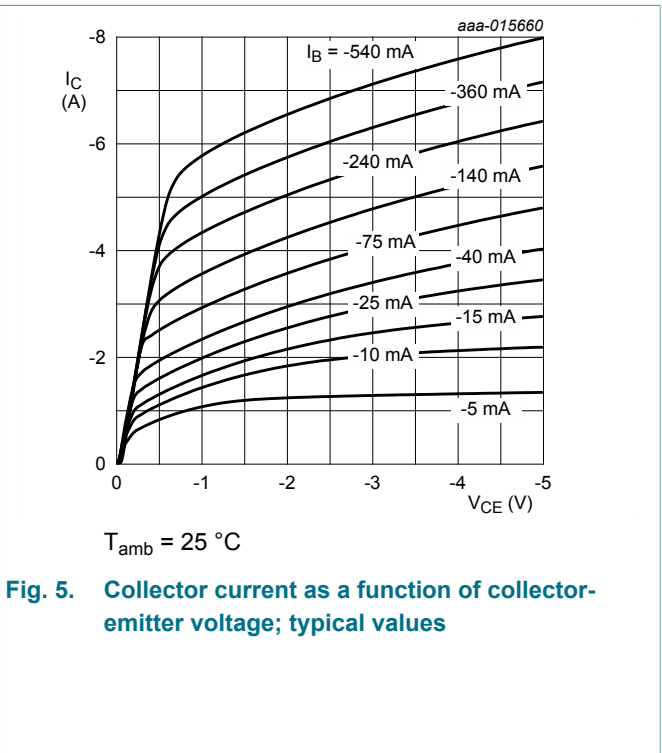
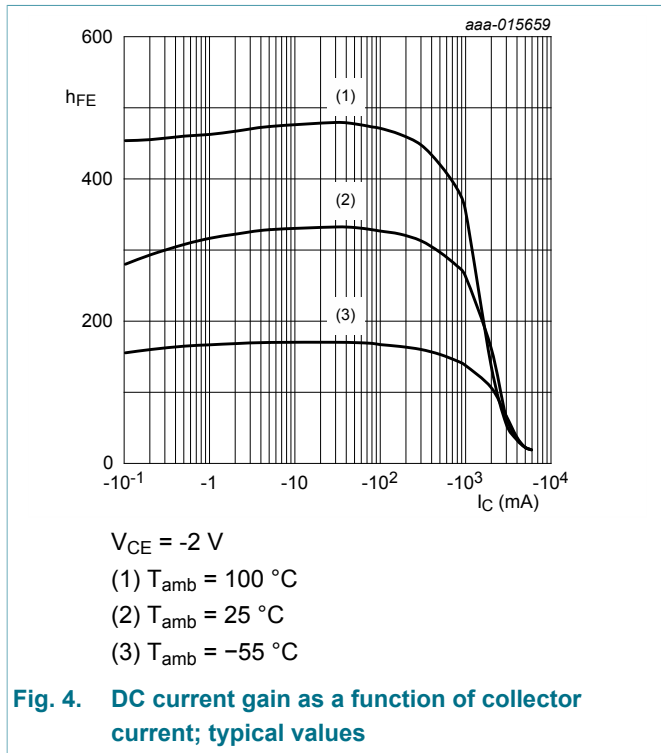
Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = -80 V; I _E = 0 A; T _{amb} = 25 °C	-	-	-100	nA
		V _{CB} = -80 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -80 V; V _{BE} = 0 V; T _{amb} = 25 °C	-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -8 V; I _C = 0 A; T _{amb} = 25 °C	-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -500 mA; T _{amb} = 25 °C	170	305	-	
		V _{CE} = -2 V; I _C = -1 A; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	160	275	-	
		V _{CE} = -2 V; I _C = -3 A; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	45	90	-	
		V _{CE} = -2 V; I _C = -6 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	10	20	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -1 A; I _B = -50 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-75	-130	mV
		I _C = -3 A; I _B = -300 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-150	-240	mV
		I _C = -6 A; I _B = -600 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-900	-1600	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -6 A; I _B = -600 mA; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C; pulsed	-	85	270	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -1 A; I _B = -50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.8	-0.95	V
		I _C = -3 A; I _B = -300 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-0.95	-1.1	V
		I _C = -6 A; I _B = -600 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-1.1	-1.25	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -2 V; I _C = -500 mA; T _{amb} = 25 °C	-	-0.7	-0.8	V
t _d	delay time	V _{CC} = -12.5 V; I _C = -3 A; I _{Bon} = -150 mA; I _{Boff} = 150 mA; T _{amb} = 25 °C	-	15	-	ns
t _r	rise time		-	220	-	ns
t _{on}	turn-on time		-	235	-	ns
t _s	storage time		-	160	-	ns
t _f	fall time		-	185	-	ns
t _{off}	turn-off time		-	345	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_T	transition frequency	$V_{CE} = -10\text{ V}; I_C = -500\text{ mA};$ $f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	116	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	52	-	pF



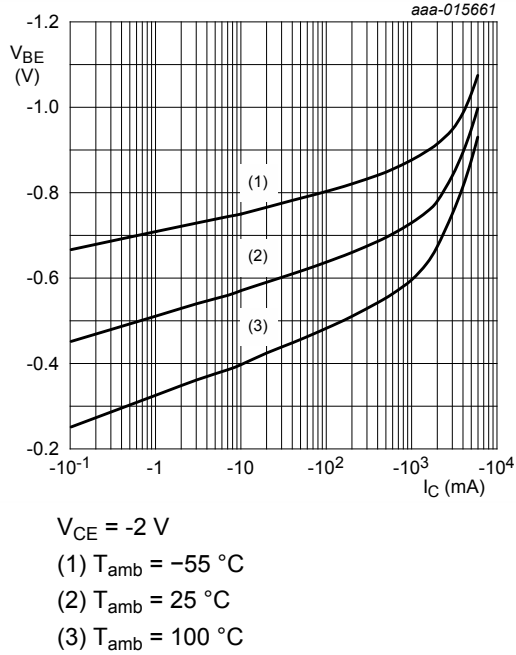


Fig. 6. Base-emitter voltage as a function of collector current; typical values

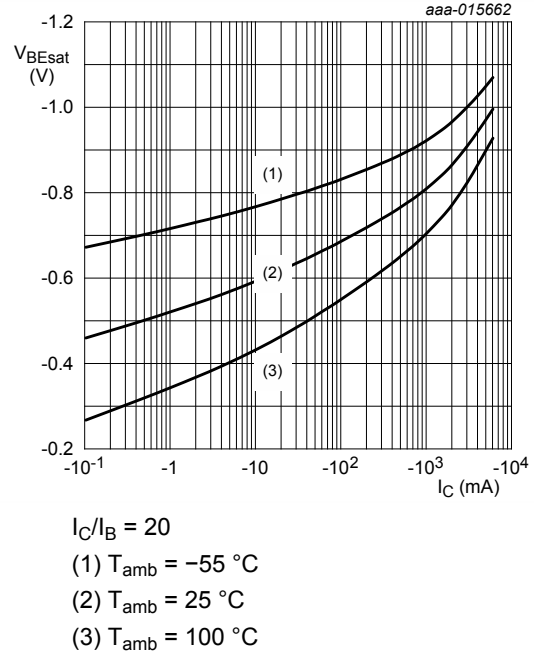


Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values

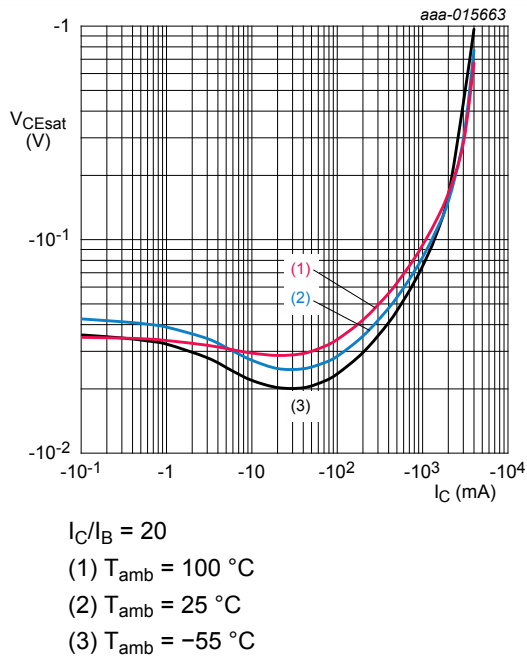


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

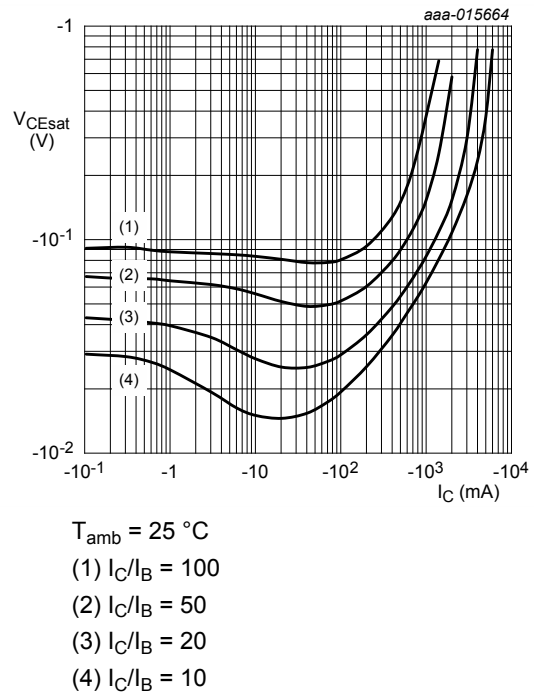
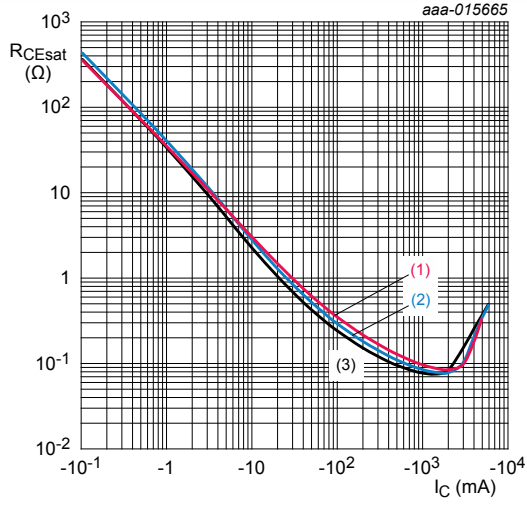
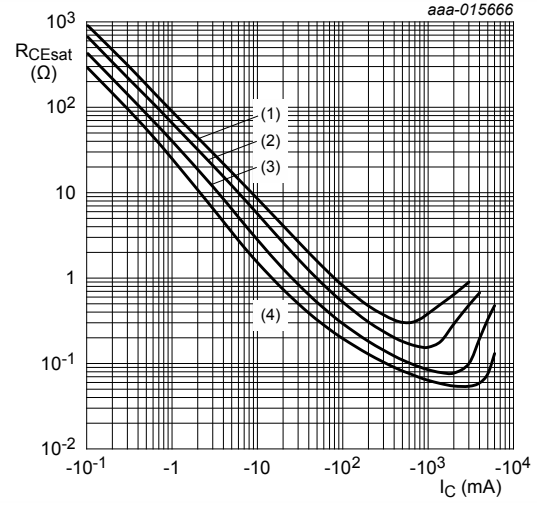


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -55\text{ °C}$

Fig. 10. Collector-emitter saturation resistance as a function of collector current; typical values



- $T_{amb} = 25\text{ °C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 20$
 - (4) $I_C/I_B = 10$

Fig. 11. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

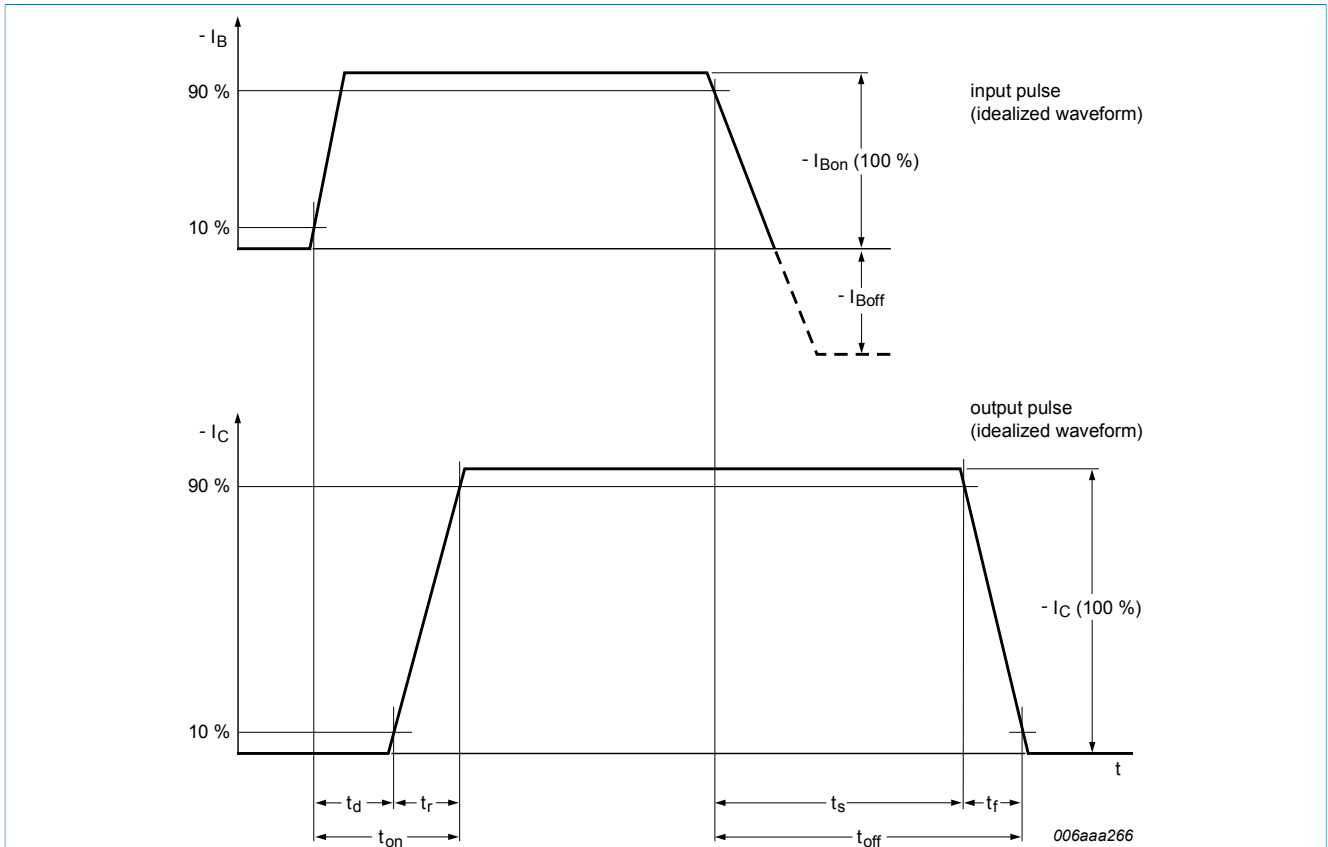


Fig. 12. BISS transistor switching time definition

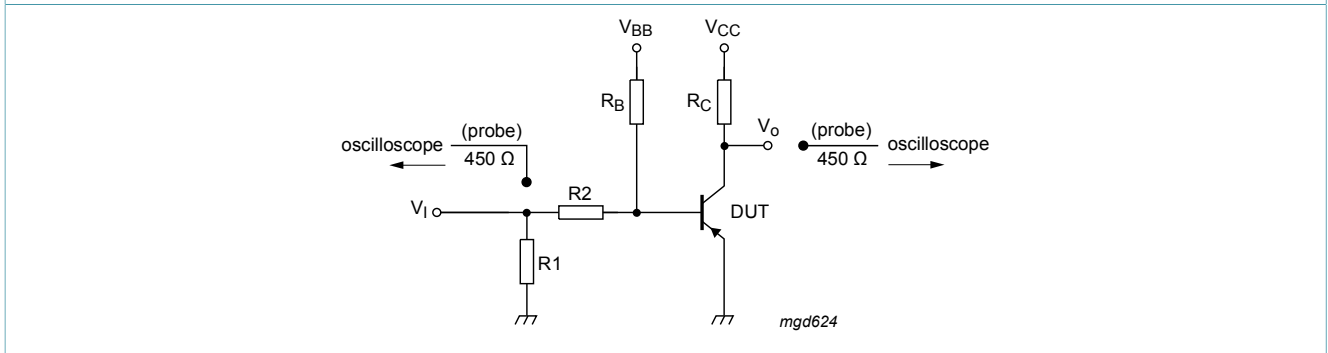


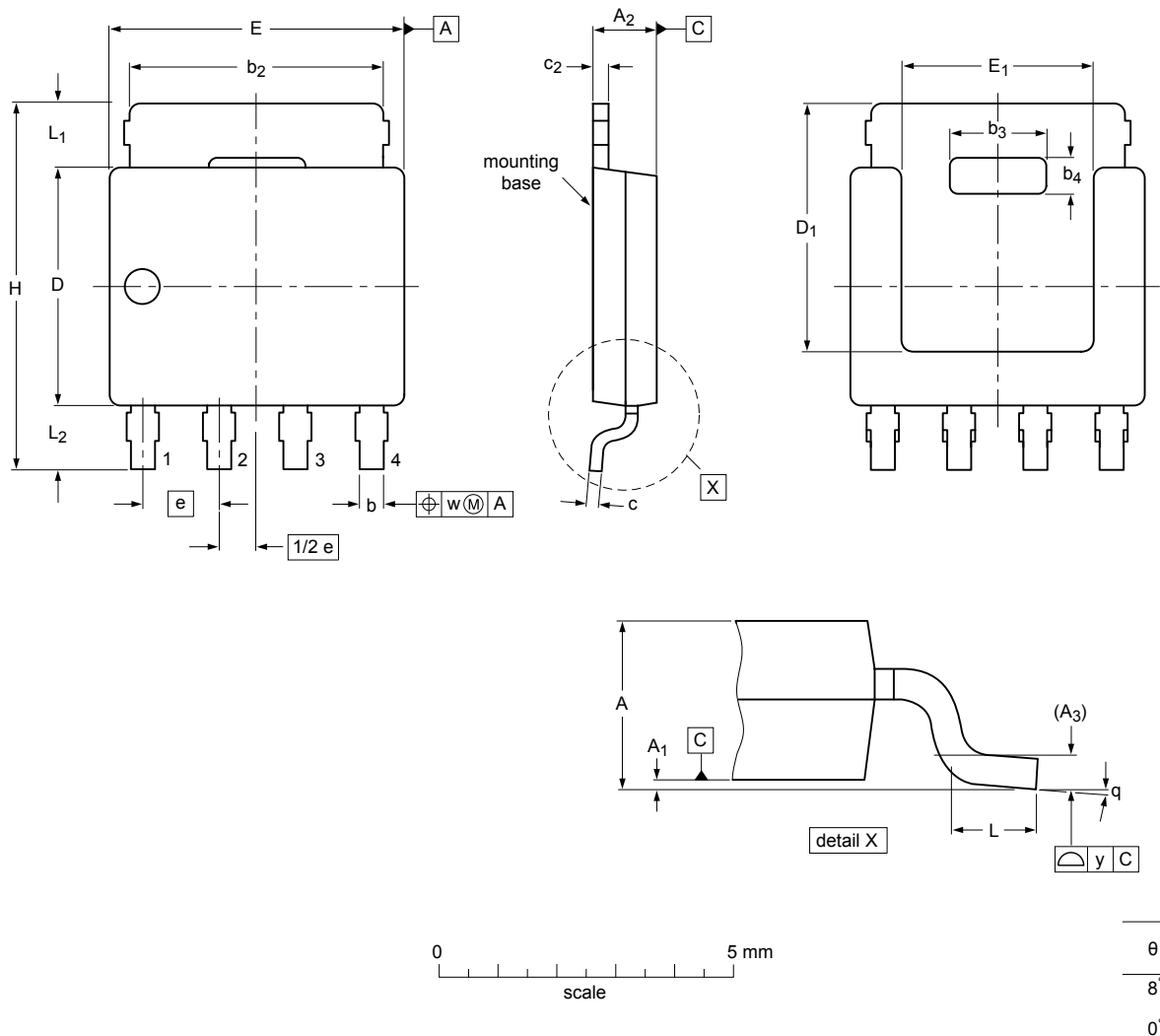
Fig. 13. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 14. Package outline LFAK56; Power-SO8 (SOT669)

13. Soldering

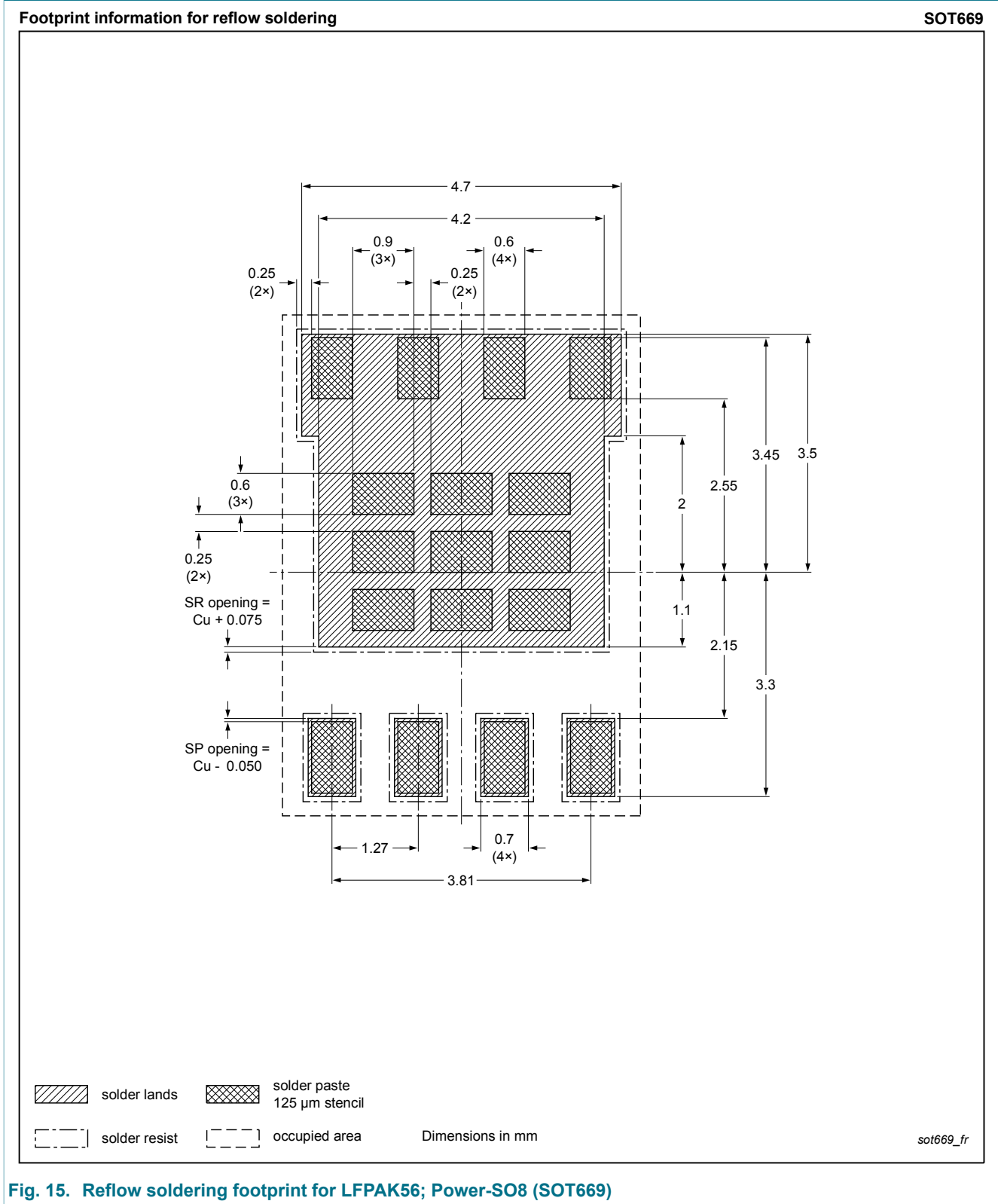


Fig. 15. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT61006PY v.1	20150121	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	3
9	Thermal characteristics	4
10	Characteristics	6
11	Test information	10
11.1	Quality information	10
12	Package outline	11
13	Soldering	12
14	Revision history	13
15	Legal information	14
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	15

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