HDMI COMPANION CHIP WITH STEP-UP DC-DC, I^{2}C LEVEL SHIFTER, AND HIGH-SPEED ESD CLAMPS

Check for Samples: TPD12S015A

FEATURES

- **Conforms to HDMI Compliance Tests Without Any External Components**
- **Supports HDMI 1.4 Data Rate**
- **Match Class D and Class C Pin Mapping**
- **Excellent Matching Capacitance (0.05pF) in Each Differential Signal Pair**
- **Internal Boost Converter to Generate 5V From a 2.3-5.5V Battery Voltage**
- **Auto-direction Sensing Level Shifting in the CEC, SDA, and SCL Paths**
- **IEC 61000-4-2 (Level 4) System Level ESD Compliance**
- **Improved Drop-in Replacement for the Industry Popular TPD12S015**
- **Industrial Temperature Range: -40°C to 85°C**

APPLICATIONS

- **Smart Phones**
- **eBook**
- **Tablet PC**
- **Digital Camcorders**
- **Portable Game Console**
- **Digital Still Cameras**

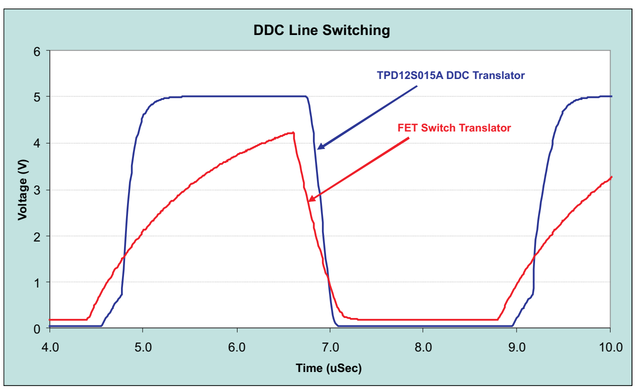
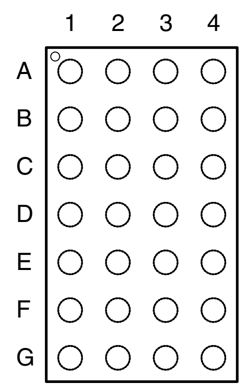


Figure 1. SCL_B or SDA_B Buffers of TPD12S015A Driving Long HDMI Cable (750pF Load)

YFF PACKAGE (TOP VIEW)



For package dimensions, see the Mechanical Drawing at the end of this document.

YFF PACKAGE PIN MAPPING

	1	2	3	4
A	LS_OE	V_{CCA}	D2+	D2–
B	SCL_A	CEC_A	GND	D1+
C	SDA_A	HPD_A	GND	D1–
D	CT_CP_HPD	GND	CEC_B	D0+
E	FB	GND	SCL_B	D0–
F	5VOUT	SW	SDA_B	CLK+
G	P_{GND}	V_{BAT}	HPD_B	CLK–

DESCRIPTION/ORDERING INFORMATION

The TPD12S015A is an integrated HDMI companion chip solution. This device offers 8 low capacitance ESD clamps allowing HDMI 1.4 data rates. The 0.4-mm pitch WCSP package pin mapping matches the HDMI Type D or Type C connectors. The integrated ESD clamps in monolithic silicon technology provide good matching between each differential signal pair. This provides an advantage over discrete ESD clamp solutions where variations between ESD clamps degrade the differential signal quality.

The TPD12S015A provides a regulated 5V output (5VOUT) for sourcing the HDMI power line. The 5VOUT pin supplies minimum 55mA to the HDMI receiver while meeting the HDMI 5VOUT specifications. The 5VOUT and the hot plug detect (HPD) circuitry are independent of the LS_OE control signal; they are controlled by the CT_CP_HPD pin. This independent control enables the detection scheme (5VOUT + HPD) to be active before enabling the HDMI link. The HPD_B port has a glitch filter to avoid false detection due to the bouncing while inserting the HDMI plug.

There are three non-inverting bi-directional translation circuits for the SDA, SCL, and CEC lines; they are controlled by the LS_OE control signal. Each have a common power rail (VCCA) on the A side from 1.1V to 3.6V. On the B side, the SCL_B and SDA_B each have an internal 1.75kΩ pull-up connected to the regulated 5V rail (5VOUT). The SCL and SDA pins meet the I2C specifications, and drive at least 750pF loads which exceeds the HDMI cable specification. An LDO generates a 3.3V internal rail for the CEC line operation when LS_OE = H & CT_CP_HPD = H. The CEC_B pin has a 26kΩ pull-up to this internal 3.3V rail.

The TPD12S015A provides IEC61000-4-2 (Level 4) ESD protection. This device is offered in a space saving 1.6mm × 2.8mm WCSP package.

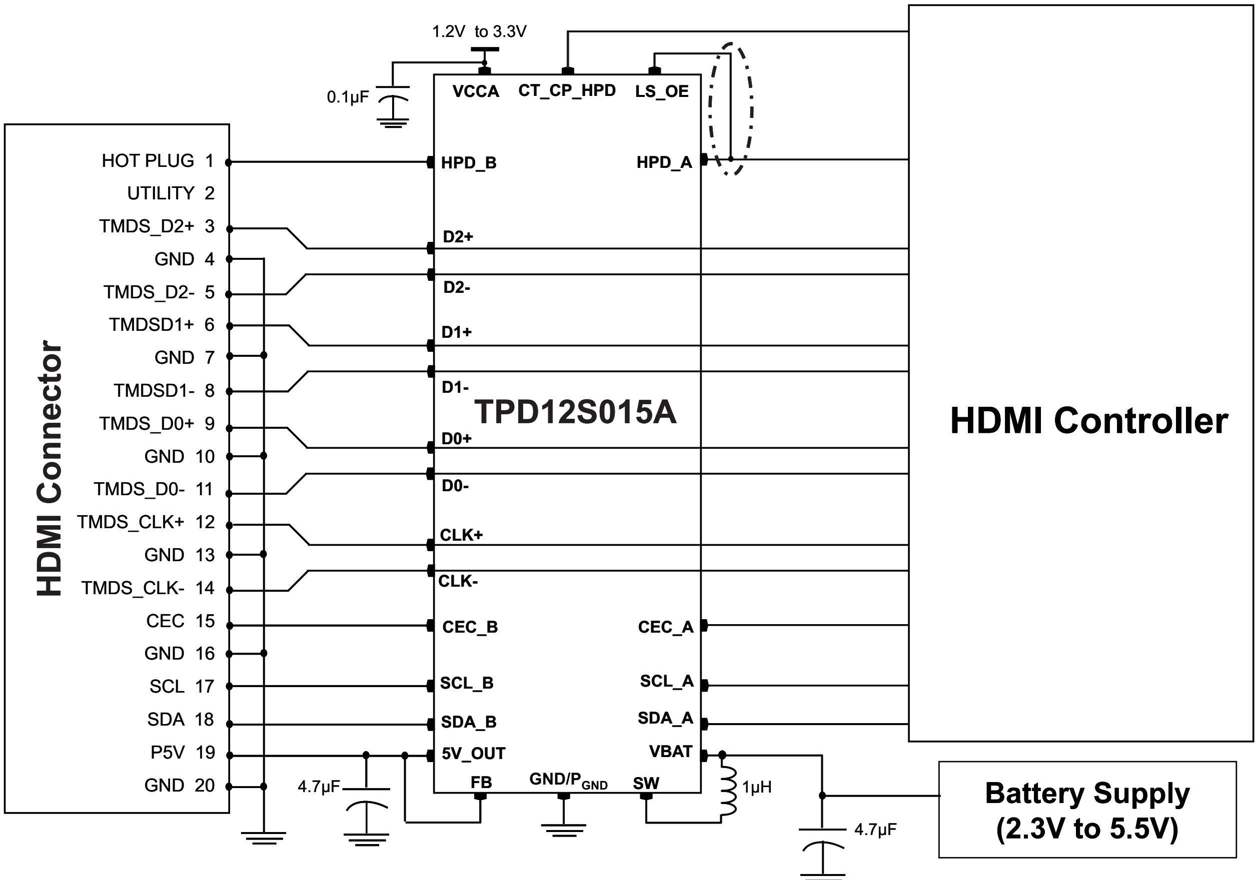
ORDERING INFORMATION

T_A	PACKAGE[(1) (2)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YFF	Tape and reel	TPD12S015AYFFR	PN015A

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

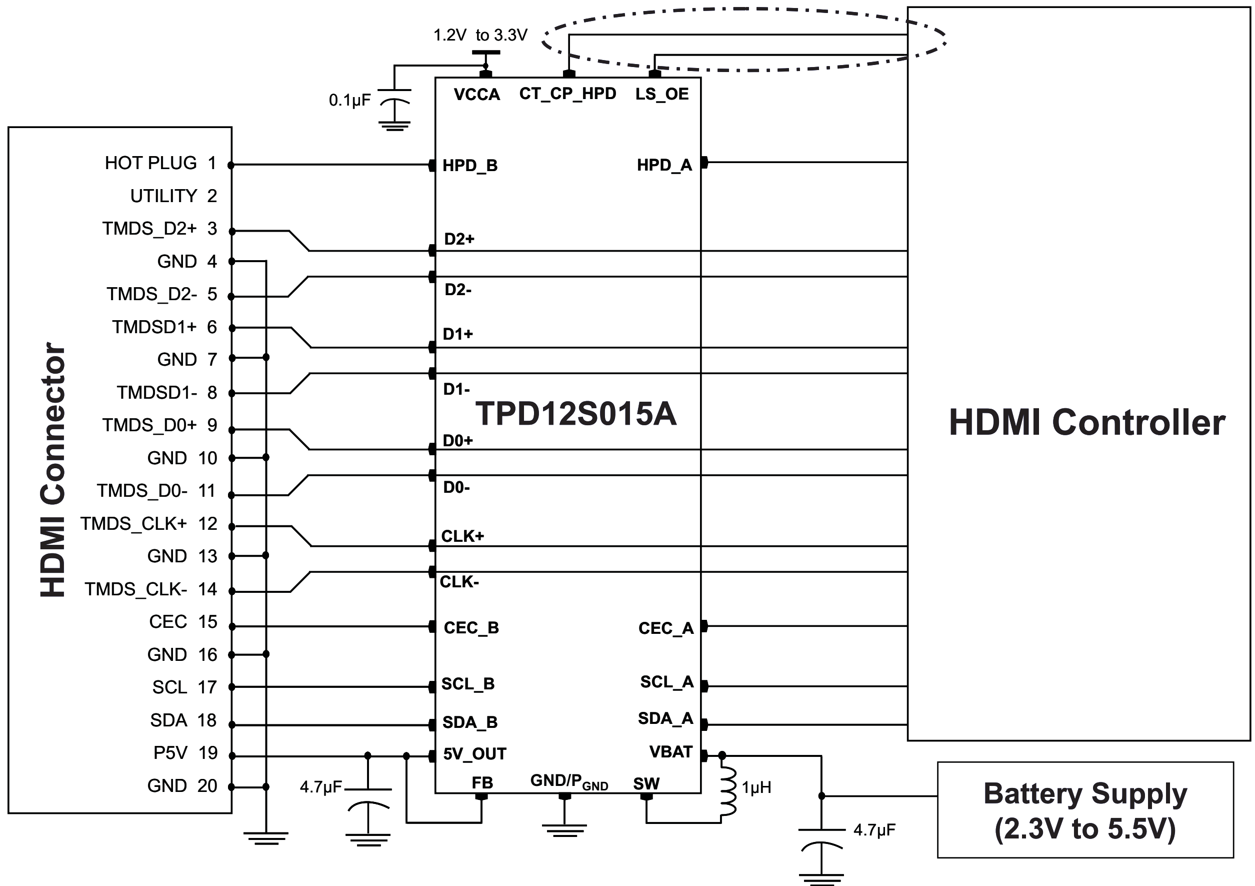
SYSTEM LEVEL BLOCK DIAGRAM

Application Schematics for HDMI controllers with one GPIO for HDMI Interface Control



Some HDMI controllers may have only one GPIO to control the HDMI interface. Refer to Figure 1, HDMI Driver Chip is controlling the TPD12S015A via only one control line (CT_CP_HPD). In this mode the HPD_A to LE_OE pin are connected shown in the above oval dotted line.

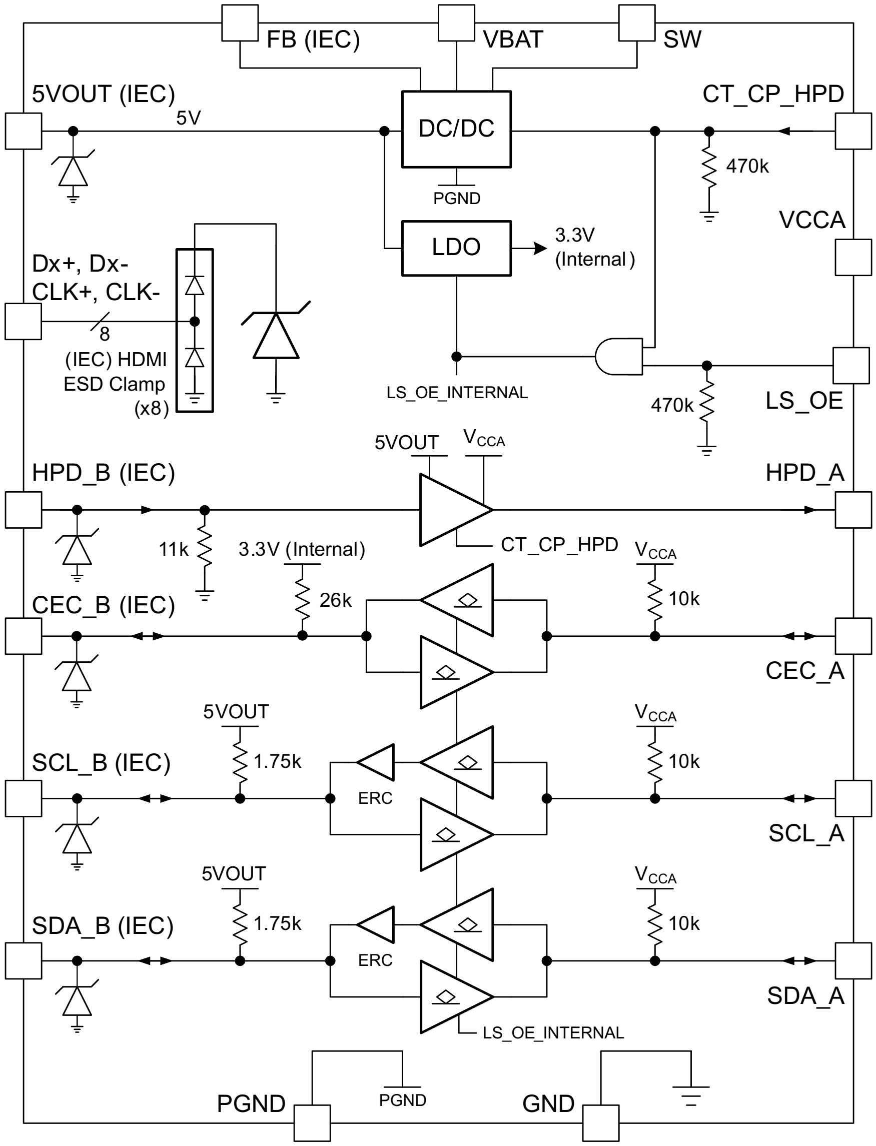
Application Schematics for HDMI controllers with TOW GPIOs for HDMI Interface Control



Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The LS_OE and CT__CP_HPD are active-high enable pins. They control the TPD12S015A power saving options according to the following table:

LS_OE	CT_CP_HPD	VCCA	VBAT	5VOUT	A-side Pull-ups	DDC, B-Side Pull-ups	CEC, B-Side Pull-ups	CEC LDO	DC/DC & HPD	DDC/CEC VLTs	ICC VCCA Typ	ICC VBAT Typ	Comment
L	**L**	1.8V	3.3V	Off	Off	Off	Off	Off	Off	Off	1µA	1µA	Fully Disabled
L	**H**	1.8V	3.3V	On	On	On	Off	Off	On	Off	1µA	30µA	DC/DC on
H	**L**	1.8V	3.3V	Off	Off	Off	Off	Off	Off	Off	1µA	1µA	Not Valid State
H	**H**	1.8V	3.3V	On	On	On	On	On	On	On	13µA	255µA	Fully On
X	**X**	0V	0V	Off	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	**X**	1.8V	0V	Off	Low	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	**X**	0V	3.3V	Off	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down

CIRCUIT BLOCK DIAGRAM



'3.3V (Internal)' is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3V from 5VOUT when LS_OE = H & CT_CP_HPD = H.

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
5VOUT	F1	Power Out	DC/DC output. The 5-V power pin can supply 55 mA regulated current to the HDMI receiver. Separate DC/DC converter control pin CT_CP_HPD disables the DC/DC converter when operating at low-power mode.
CEC_A	B2	I/O	System-side CEC bus I/O. This pin is bi-directional and referenced to V_{CCA}.
CEC_B	D3	I/O	HDMI-side CEC bus I/O. This pin is bi-directional and referenced to the 3.3-V internal supply.
CLK–, CLK+	G4, F4	ESD	High-speed ESD clamp: provides ESD protection to the high-speed HDMI differential data lines
CT_CP_HPD	D1	Control	DC/DC Enable. Enables the DC/DC converter and HPD circuitry when CT_CP_HPD = H. The CT_CP_HPD is referenced to V_{CCA}.
D0–, D0+, D1– , D1+, D2–, D2+	E4, D4, C4, B4, A4, A3	ESD	High-speed ESD clamp: provides ESD protection to the high-speed HDMI differential data lines
FB	E1	I	Feedback input. This pin is a feedback control pin for the DC/DC converter. It must be connected to 5VOUT.
GND	B3, C3, D2, E2	Ground	Device ground
HPD_A	C2	O	System-side output for the hot plug detect. This pin is unidirectional and is referenced to V_{CCA}.
HPD_B	G3	I	HDMI-side input for the hot plug detect. This pin is unidirectional and is referenced to 5VOUT.
LS_OE	A1	Control	Level shifter enable. This pin is referenced to V_{CCA}. Enables SCL, SDA, CEC level shifters, and LDO when LS_OE = H.
P_{GND}	G1	Analog Ground	DC/DC converter ground. This pin should be tied externally to the system GND plane. See board layout in applications section.
SCL_A	B1	I/O	System-side input/output for I2C bus. This pin is bi-directional and referenced to V_{CCA}.
SCL_B	E3	I/O	HDMI-side input/output for I^2C bus. This pin is bi-directional and referenced to 5VOUT.
SDA_A	C1	I/O	System-side input/output for I2C bus. This pin is bi-directional and referenced to V_{CCA}.
SDA_B	F3	I/O	HDMI-side input/output for I^2C bus. This pin is bi-directional and referenced to 5VOUT.
SW	F2	I	Switch input. This pin is the inductor input for the DC/DC converter.
V_{BAT}	G2	Supply	Battery supply. This voltage is typically 2.3 V to 5.5 V
V_{CCA}	A2	Supply	System-side supply. this voltage is typically 1.2 V to 3.3 V from the core microcontroller.

ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage range				4.0	V
V_{BAT}	Supply voltage range			–0.3	6.0	
V_I	Input voltage range		HPD_B, Dx, CLKx	–0.3	6.0	V
			CT_CP_HPD, LS_OE	–0.3	4.0	
V_O		Voltage range applied to any output in the high-impedance or power-off state[(2)]	SCL_A, SDA_A, CEC_A, HPD_A	–0.3	4.0	V
			SCL_B, SDA_B, CEC_B	–0.3	6.0	
		Voltage range applied to any output in the high or low state[(2)]	SCL_A, SDA_A, CEC_A, HPD_A	–0.3	V_{CCA} + 0.3	
			SCL_B, SDA_B, CEC_B	–0.3	6.0	
I_{IK}	Input clamp current		$V_I < 0$		–50	mA
I_{OK}	Output clamp current		$V_O < 0$		–50	mA
I_{OUTMAX}	Continuous current through 5VOUT or GND				±100	mA
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to "absolute maximum conditions" for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

over recommended operating free-air temperature range (unless otherwise noted)

			SUPPLY	MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage			1.1		3.6	V
V_{BAT}	Supply voltage			2.3		5.5	V
V_{IH}	High-level input voltage	SCL_A, SDA_A, CEC_A	V_{CCA} = 1.1 V to 3.6 V	0.7*V_{CCA}		V_{CCA}	V
		CT_CP_HPD, LS_OE		1		3.6	
		SCL_B, SDA_B	5VOUT = 5.0 V	0.7*5VOUT		5VOUT	
		CEC_B		0.7*3.3V (internal)[(1)]		3.3V (internal)[(1)]	
		HPD_B		2.0		5VOUT	
V_{IL}	Low-level input voltage	SCL_A, SDA_A, CEC_A	V_{CCA} = 1.1 V to 3.6 V	0		0.082*V_{CCA}	V
		CT_CP_HPD, LS_OE		0		0.4	
		SCL_B, SDA_B	5VOUT = 5.0 V	0		0.3*5VOUT	
		CEC_B		0		0.3*3.3V (internal)[(1)]	
		HPD_B		0		0.8	
V_{ILC}	Low-level input voltage (contention)	SCL_A, SDA_A, CEC_A	V_{CCA} = 1.1 V to 3.6 V	0		0.065*V_{CCA}	V
$V_{OL} – V_{ILC}$	Delta between V_{OL} and V_{ILC}	SCL_A, SDA_A, CEC_A	V_{CCA} = 1.1 V to 3.6 V		0.1*V_{CCA}		V
T_A	Operating free-air temperature			–40		85	°C

(1) '3.3V (internal)' is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3V from 5VOUT when LS_OE = H & CT_CP_HPD = H.

ESD RATINGS

PARAMETER	PINS	TYP	UNIT
Human Body Model JESD22 A114-B	SCL_A, SDA_A, CEC_A, CT_CP_HPD, LS_OE, VCCA	2.5	kV
Charged Device Model JESD22 C101	ALL	1000	V
IEC 61000-4-2 Contact Discharge	D0+, D0-, D1+, D1-, D2+, D2-, CLK+, CLK-, SCL_B, SDA_B, CEC_B, HPD_B, 5VOUT, FB	±8	kV
Human Body Model	D0+, D0-, D1+, D1-, D2+, D2-, CLK+, CLK-, SCL_B, SDA_B, CEC_B, HPD_B, 5VOUT, FB	±15	kV

ELECTRICAL CHARACTERISTICS

I_{CC}

PARAMETER		PIN	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCA}	Standby	V_{CCA}	I/O = High			2	µA
	Active					15	
I_{CCB}	Standby	V_{BAT}	CT_CP_HPD=L, LS_OE=L, HPD_B=L		2		µA
	DC/DC and HPD active		CT_CP_HPD=H, LS_OE=L, HPD_B=L		30	50	
	DC/DC, HPD, DDC, CEC active		CT_CP_HPD=H LS_OE=H, HPD_B=L, I/O =H		225	300	

High-Speed ESD Lines: Dx, CLK

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OFF}	Current from IO port to supply pins	V_{CC} = 0 V, V_{IO} = 3.3 V			0.01	0.5	µA
V_{DL}	Diode forward voltage	I_D = 8 mA,	Lower clamp diode		0.85	1.0	V
R_{DYN}	Dynamic resistance	I = 1 A	D, CLK		1		Ω
C_{IO}	IO capacitance	V_{CC} = 5 V V_{IO} = 2.5 V	D, CLK		1.3		pF
V_{BR}	Break-down voltage	I_{IO} = 1mA		9		12	V

DC-DC Converter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Input voltage range		2.3		5.5	V
5VOUT	Total DC output voltage	Includes voltage references, DC load / line regulations, process and temperature	4.9	5	5.13	V
TOVA	Total output voltage accuracy	Includes voltage references, DC load / line regulations, transient load / line regulations, ripple, process and temperature	4.8	5	5.3	V
V_{O_Ripple}	Output voltage ripple, loaded	I_O = 65 mA			20	mV (p-p)
F_clk	Internal operating frequency	V_{BAT} = 2.3 V to 5.5 V		3.5		MHz
t_{start}	Startup time	From CT_CP_HPD input to 5 V power output 90% point			300	µs
I_O	Output current	V_{BAT} = 2.3 V to 5.5 V	55			mA
	Reverse leakage current V_O	CT_CP_HPD= L, V_O = 5.5 V			2.5	µA
	Leakage current from battery to V_O	CT_CP_HPD= L			5	µA
V_{BATUVT}	Under voltage lockout threshold	Falling		2		V
		Rising		2.1		V
V_{BATOVT}	Over voltage lockout threshold	Falling		5.9		V
		Rising		6.0		V
	Line transient response	V_{BAT} = 3.6 V, a pulse of 217Hz 600 mVp-p square wave, I_O = 20/65 mA		±25	±50	mVpk

DC-DC Converter (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Load transient response	V_{BAT} = 3.6 V, I_O = 5 to 65 mA, pulse of 10 µs, t_r = t_f = 0.1 µs		50		mVpk
$I_{DD\ (idle)}$	Power supply current from V_{BAT} to DC/DC, enabled, unloaded	I_O = 0 mA		30	50	µA
$I_{DD\ (disabled)}$	Power supply current from V_{BAT}, DC/DC Disabled, Unloaded	V_{BAT} = 2.3 V to 5.5 V, I_O = 0 mA, CT_CP_HPD Low			2	µA
$I_{DD(system\ off)}$	Power supply current from V_{BAT}, VCCA =0V	V_{CCA} = 0 V			5	µA
I_inrush (startup)	Inrush current, average over T_startup time	V_{BAT} = 2.3 V to 5.5 V, I_O = 65 mA		100		mA
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
ΔT_{SD}	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
I_{SC}	Short circuit current limit from output	5Ω short to GND			500	mA

Passive Components

PARAMETER		TYP	UNIT
L_{IN}	External inductor, 0805 footprint	1	µH
C_{IN}	Input capacitor, 0603 footprint	4.7	µF
C_{OUT}	Output capacitor, 0603 footprint	4.7	µF
C_{VCCA}	Input capacitor, 0402 footprint	0.1	µF

Voltage Level Shifter: SCL, SDA Lines (x_A/x_B Ports)

T_A = –40°C to 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –10 µA,	$V_I = V_{IH}$	1.1 V to 3.6 V	V_{CCA} × 0.8			V
V_{OLA}		I_{OL} = 10 µA,	$V_I = V_{IL}$	1.1 V to 3.6 V		V_{CCA} × 0.17		V
V_{OHB}		I_{OH} = –10 µA,	$V_I = V_{IH}$		5VOUT × 0.9			V
V_{OLB}		I_{OL} = 3 mA,	$V_I = V_{IL}$				0.4	V
ΔV_T hysteresis	SDx_A ($V_{T+} - V_{T–}$)			1.1 V to 3.6 V		40		mV
	SDx_B ($V_{T+} - V_{T–}$)			1.1 V to 3.6 V		400		
R_{PU}	(Internal pullup)	SCL_A, SDA_A,	Internal pullup connected to V_{CCA} rail			10		kΩ
		SCL_B, SDA_B,	Internal pullup connected to 5 V rail			1.75		
$I_{PULLUPAC}$	Transient boosted pullup current (rise time accelerator)	SCL_B, SDA_B,	Internal pullup connected to 5 V rail			15		mA
I_{OFF}	A port	V_{CCA} = 0 V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		0 V to 3.6 V			±5	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND		1.1 V to 3.6 V			±5	µA
	A port	$V_I = V_{CCI}$ or GND		1.1 V to 3.6 V			±5	

Voltage Level Shifter: CEC Lines (x_A/x_B Ports)

T_A = –40°C to 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –10 µA,	$V_I = V_{IH}$	1.1 V to 3.6 V	V_{CCA} × 0.8			V
V_{OLA}		I_{OL} = 10 µA,	$V_I = V_{IL}$	1.1 V to 3.6 V			V_{CCA} × 0.17	V
V_{OHB}		I_{OH} = –10 µA,	$V_I = V_{IH}$		3.3V (internal) × 0.9 (1)			V
V_{OLB}		I_{OL} = 3 mA,	$V_I = V_{IL}$				0.4	V
ΔV_T hysteresis	CEC_A ($V_{T+} – V_{T–}$)			1.1 V to 3.6 V		40		mV
	CEC_B ($V_{T+} – V_{T–}$)			1.1 V to 3.6 V		300		
R_{PU}	(Internal pullup)	CEC_A	Internal pullup connected to V_{CCA} rail			10		kΩ
		CEC_B	Internal pullup connected to internal 3.3 V rail			26		
I_{OFF}	A port	V_{CCA} = 0 V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		0 V to 3.6 V			±1.8	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND		1.1 V to 3.6 V			±5	µA
	A port	$V_I = V_{CCI}$ or GND		1.1 V to 3.6 V			±5	

(1) '3.3V (internal)' is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3V from 5VOUT when LS_OE = H & CT_CP_HPD = H

Voltage Level Shifter: HPD Line (x_A/x_B Ports)

T_A = –40°C to 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –3 mA,	$V_I = V_{IH}$	1.1 V to 3.6 V	V_{CCA} × 0.7			V
V_{OLA}		I_{OL} = 3 mA,	$V_I = V_{IL}$	1.1 V to 3.6 V			0.4	V
ΔV_T hysteresis	HPD_B ($V_{T+} – V_{T–}$)			1.1 V to 3.6 V		200		mV
R_{PD}	(Internal pulldown)	HPD_B,	Internal pulldown connected to GND			11		kΩ
I_{OZ}	A port	$V_I = V_{CCI}$ or GND		3.6 V			±5	µA

LS_OE, CT_CP_HPD

T_A = –40°C to 85°C unless otherwise specified

PARAMETER	TEST CONDITIONS	V_{CCA}	MIN	TYP	MAX	UNIT
I_I	$V_I = V_{CCA}$ or GND	1.1 V to 3.6 V			±12	µA

I/O Capacitance

T_A = –40°C to 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS	V_{CCA}	MIN	TYP	MAX	UNIT
C_I	Control inputs	V_I = 1.89 V or GND, AC input = 30 mV(p-p); f = 10 MHz	1.1 V to 3.6 V		7.1		pF
C_{IO}	A port	V_O = 1.89 V or GND, AC input = 30 mV(p-p); f = 10 MHz, CT_CP_HPD = H, LS_OE = L	1.1 V to 3.6 V		8.3		pF
	B port	V_O = 5.0 V or GND, AC input = 30 mV(p-p); f = 10 MHz, CT_CP_HPD = H, LS_OE = L	3.3 V		15		pF

I/O Capacitance (continued)

T_A = –40°C to 85°C unless otherwise specified

PARAMETER		TEST CONDITIONS	V_{CCA}	MIN	TYP	MAX	UNIT
C_{IO}	SCL_B, SDA_B	V_{BAT} = 0 V, V_{bias} = 2.5 V; AC input = 3.5 V(p-p); f = 100 kHz	0 V		20		pF
	CEC_B	V_{BAT} = 0 V, V_{bias} = 1.65 V; AC input = 2.5 V(p-p); f = 100 kHz	0 V		20		pF
		V_{BAT} = 3.3V, V_{bias} = 1.65 V; AC input = 2.5 V(p-p); f = 100 kHz, CT_CP_HPD = H, LS_OE = L	3.3 V		20		pF

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_L	Bus load capacitance (B side)				750	pF
	Bus load capacitance (A side)				15	

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 1.2V

V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay	A to B	DDC Channels Enabled		344		ns
		B to A			355		
t_{PLH}	Propagation delay	A to B	DDC Channels Enabled		452		ns
		B to A			178		
t_f	A port fall time	A Port	DDC Channels Enabled		138		ns
	B port fall time	B Port			83		
t_r	A port rise time	A Port	DDC Channels Enabled		194		ns
	B port rise time	B Port			92		
f_{MAX}	Maximum switching frequency		DDC Channels Enabled	400			kHz

Voltage Level Shifter: CEC Line (x_A & x_B ports); VCCA = 1.2V

V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	CEC Channels Enabled		445		ns
		B to A			337		
t_{PLH}		A to B			13		μs
		B to A			0.266		
t_f	A port fall time	A Port	CEC Channels Enabled		140		ns
	B port fall time	B Port			96		
t_r	A port rise time	A Port	CEC Channels Enabled		202		ns
	B port rise time	B Port			15		μs

Voltage Level Shifter: HPD Line (x_A & x_B ports); VCCA = 1.2V

V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	B to A	CEC Channels Enabled		10		μs
t_{PLH}		B to A			9		
t_f	A port fall time	A Port	CEC Channels Enabled		0.67		ns
t_r	A port rise time	A Port	CEC Channels Enabled		0.74		ns

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 1.5V

V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	DDC Channels Enabled		335		ns
		B to A			265		
t_{PLH}		A to B			438		
		B to A			169		

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 1.5V (continued)

V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	A port fall time	A Port	DDC Channels Enabled		110		ns
	B port fall time	B Port			83		
t_r	A port rise time	A Port	DDC Channels Enabled		190		ns
	B port rise time	B Port			92		
f_{MAX}	Maximum switching frequency		DDC Channels Enabled	400			kHz

Voltage Level Shifter: CEC Line (x_A & x_B ports); VCCA = 1.5V

V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	CEC Channels Enabled		437		ns
		B to A			267		
t_{PLH}		A to B			13		µs
		B to A			0.264		
t_f	A port fall time	A Port	CEC Channels Enabled		110		ns
	B port fall time	B Port			96		
t_r	A port rise time	A Port	CEC Channels Enabled		202		ns
	B port rise time	B Port			15		µs

Voltage Level Shifter: HPD Line (x_A & x_B ports); VCCA = 1.5V

V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	B to A	CEC Channels Enabled		10		µs
t_{PLH}		B to A			9		
t_f	A port fall time	A Port	CEC Channels Enabled		0.47		ns
t_r	A port rise time	A Port	CEC Channels Enabled		0.51		ns

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 1.8V

V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	DDC Channels Enabled		334		ns
		B to A			229		
t_{PLH}		A to B			431		
		B to A			169		
t_f	A port fall time	A Port	DDC Channels Enabled		94		ns
	B port fall time	B Port			83		
t_r	A port rise time	A Port	DDC Channels Enabled		191		ns
	B port rise time	B Port			92		
f_{MAX}	Maximum switching frequency		DDC Channels Enabled	400			kHz

Voltage Level Shifter: CEC Line (x_A & x_B ports); VCCA = 1.8V

V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	CEC Channels Enabled		441		ns
		B to A			231		
t_{PLH}		A to B			13		µs
		B to A			0.26		
t_f	A port fall time	A Port	CEC Channels Enabled		94		ns
	B port fall time	B Port			96		
t_r	A port rise time	A Port	CEC Channels Enabled		201		ns
	B port rise time	B Port			15		µs

Voltage Level Shifter: HPD Line (x_A & x_B ports); VCCA = 1.8V

V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	B to A	CEC Channels Enabled		10		µs
t_{PLH}		B to A			9		
t_f	A port fall time	A Port	CEC Channels Enabled		0.41		ns
t_r	A port rise time	A Port	CEC Channels Enabled		0.45		ns

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 2.5V

V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	DDC Channels Enabled		330		ns
		B to A			182		
t_{PLH}		A to B			423		
		B to A			166		
t_f	A port fall time	A Port	DDC Channels Enabled		79		ns
	B port fall time	B Port			83		
t_r	A port rise time	A Port	DDC Channels Enabled		188		ns
	B port rise time	B Port			92		
f_{MAX}	Maximum switching frequency		DDC Channels Enabled	400			kHz

Voltage Level Shifter: CEC Line (x_A & x_B ports); VCCA = 2.5V

V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	CEC Channels Enabled		454		ns
		B to A			184		
t_{PLH}		A to B			13		µs
		B to A			0.255		
t_f	A port fall time	A Port	CEC Channels Enabled		79		ns
	B port fall time	B Port			96		
t_r	A port rise time	A Port	CEC Channels Enabled		194		ns
	B port rise time	B Port			15		µs

Voltage Level Shifter: HPD Line (x_A & x_B ports); VCCA = 2.5V

V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	B to A	CEC Channels Enabled		10		μs
t_{PLH}		B to A			9		
t_f	A port fall time	A Port	CEC Channels Enabled		0.37		ns
t_r	A port rise time	A Port	CEC Channels Enabled		0.39		ns

Voltage Level Shifter: SCL, SDA Lines (x_A & x_B ports); VCCA = 3.3V

V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	DDC channels enabled		323		ns
		B to A			158		
t_{PLH}		A to B			421		
		B to A			162		
t_f	A port fall time	A Port	DDC channels enabled		71		ns
	B port fall time	B Port			84		
t_r	A port rise time	A Port	DDC channels enabled		188		ns
	B port rise time	B Port			92		
f_{MAX}	Maximum switching frequency		DDC channels enabled	400			kHz

Voltage Level Shifter: CEC Line (x_A & x_B ports); VCCA = 3.3V

V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	A to B	CEC channels enabled		450		ns
		B to A			160		
t_{PLH}		A to B			13		μs
		B to A			0.251		
t_f	A port fall time	A Port	CEC channels enabled		71		ns
	B port fall time	B Port			96		
t_r	A port rise time	A Port	CEC channels enabled		194		ns
	B port rise time	B Port			15		μs

Voltage Level Shifter: HPD Line (x_A & x_B ports); VCCA = 3.3V

V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	B to A	CEC channels enabled		10		μs
t_{PLH}		B to A			9		
t_f	A port fall time	A Port	CEC channels enabled		0.35		ns
t_r	A port rise time	A Port	CEC channels enabled		0.37		ns

APPLICATION INFORMATION

DDC/CEC Level Shift Circuit Operation

The TPD12S015A enables DDC translation from V_{CCA} (system side) voltage levels to 5V (HDMI cable side) voltage levels without degradation of system performance. The TPD12S015A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, VCCA side DDC-bus and the 5V DDC-bus. The port B I/Os are over-voltage tolerant to 5.5 V even when the device is unpowered. After powerup and with the LS_OE and CT_CP_HPD pins high, a low level on port A (below approximately V_{ILC} = 0.08*V_{CCA} V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to V_{OLB} V. When port A rises above approximately 0.10*VCCA V, the port B pulldown driver is turned off and the internal pullup resistor pulls the pin high. When port B falls first and goes below 0.3*5VOUT, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately V_{OLA} = 0.16*V_{CCA} V. The port B pulldown is not enabled unless the port A voltage goes below V_{ILC}. If the port A low voltage goes below V_{ILC}, the port B pulldown driver is enabled until port A rises above (V_{ILC} + $\Delta V_{T\text{-}HYSTA}$), then port B, if not externally driven LOW, will continue to rise being pulled up by the internal pullup resistor.

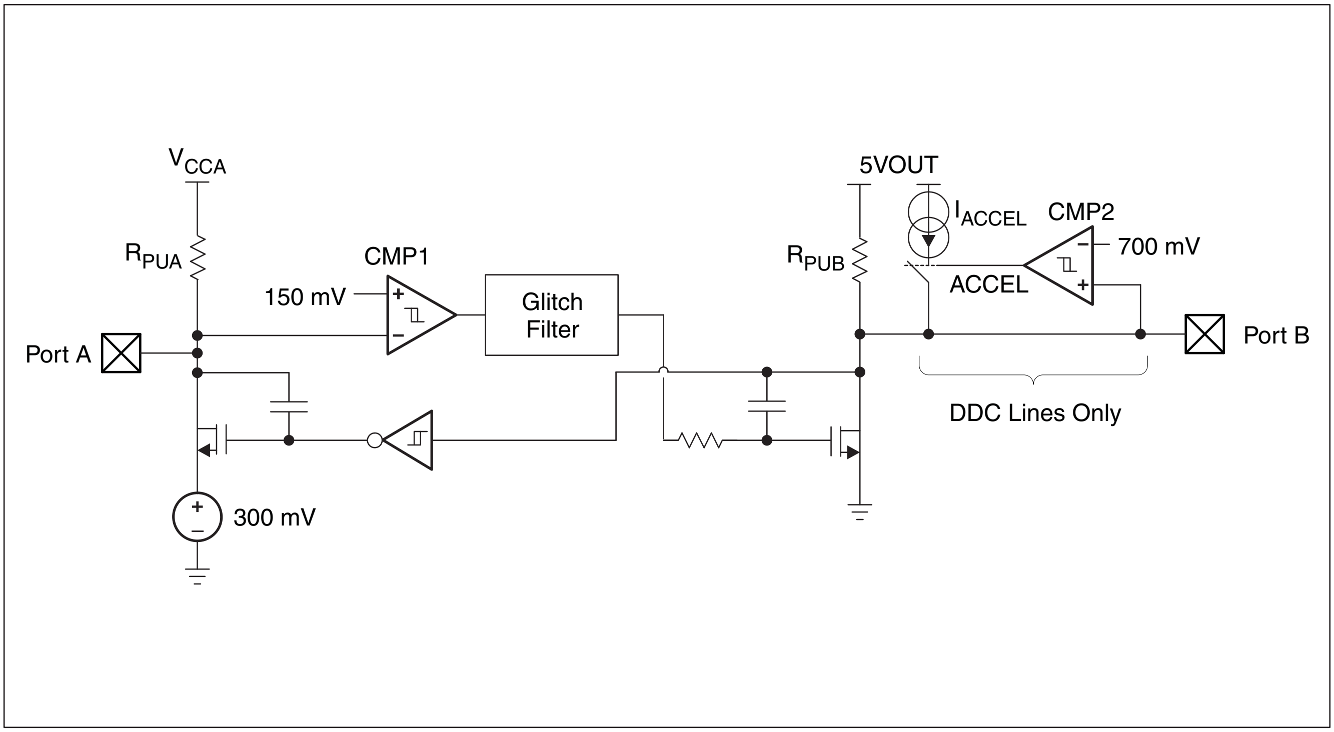


Figure 2. DDC/CEC Level Shifter Block Diagram

DDC/CEC Level Shifter Operational Notes for V_{CCA} = 1.8 V

- The threshold of CMP1 is ~150mV +/- the 40mV of total hysteresis.
- The comparator will trip for a falling waveform at ~130mV
- The comparator will trip for a rising waveform at ~170mV
- To be recognized as a zero, the level at Port A must first go below 130mV (VILC in spec) and then stay below 170mV (VILA in spec)
- To be recognized as a one, the level at A must first go above 170mV and then stay above 130mV
- VILC is set to 110mV in Electrical Characteristics Table to give some margin to the 130mV
- VILA is set to 140mV in the Electrical Characteristics Table to give some margin to the 170mV
- VIHA is set to 70% of VCCA to be consistent with standard CMOS levels

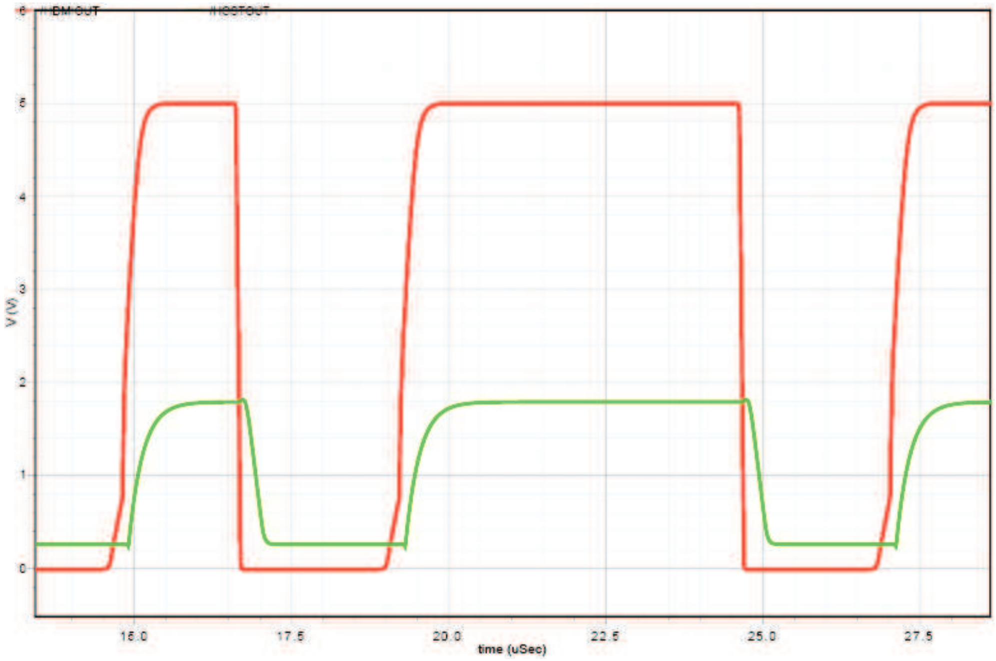


Figure 3. DDC/CEC Level Shifter Operation (B to A Direction)

Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise time accelerator boosts the cable side DDC signal independent of which side of the bus is releasing the signal.

Remark

Ground offset between the TPD12S015A ground and the ground of devices on port A of the TPD12S015A must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 ohms or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the TPD12S015A to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since VILC can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD12S015A as their output LOW levels will not be recognized by the TPD12S015A as a LOW. If the TPD12S015A is placed in an application where the VIL of port A of the TPD12S015A does not go below its VILC it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided. Port B is interoperable with all I^2C bus slaves, masters and repeaters.

CEC Level Shift Operation

The CEC level shift function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

Internal Pullup Resistor

The TPD12S015A has incorporated all the required pullup and pulldown resistors at the interface pins. The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines. For proper system operation no external resistors should be placed at the A and B ports. If there is internal pullups at the host processor, they should be disabled.

Power-Save Mode

The TPD12S015A integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

Under-Voltage Lockout

The under voltage lockout circuit prevents the DC/DC converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{BATUV}. The under-voltage lockout threshold V_{BATUV} for falling V_{IN} is typically 2.0V. The device starts operation once the rising VIN trips under-voltage lockout threshold V_{BATUV} again at typical 2.1 V.

Enable

The DC/DC converter is enabled when the CT_CP_HPD is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in typically 250 µs after the device has been enabled. The CT_CP_HPD input can be used to control power sequencing in a system with various DC/DC converters. The CT_CP_HPD pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With CT_CP_HPD = GND, the dc/dc enters shutdown mode.

Soft Start

The DC/DC converter has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage reaches its nominal value within tStart of typically 250 µs after CT_CP_HPD pin has been pulled to high level. The output voltage ramps up from 5% to its nominal value within t_{Ramp} of 300 µs. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches V_{IN}. Once the output voltage trips this threshold, the device operates with its nominal current limit ILIMF.

Inductor Selection

To make sure that the TPD12S015A devices can operate, an inductor must be connected between pin V_{BAT} and pin L. A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (5VOUT). Estimation of the maximum average inductor current can be done using Equation 1.

$$I_{L\_MAX} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \tag{1}$$

For example, for an output current of 55 mA at 5VOUT, approx 150 mA of average current flows through the inductor at a minimum input voltage of 2.3 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using Equation 2.

$$L_{MIN} \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}} \tag{2}$$

Parameter *f* is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 20% x I_L. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications a 1.0 µH inductance is recommended. The device has been optimized to operate with inductance values between 1.0 µH and 1.3 µH. It is recommended that an inductance value of at least 1.0 µH is used, even if Equation 2 yields something lower. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 3 shows how to calculate the peak current I.

$$I_{L(peak)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \quad (3)$$

where $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents.

Input Capacitor

Because of the nature of the boost converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. At least 1.2 uF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the V_{IN} and GND pins and better to use a 4.7 uF capacitor, in order to improve the input noise filtering.

Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the V_{OUT} and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 4 can be used.

$$C_{\min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (4)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple. With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using $\Delta V_{ESR} = I_{OUT} \times R_{ESR}$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value should be 1.2 uF but preferred value is about 4.7 uF

Table 1. Passive Components: Recommended Minimum Effective Values

COMPONENT	MIN	TARGET	MAX	UNIT
C_{IN}	1.2	4.7	6.5	µF
C_{OUT}	1.2	4.7	10	µF
L_{IN}	0.7	1	1.3	µH

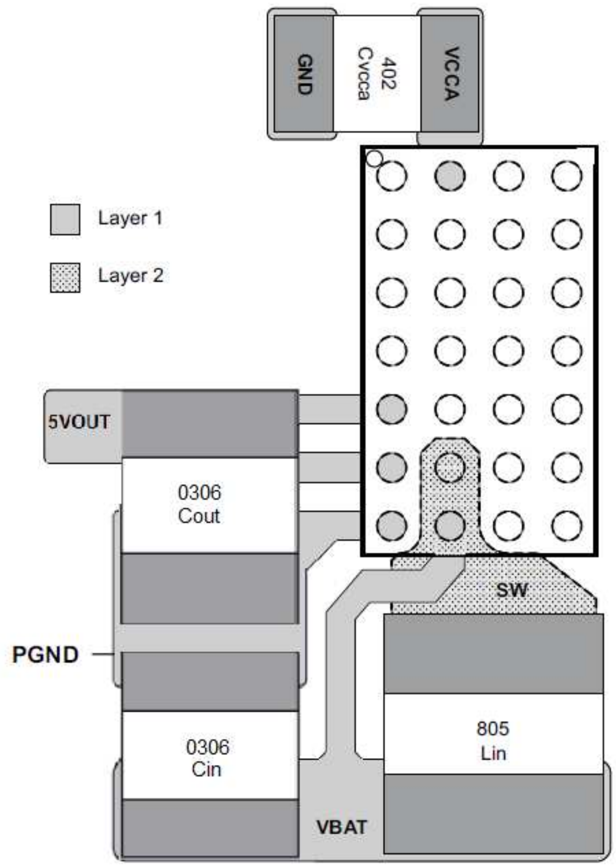


Figure 4. Board Layout (DC-DC Components) (Top View)

List of components:

- L_{IN} = MURATA LQM21PN1R0MC0 (1.0 µH, 800 mA, 0805, Shielded)
- C_{IN} = C_{OUT} = MURATA LLL31MR70J475MA01 (4.7 µF, Low ESL type, 6.3 V, 0306, X7R)
- C_{VCCA} = MURATA GRM155R60J475ME87D (0.1 µF, 6.3 V, 0402, X5R)

TPD12S015A EVM Layout

The TPD12S015A EVM has been designed for HDMI functional testing and includes both HDMI A-type and HDMI C-type connectors. Board jumpers enable and disable the dc-dc and level shifting circuitry. There are two supply terminals (VCCA and VBAT) and one GND terminal at the edge of the board. High speed lines were kept on top and bottom layers and matched for 50 Ω line to GND. All the high speed lines are matched to minimize the skew. The board has three test fixtures for testing the TPD12S015A in the following environments:

- The top segment enables system designers to test the TPD12S015A using the HDMI Class A connector
- The middle segment enables the system designers to test to test the TPD12S015A using the HDMI Class C connector
- The bottom segment enables the system designers to test signal integrity and eye pattern using differential probe.

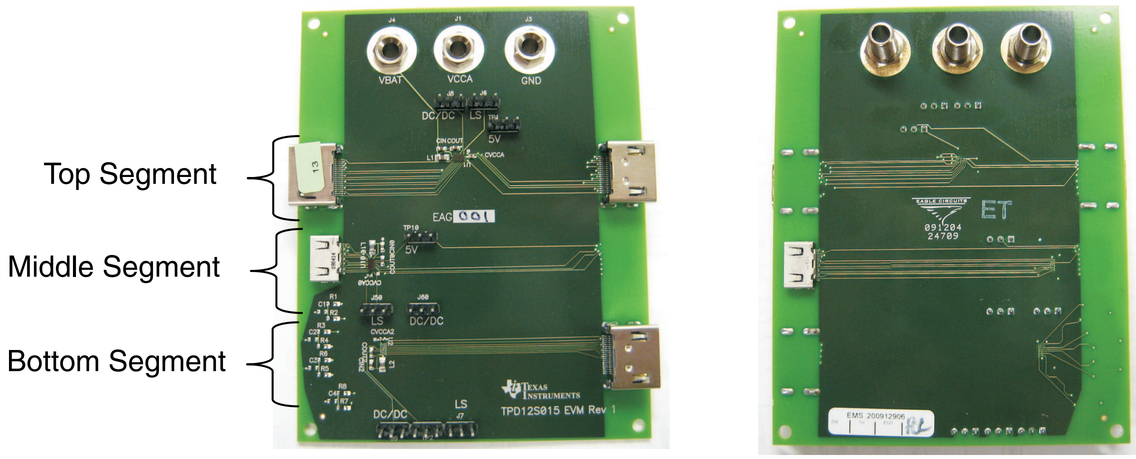


Figure 5. TPD12S015A EVM Top and Bottom View

The EVM board has 6 layers. The signal stack up is described below:

BOARD LAYER	DESCRIPTION
Layer 1	High-speed signal layer
Layer 2	Ground plane
Layer 3	Control signal layer
Layer 4	Control signal layer
Layer 5	Power plane
Layer 6	High-speed signal layer

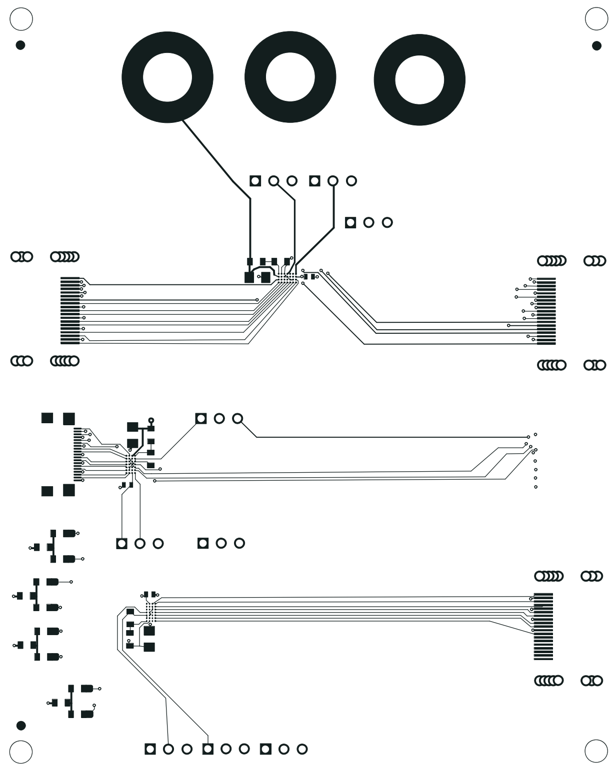


Figure 6. Layer 1: High-Speed Signal layer

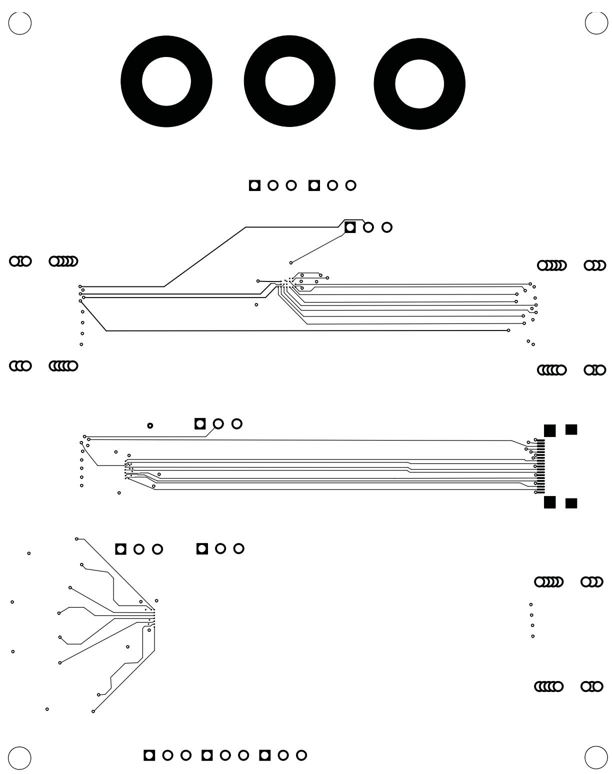


Figure 7. Layer 6: High-Speed Signal layer

TYPICAL CHARACTERISTICS

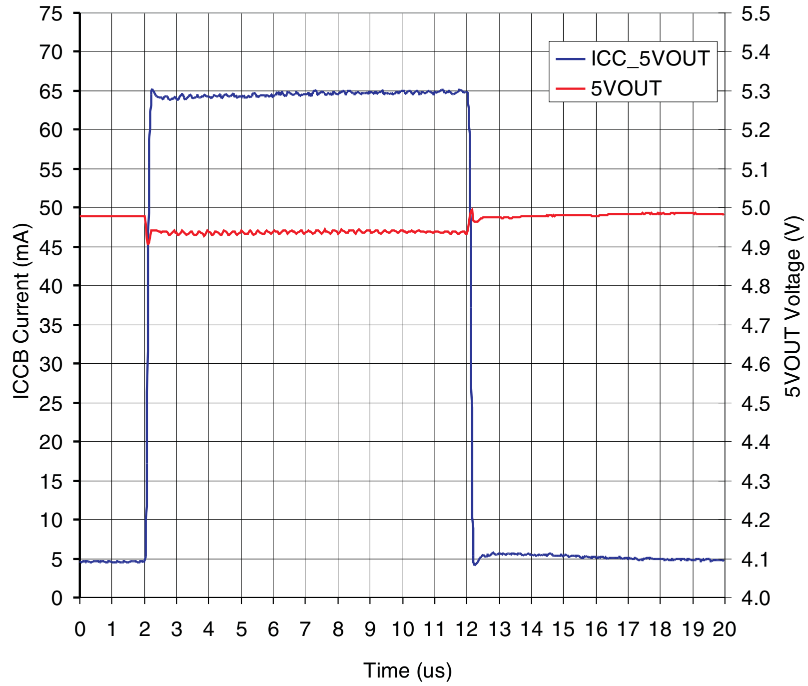


Figure 8. Load Transient Response

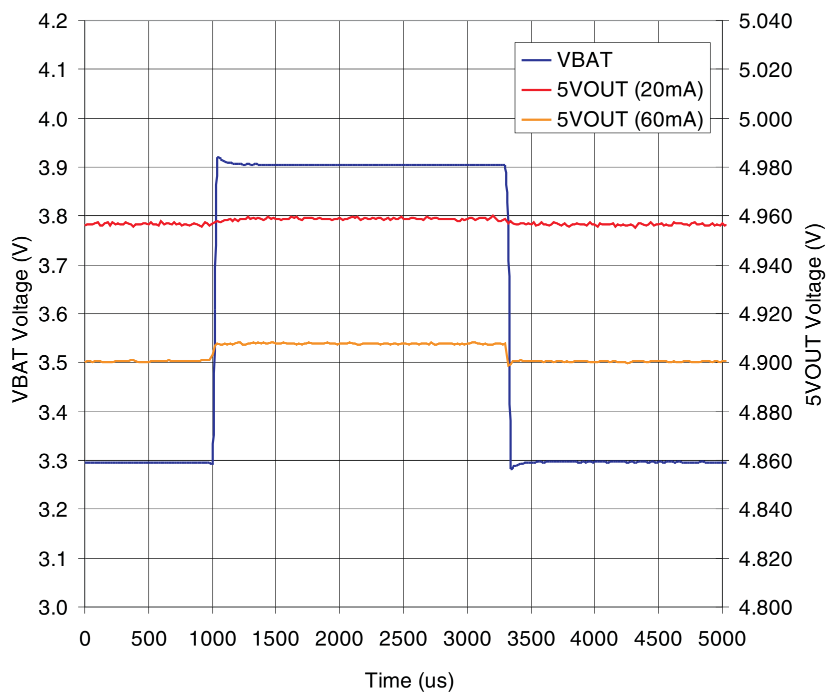


Figure 9. Line Transient Response

TYPICAL CHARACTERISTICS (continued)

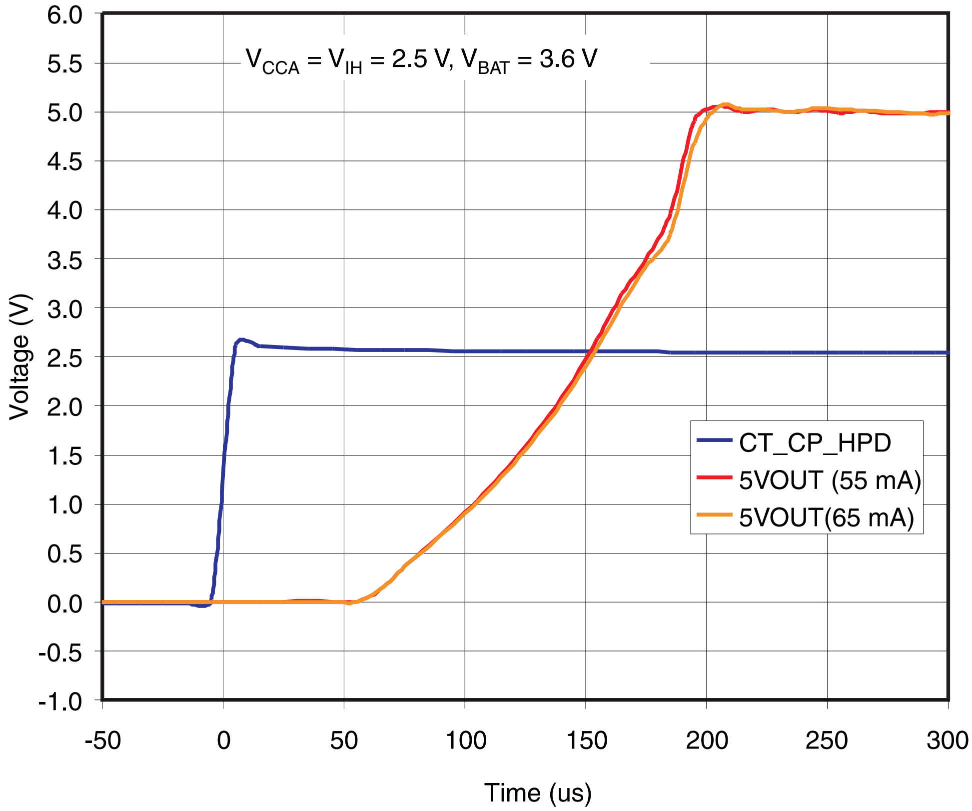


Figure 10. t_{START}

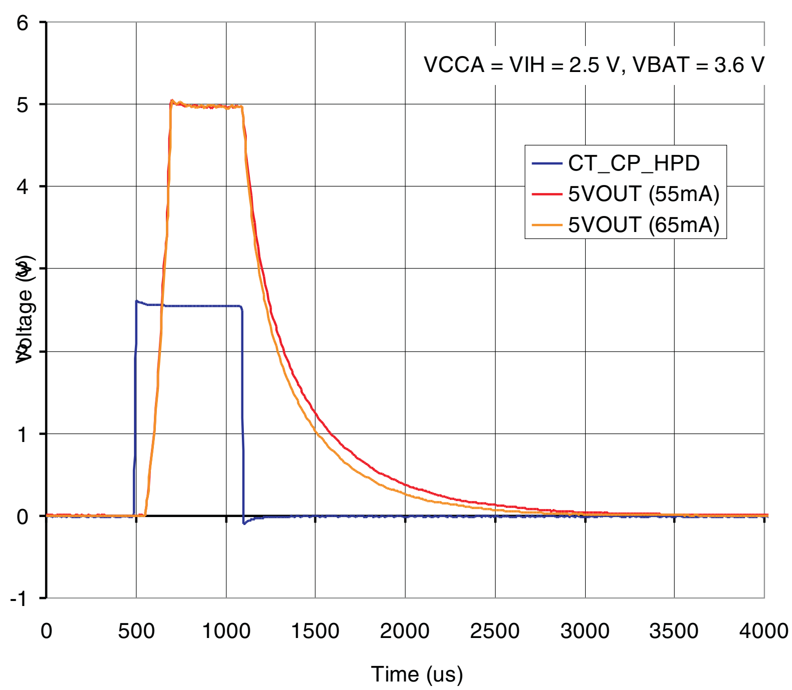


Figure 11. DC/DC Startup and Shutdown

TYPICAL CHARACTERISTICS (continued)

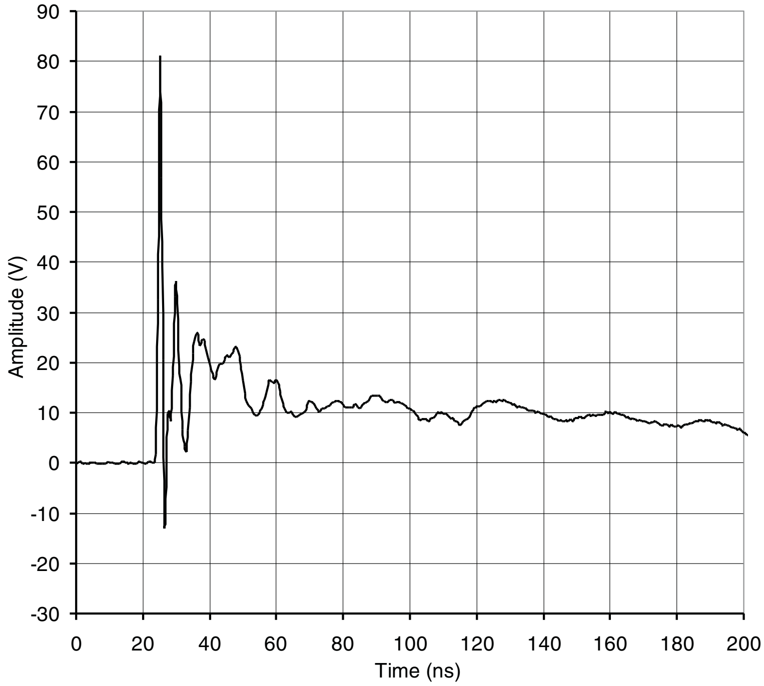


Figure 12. IEC Clamping Waveforms 8 kV Contact (IEC ESD Pins)

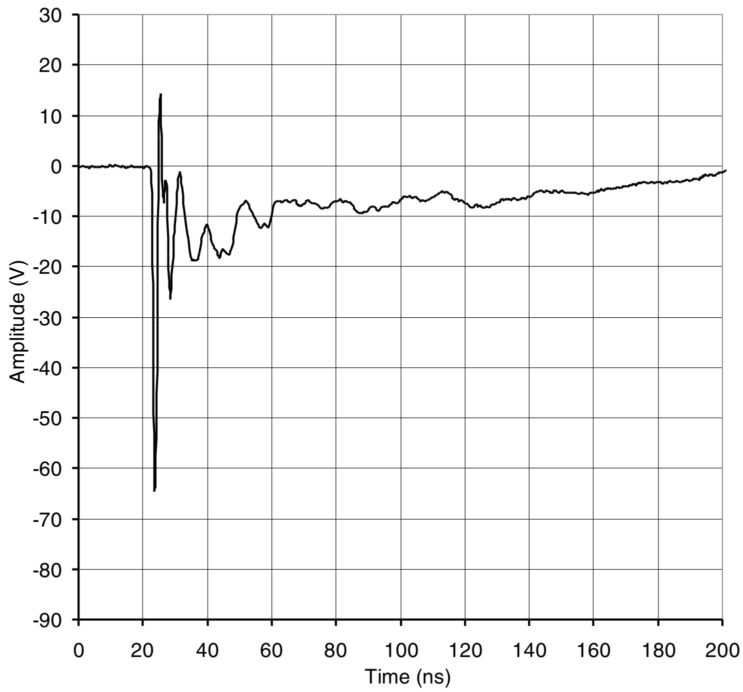


Figure 13. IEC Clamping Waveforms -8 kV Contact (IEC ESD Pins)

TYPICAL CHARACTERISTICS (continued)

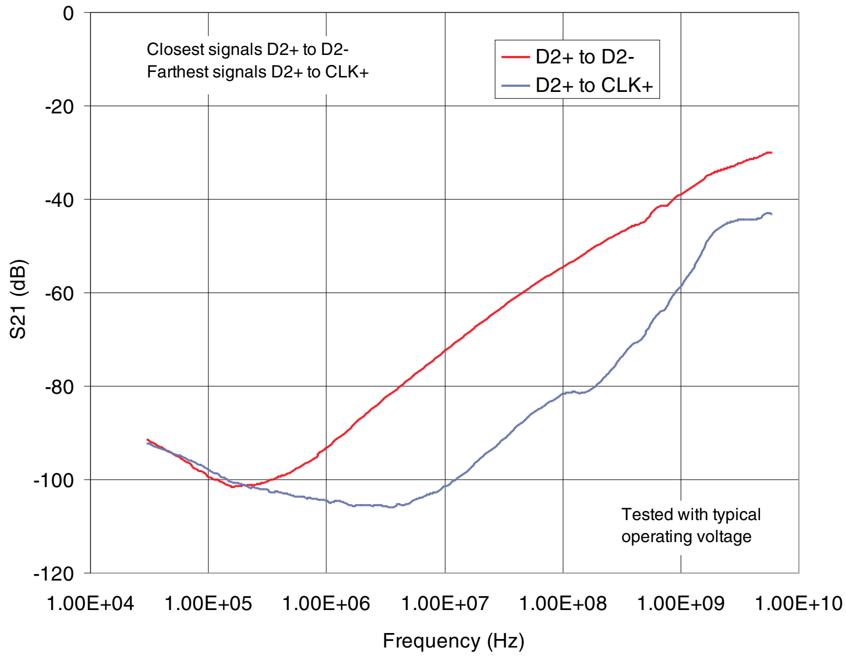


Figure 14. Channel-to-Channel Crosstalk

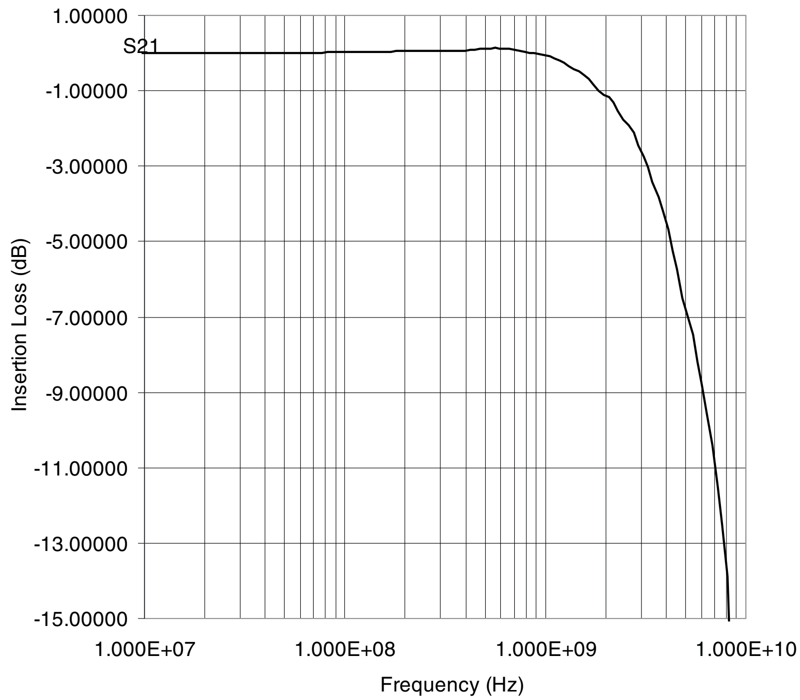


Figure 15. Insertion Loss Data Line to GND

TYPICAL CHARACTERISTICS (continued)

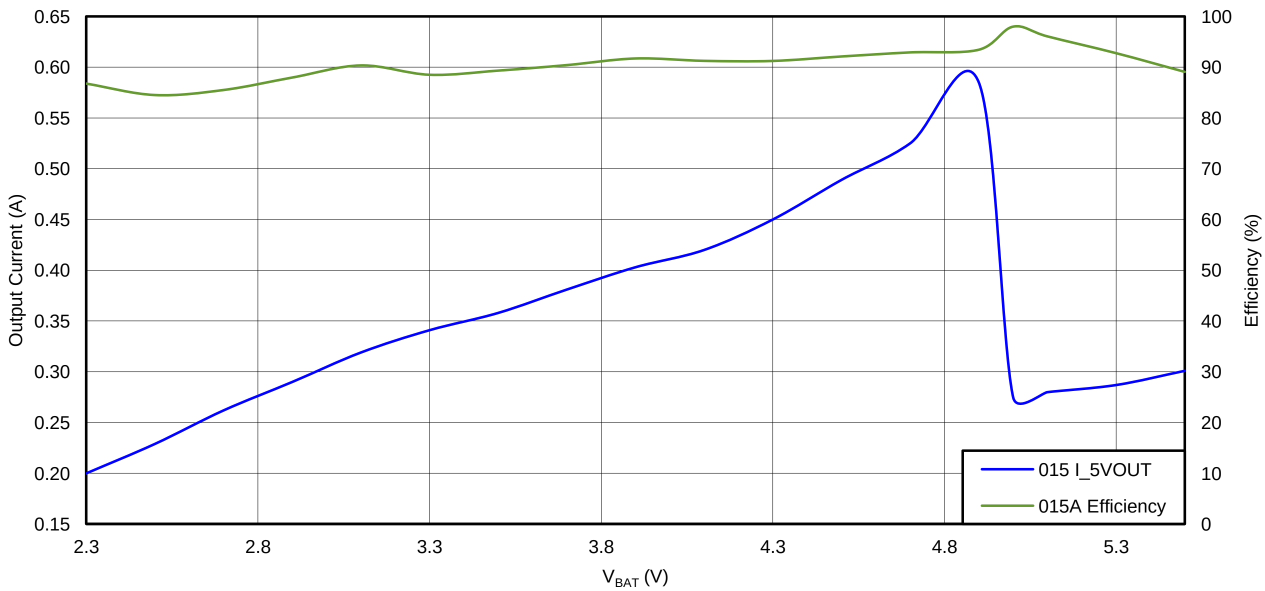


Figure 16. Power Derating Curve

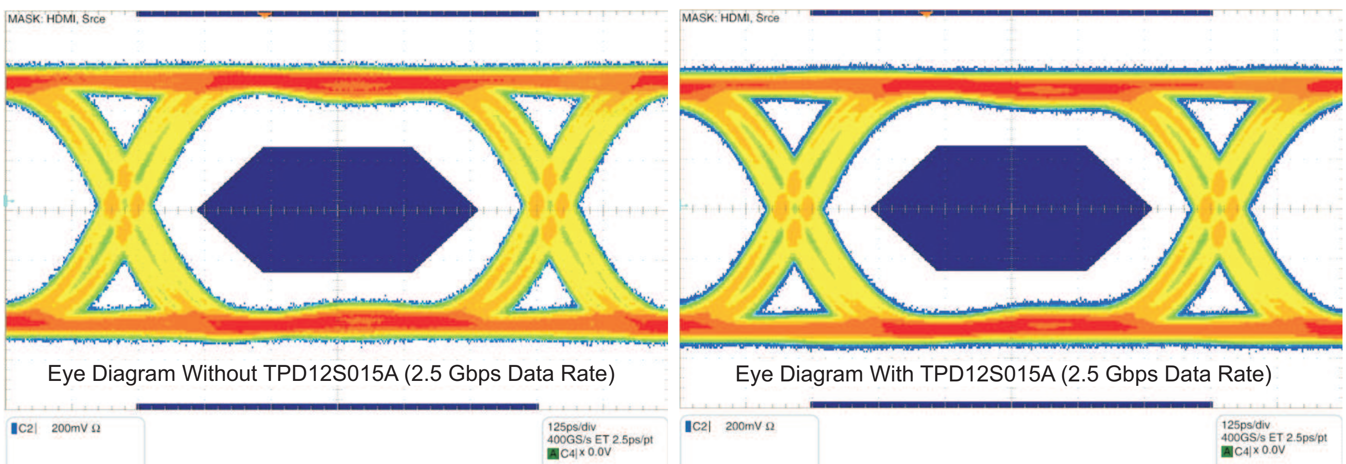


Figure 17. Eye Diagram Performance on a Test Board for the D+, D- Lines at 2.5 Gbps

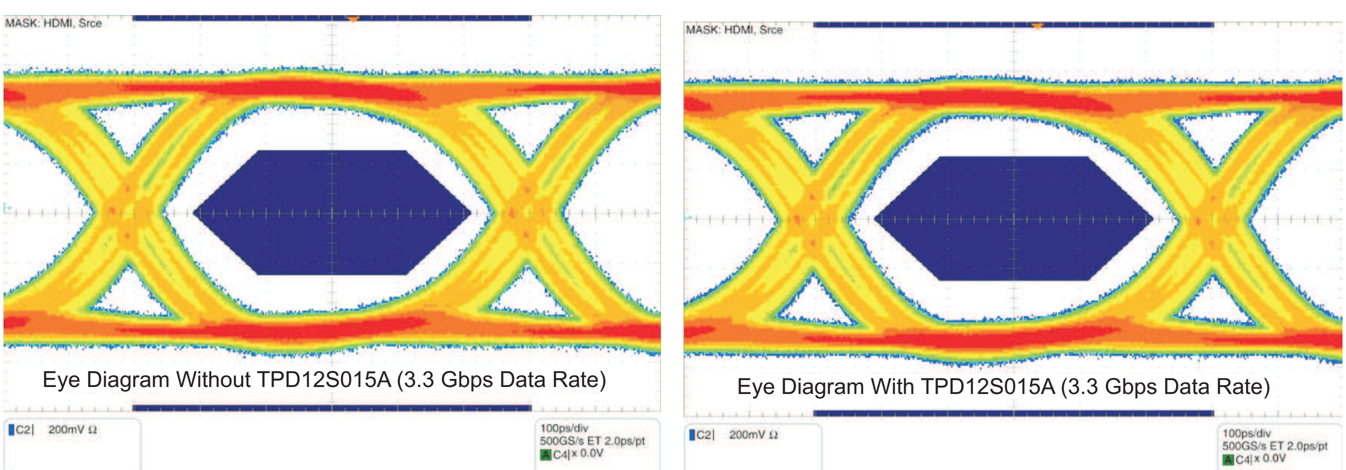
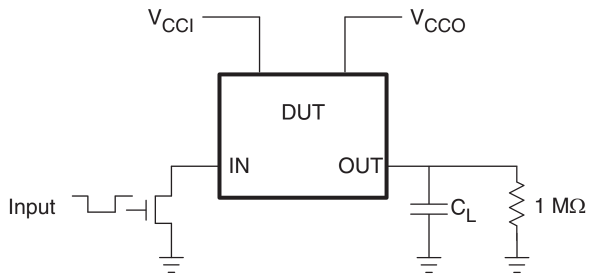
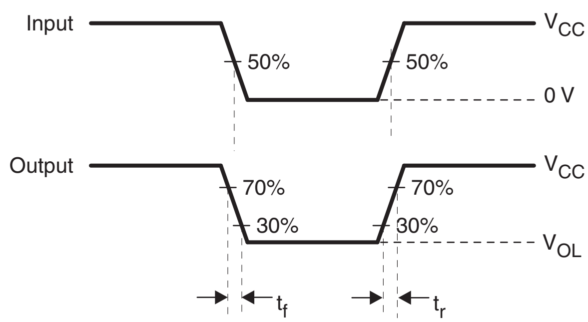


Figure 18. Eye Diagram Performance on a Test Board for the D+, D- Lines at 3.3 Gbps

PARAMETER MEASUREMENT INFORMATION



PIN	C_L
DDC, CEC (A side)	750 pF
DDC, CEC, HPD (B side)	15 pF



A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 19. Test Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision B (April 2012) to Revision C **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD12S015AYFFR	ACTIVE	DSBGA	YFF	28	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	PN015A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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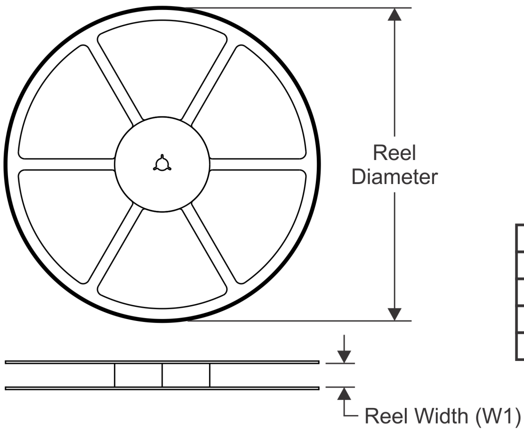
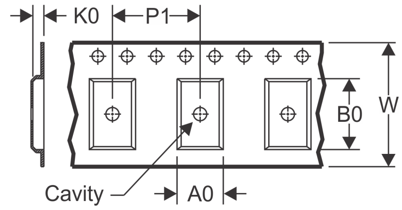
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

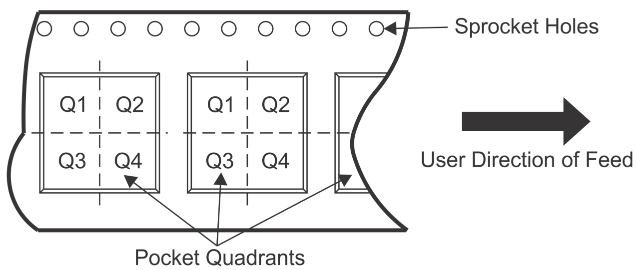


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

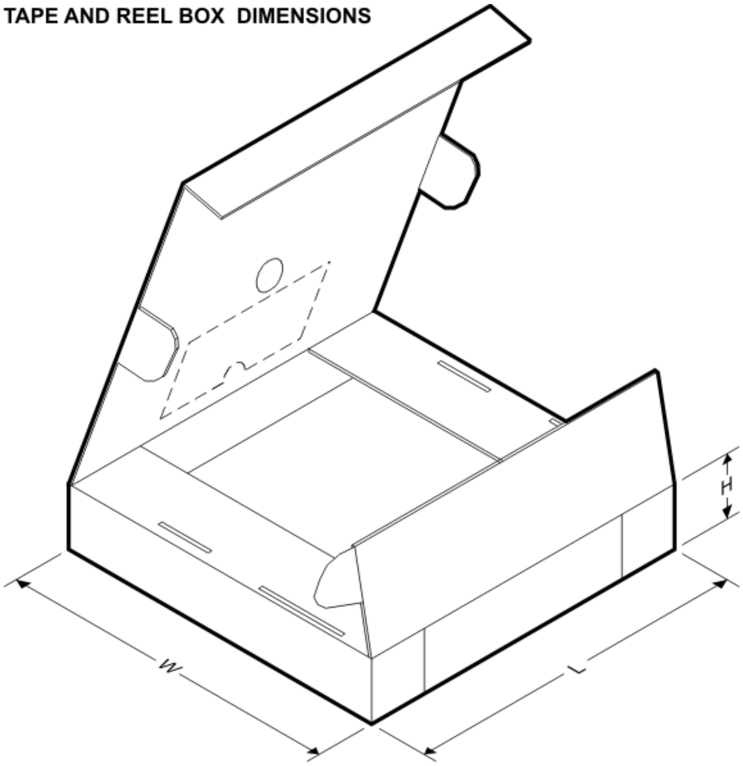
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S015AYFFR	DSBGA	YFF	28	3000	180.0	8.4	1.73	2.93	0.81	4.0	8.0	Q1

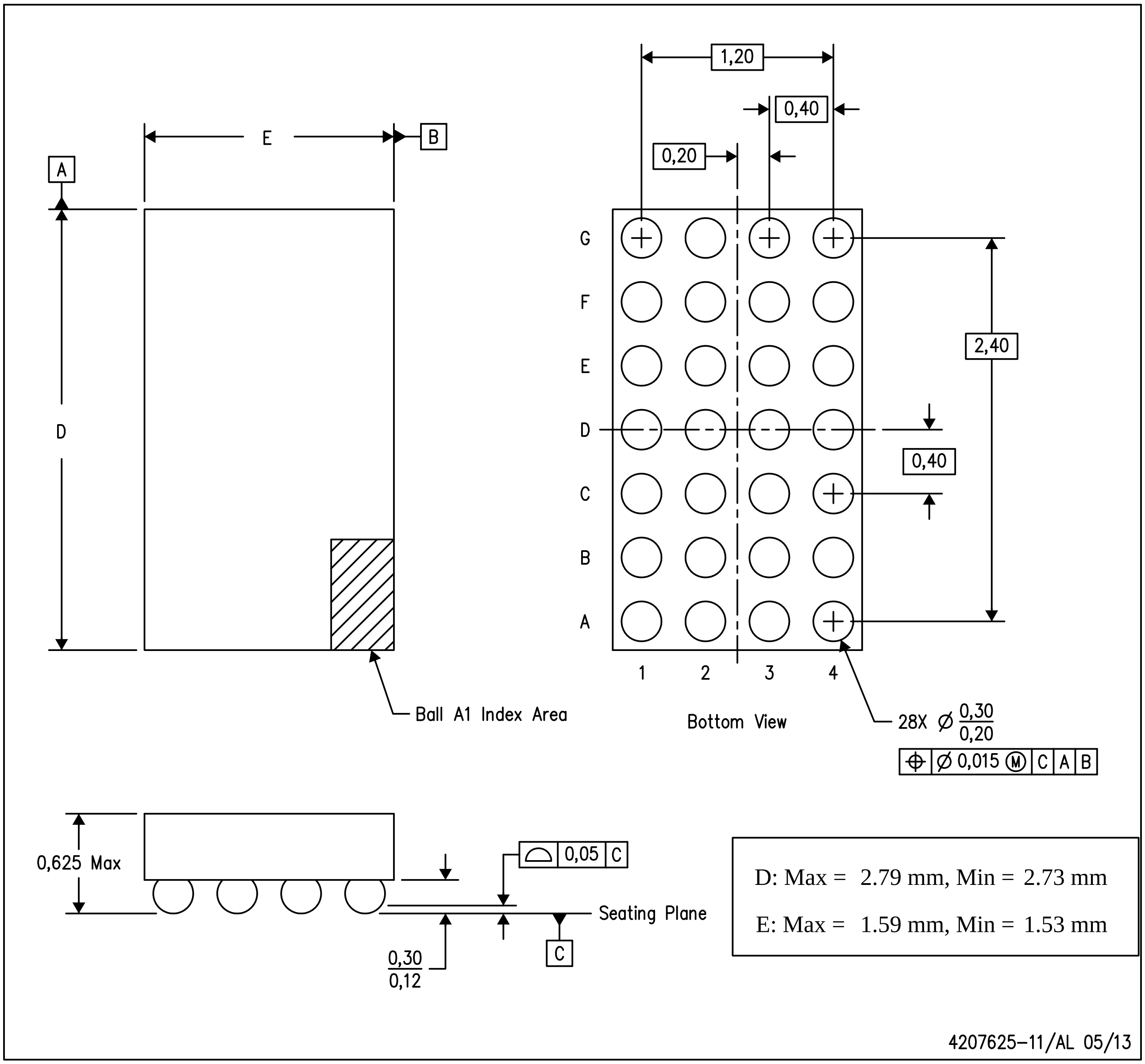
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S015AYFFR	DSBGA	YFF	28	3000	182.0	182.0	20.0

YFF (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



D: Max = 2.79 mm, Min = 2.73 mm

E: Max = 1.59 mm, Min = 1.53 mm

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.