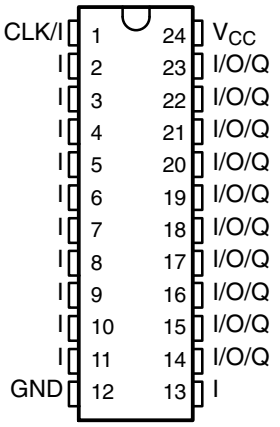
TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM
HIGH-PERFORMANCE *IMPACT* ™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

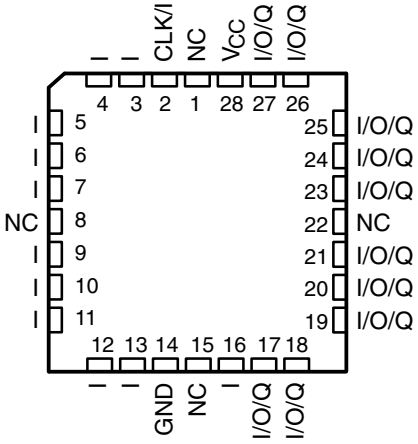
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010

- **Second-Generation PLD Architecture**
- **Choice of Operating Speeds**
  - **TIBPAL22V10AC . . . 25 ns Max**
  - **TIBPAL22V10AM . . . 30 ns Max**
  - **TIBPAL22V10C . . . 35 ns Max**
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Functionally Equivalent to AMDs AMPAL22V10 and AMPAL22V10A**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10 and TIBPAL22V10A are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept “Programmable Output Logic Macrocell”. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

description (continued)

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

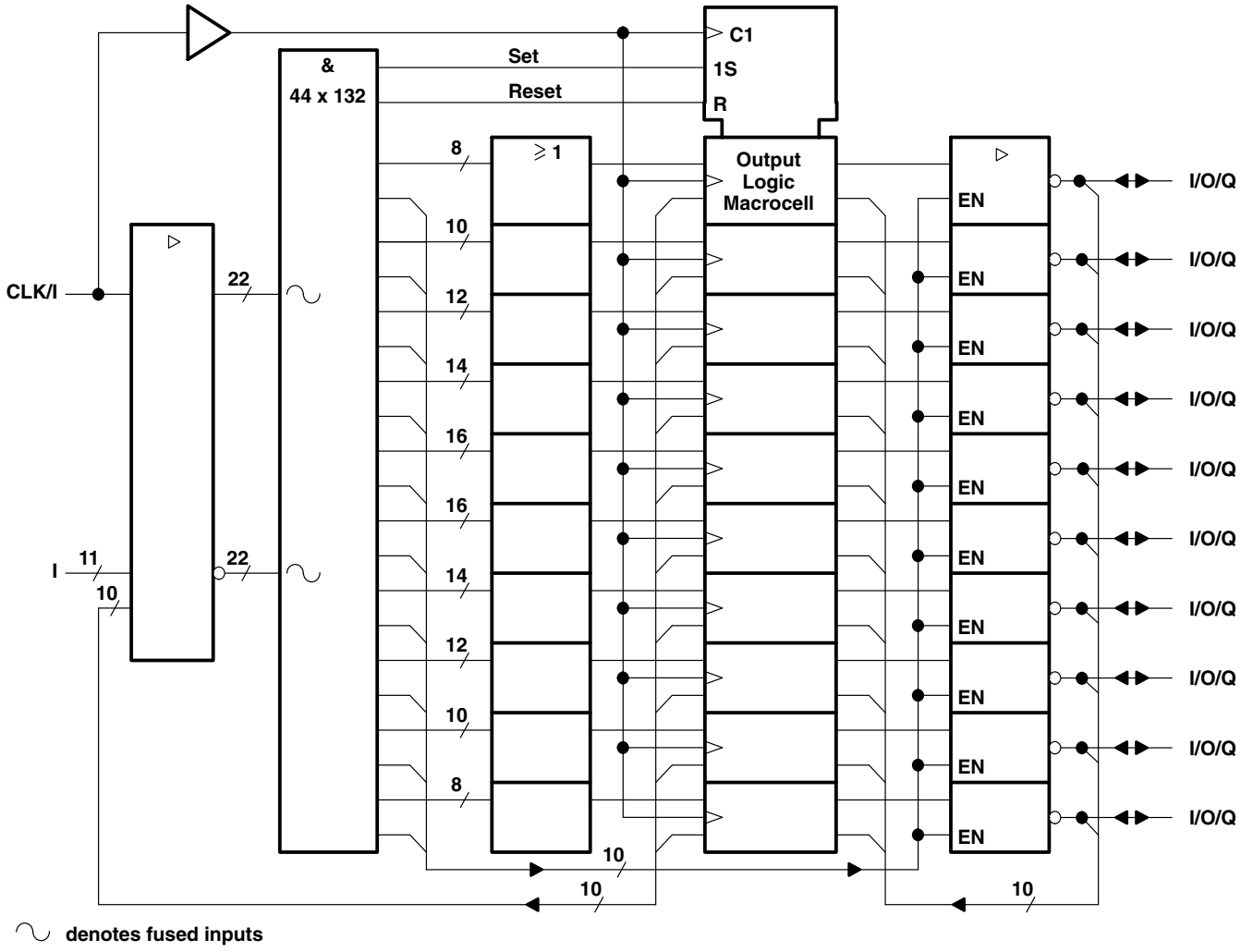
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10 and TIBPAL22V10A offer quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The TIBPAL22V10C and TIBPAL22V10AC are characterized for operation from 0°C to 75°C. The TIBPAL22V10AM is characterized for operation over the full military temperature range of –55°C to125°C.

functional block diagram (positive logic)



TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM
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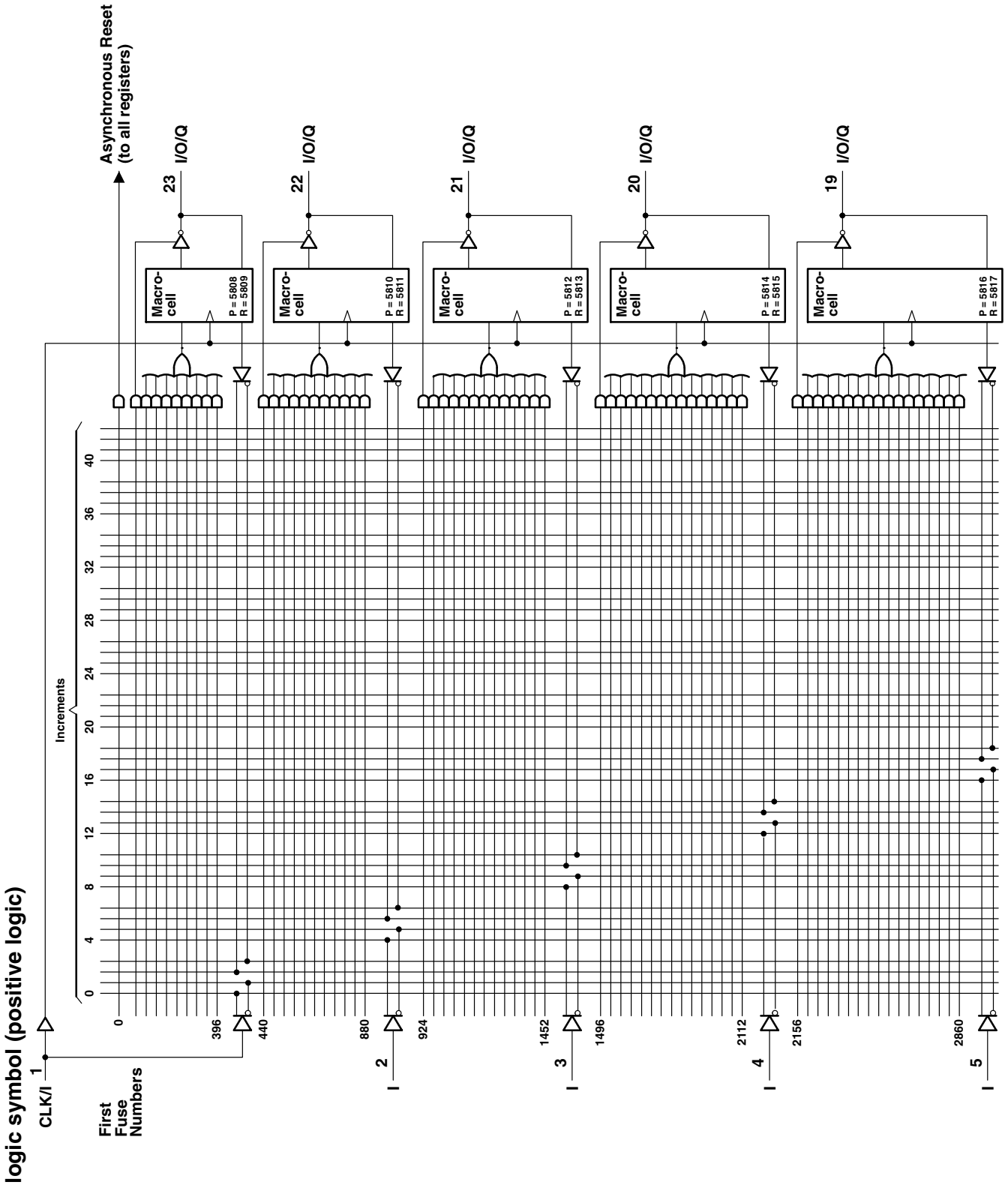
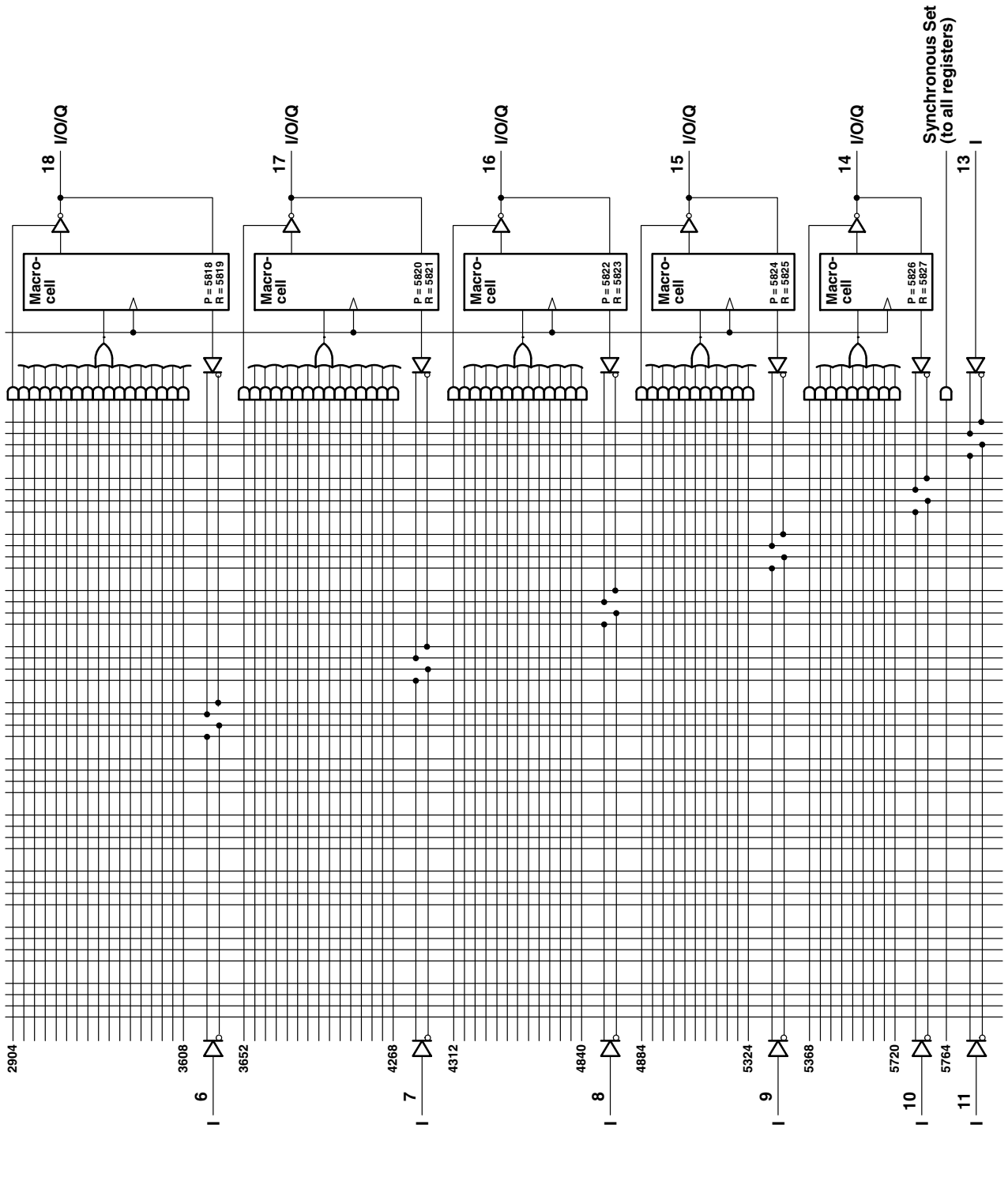
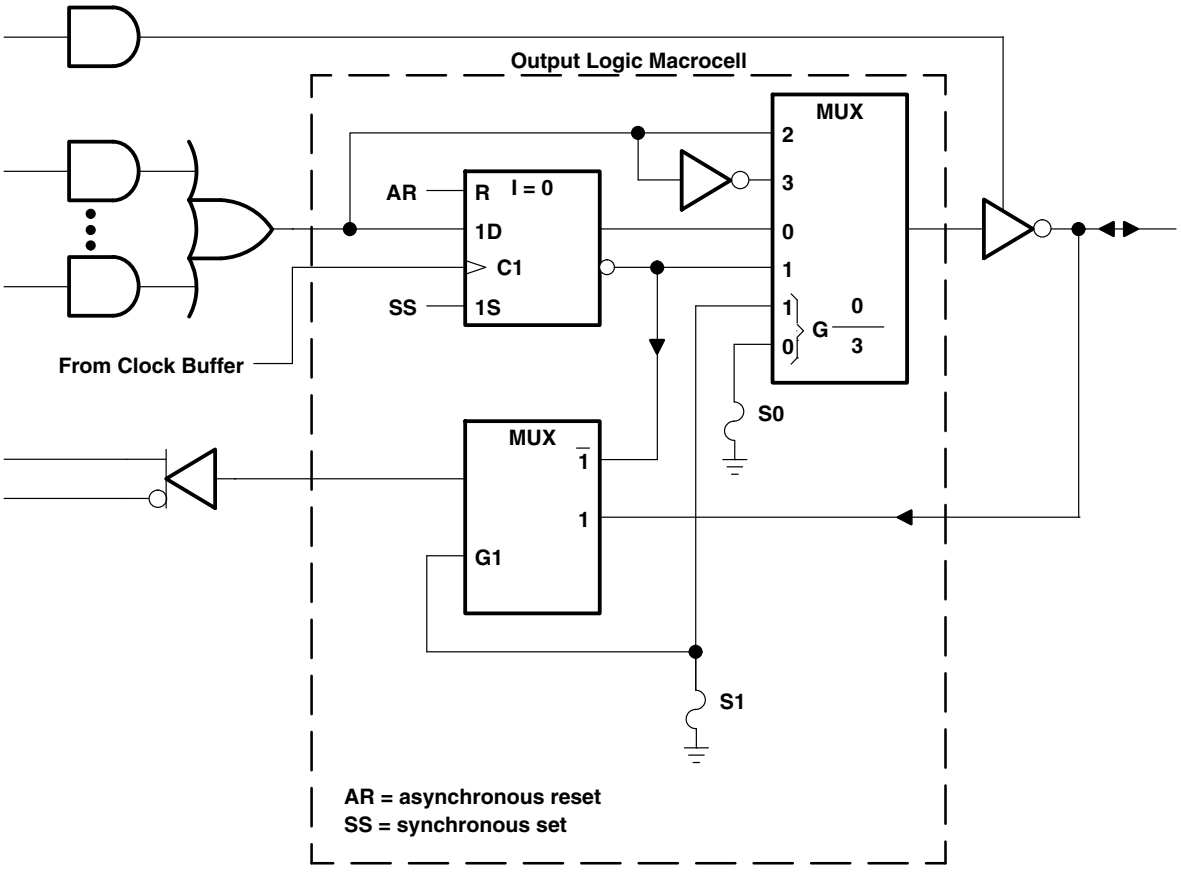
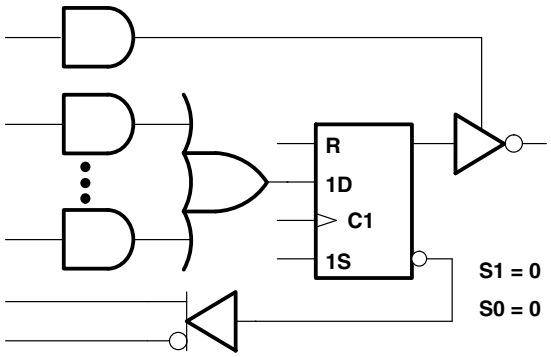
SRPS024A – OCTOBER 1986 – REVISED APRIL 2010



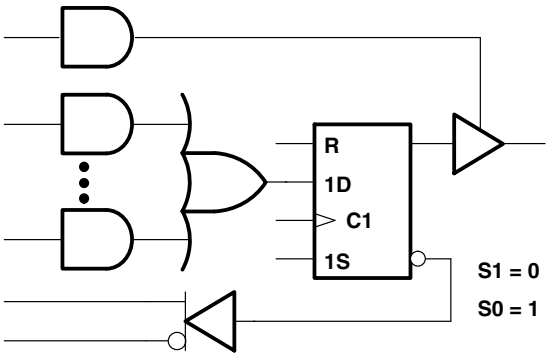

18 I/O/Q
17 I/O/Q
16 I/O/Q
15 I/O/Q
14 I/O/Q
Synchronous Set (to all registers)
13 I
Macro-cell
P = 5818 R = 5819
P = 5820 R = 5821
P = 5822 R = 5823
P = 5824 R = 5825
P = 5826 R = 5827
2904
3608
3652
4268
4312
4840
4884
5324
5368
5720
5764
6 I
7 I
8 I
9 I
10 I
11 I
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

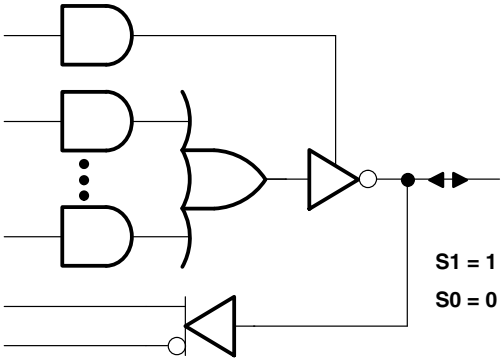




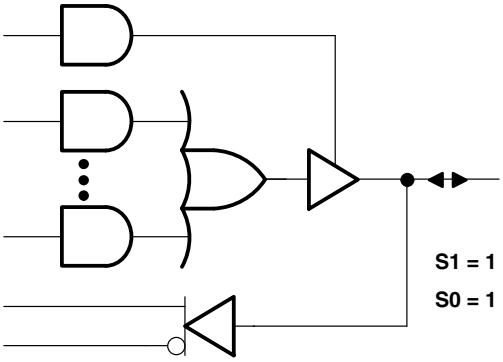
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . –5.5 V
Voltage range applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			TIBPAL22V10C			TIBPAL22V10AC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–3.2			–3.2	mA
I_{OL}	Low-level output current				16			16	mA
f_{clock}	Clock frequency†				18			28.5	MHz
t_w	Pulse duration	Clock high or low	25			15			ns
		Asynchronous reset high or low	35			25			
t_{su}	Setup time before clock↑	Input	30			20			ns
		Feedback	30			20			
		Synchronous set	30			25			
		Asynchronous reset low (inactive)	35			25			
t_h	Hold time, input, set, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

† f_{clock} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{clock} (without feedback) = $\frac{1}{t_w(\text{low}) + t_w(\text{high})}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			TIBPAL22V10C			TIBPAL22V10AC			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1			0.1	mA
I_{IL}	Any output	V_{CC} = 5.25 V,	V_I = 0.4 V				–100			–100	µA
	Any I/O						–250			–250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1			1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				25			25	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25			–0.25	mA
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–90	–30		–90	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open		120	180		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL22V10C			TIBPAL22V10AC			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	With feedback			18			28.5			MHz
t_{pd}	I, I/O	I/O	R1 = 300 Ω,		15	35		15	25	ns
t_{pd}	I, I/O (reset)	Q	R2 = 390 Ω,		15	40		15	30	ns
t_{pd}	CLK	Q	See Figure 4		10	25		10	15	ns
t_{en}	I, I/O	I/O, Q			15	35		15	25	ns
t_{dis}	I, I/O	I/O, Q			15	35		15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{max} (without feedback) = $\frac{1}{t_w(\text{low}) + t_w(\text{high})}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . –5.5 V
Voltage range applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency†				22	MHz
t_w	Pulse duration	Clock high or low	20			ns
		Asynchronous reset high or low	30			
t_{su}	Setup time before clock↑	Input	25			ns
		Feedback	25			
		Synchronous set	25			
		Asynchronous reset low (inactive)	30			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55		125	°C

† f_{clock} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{clock} (without feedback) = $\frac{1}{t_w(\text{low}) + t_w(\text{high})}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.5		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V				–100	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				25	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–90	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback			22			MHz
t_{pd}	I, I/O	I/O	R1 = 390 Ω,		15	30	ns
t_{pd}	I, I/O (reset)	Q	R2 = 750 Ω,		15	35	ns
t_{pd}	CLK	Q	See Figure 4		10	20	ns
t_{en}	I, I/O	I/O, Q			15	30	ns
t_{dis}	I, I/O	I/O, Q			15	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{max} (without feedback) = $\frac{1}{t_w(\text{low}) + t_w(\text{high})}$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

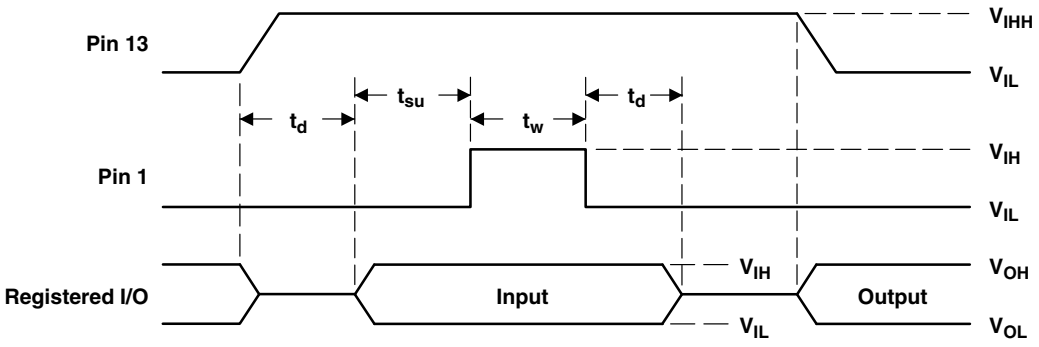
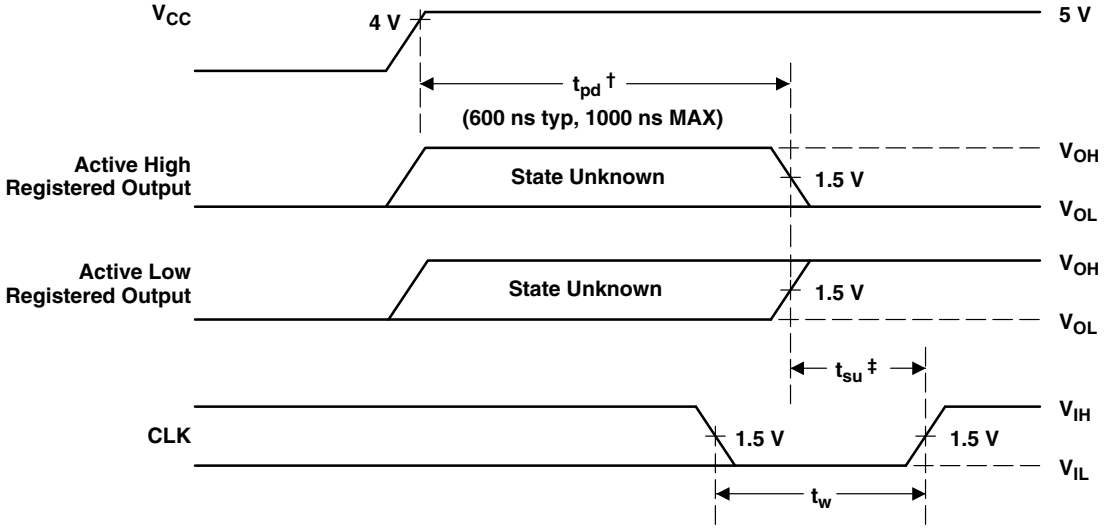


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w = 100$ ns to 1000 ns. $V_{IHH} = 10.25$ V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

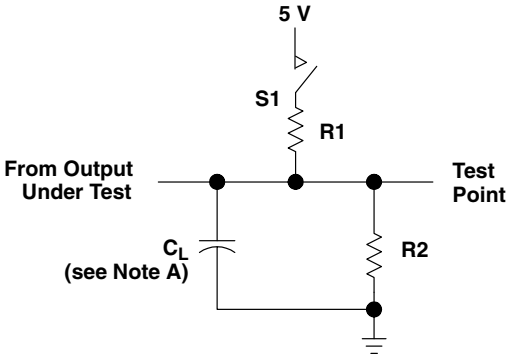
Figure 3. Power-Up Reset Waveforms

programming information

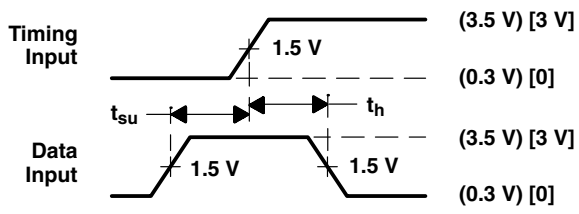
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

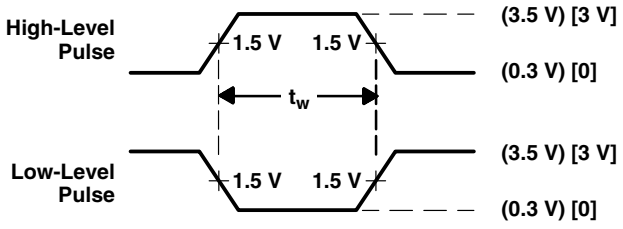
PARAMETER MEASUREMENT INFORMATION



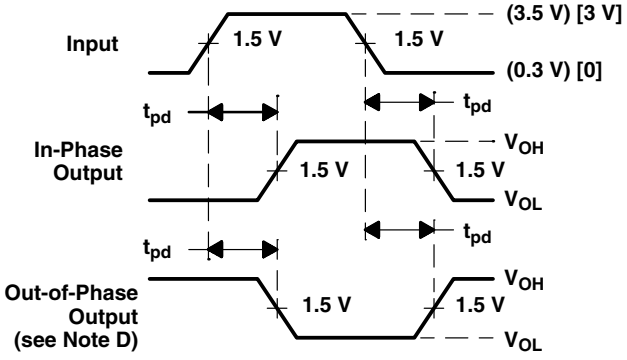
LOAD CIRCUIT FOR 3-STATE OUTPUTS



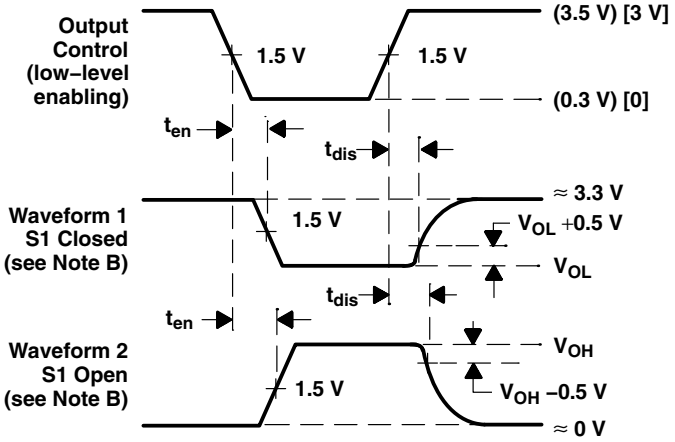
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86053013A	NRND	LCCC	FK	28	1	TBD	Call TI	Call TI	-55 to 125	5962-86053013A TIBPAL22V10AMFKB	
5962-8605301KA	NRND	CFP	W	24	1	TBD	Call TI	Call TI	-55 to 125	5962-8605301KA TIBPAL22V10AMWB	
5962-8605301LA	NRND	CDIP	JT	24	1	TBD	Call TI	Call TI	-55 to 125	5962-8605301LA TIBPAL22V10AMJTB	
TIBPAL22V10ACFN	LIFEBUY	PLCC	FN	28	37	TBD	CU SN	Level-1-220C-UNLIM	0 to 75	22V10ACFN	
TIBPAL22V10ACNT	LIFEBUY	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL22V10ACNT	
TIBPAL22V10AMFKB	NRND	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-86053013A TIBPAL22V10AMFKB	
TIBPAL22V10AMJT	NRND	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL22V10AMJT	
TIBPAL22V10AMJTB	NRND	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8605301LA TIBPAL22V10AMJTB	
TIBPAL22V10AMWB	NRND	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8605301KA TIBPAL22V10AMWB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

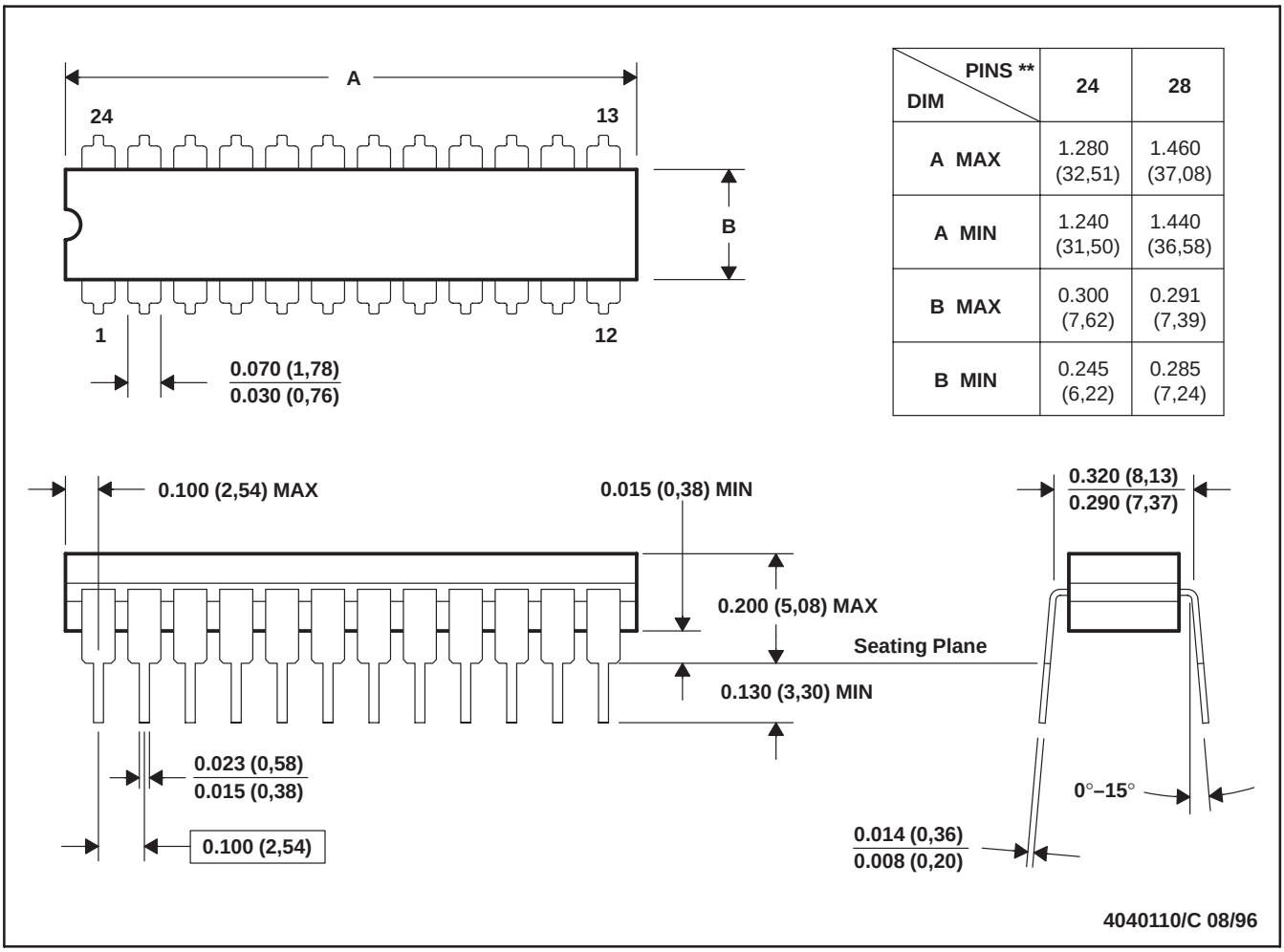
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

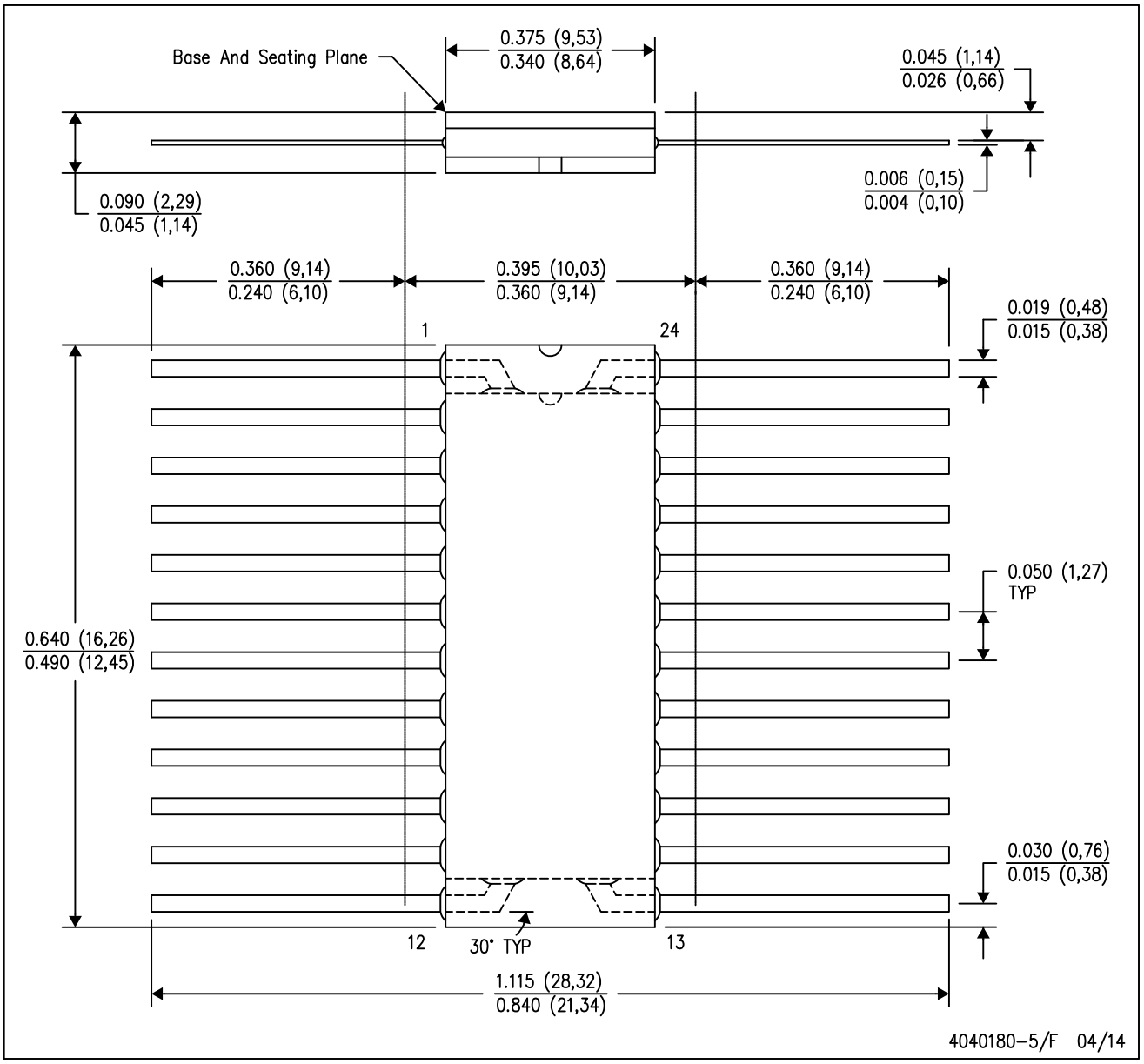
24 LEADS SHOWN



DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

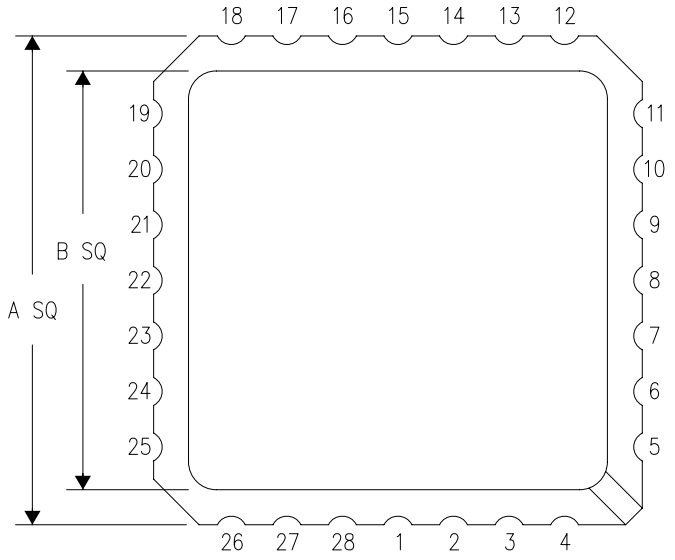
W (R–GDFP–F24) CERAMIC DUAL FLATPACK



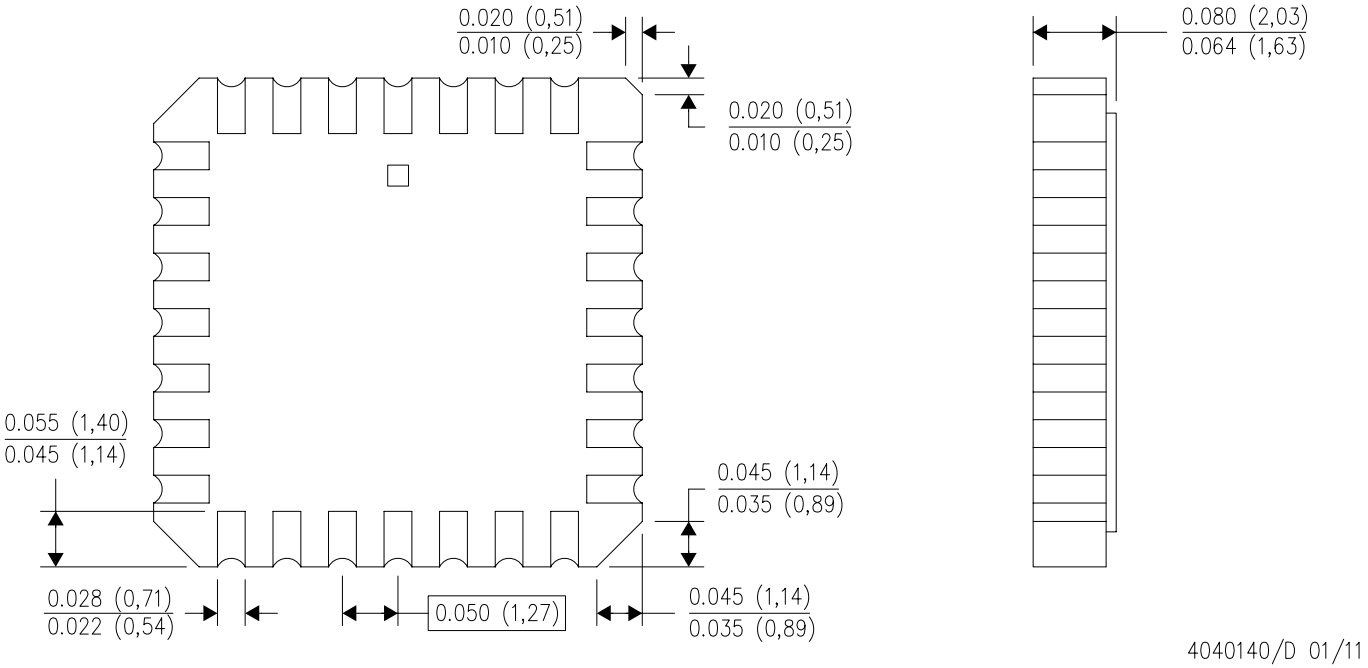
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

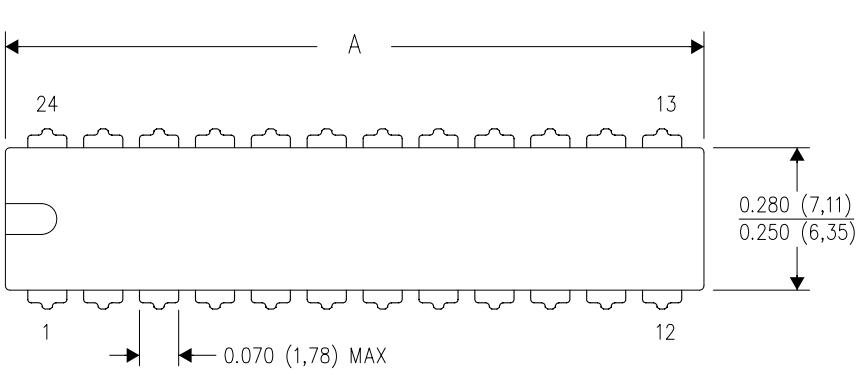


4040140/D 01/11

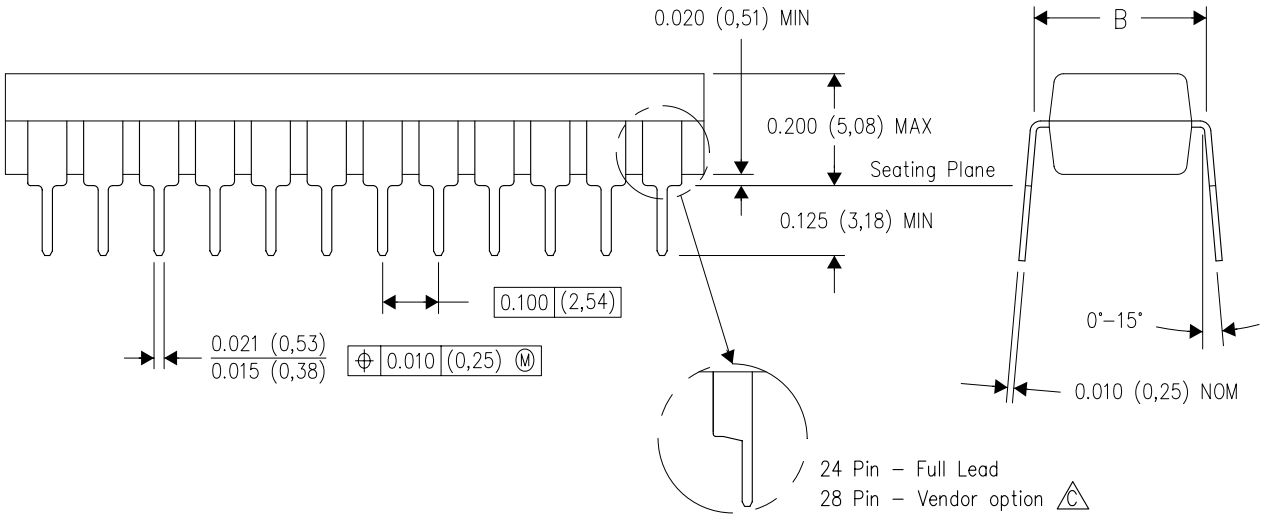
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

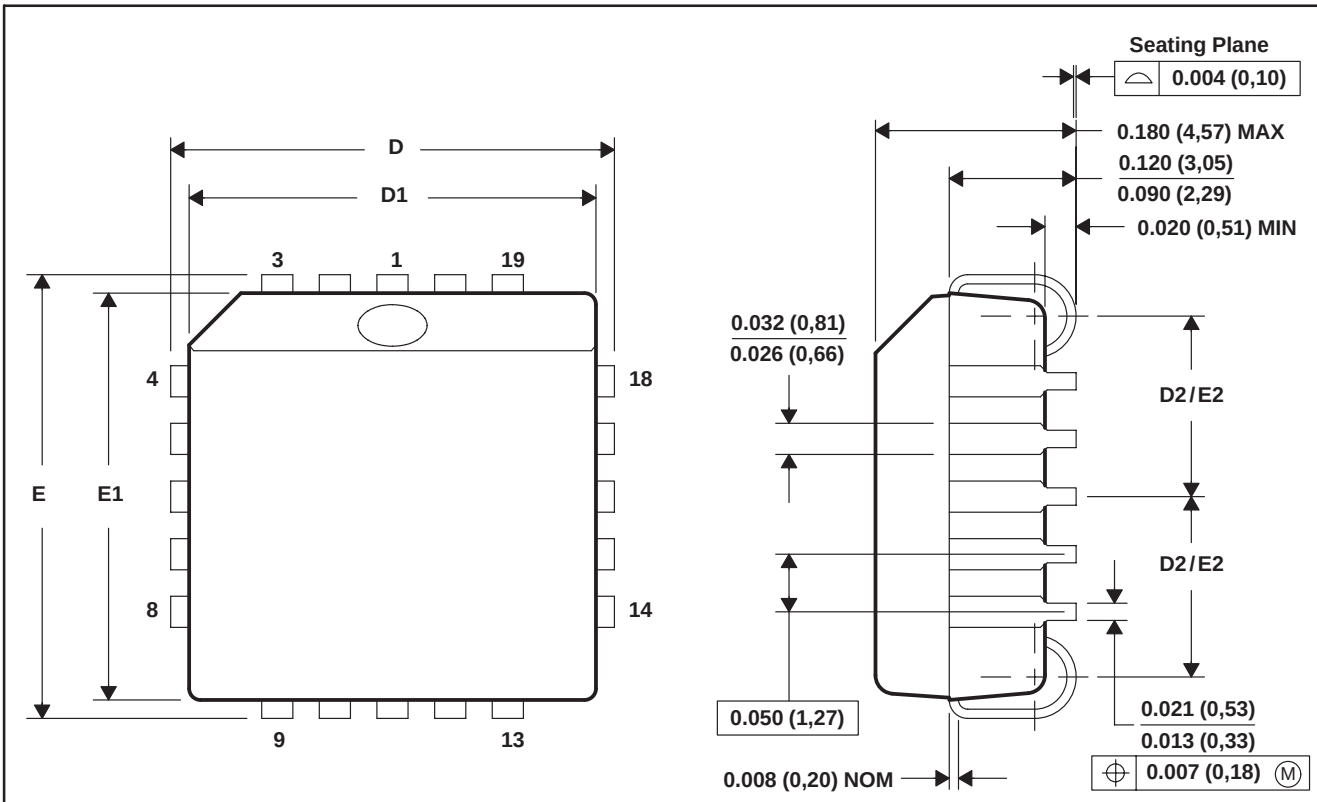
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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