



March 2015



FDD8778/FDU8778 N-Channel PowerTrench[®] MOSFET 25V, 35A, 14mΩ

Features

- Max $r_{DS(on)}$ = 14.0mΩ at $V_{GS} = 10V$, $I_D = 35A$
- Max $r_{DS(on)}$ = 21.0mΩ at $V_{GS} = 4.5V$, $I_D = 33A$
- Low gate charge: $Q_{g(TOT)} = 12.6nC(Typ)$, $V_{GS} = 10V$
- Low gate resistance
- RoHS compliant

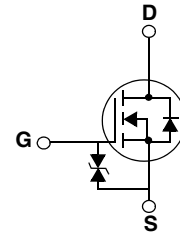
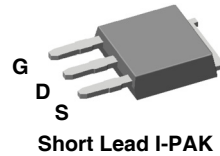
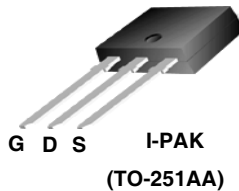
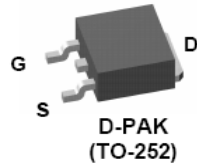


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

Application

- DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package Limited)	35	A
	-Continuous (Die Limited)	40	
	-Pulsed (Note 1)	145	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	24	mJ
P_D	Power Dissipation	39	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case TO-252, TO-251	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, TO-251	100	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient TO-252, 1in ² copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8778	FDD8778	TO-252AA	13"	16mm	2500 units
FDU8778	FDU8778	TO-251AA	N/A(Tube)	N/A	75 units
FDU8778	FDU8778_F071	TO-251AA	N/A(Tube)	N/A	75 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		17.2		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$			1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.5	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-5.3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 35\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 33\text{A}$ $V_{GS} = 10\text{V}, I_D = 35\text{A}$ $T_J = 175^\circ\text{C}$		11.6 15.7 18.2	14.0 21.0 23.8	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 13\text{V}, V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		635	845	pF
C_{oss}	Output Capacitance			160	215	pF
C_{rss}	Reverse Transfer Capacitance			108	162	pF
R_g	Gate Resistance		$f = 1\text{MHz}$		1.3	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{V}, I_D = 35\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 27\Omega$		6	12	ns
t_r	Rise Time			22	35	ns
$t_{d(off)}$	Turn-Off Delay Time			43	69	ns
t_f	Fall Time			32	51	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V		$V_{GS} = 0\text{V}$ to 10V		12.6	18
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	$V_{DD} = 13\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	6.7	9.4	nC
Q_{gs}	Gate to Source Gate Charge			2.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.2		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 35\text{A}$ $V_{GS} = 0\text{V}, I_S = 15\text{A}$		1.03 0.89	1.25 1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 35\text{A}, di/dt = 100\text{A}/\mu\text{s}$		25	38	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 35\text{A}, di/dt = 100\text{A}/\mu\text{s}$		17	26	nC

Notes:

- 1: Pulse time < 300 μs , Duty cycle = 2%.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.1\text{mH}$, $I_{AS} = 22\text{A}$, $V_{DD} = 23\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

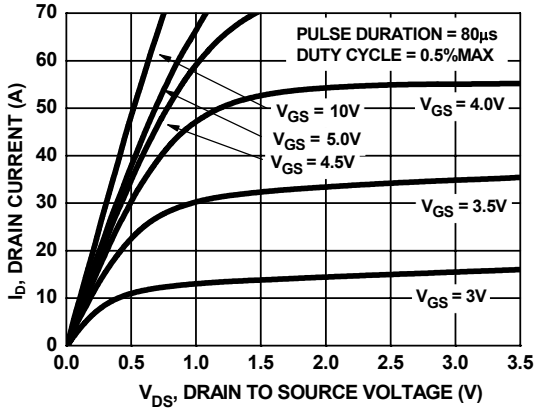


Figure 1. On Region Characteristics

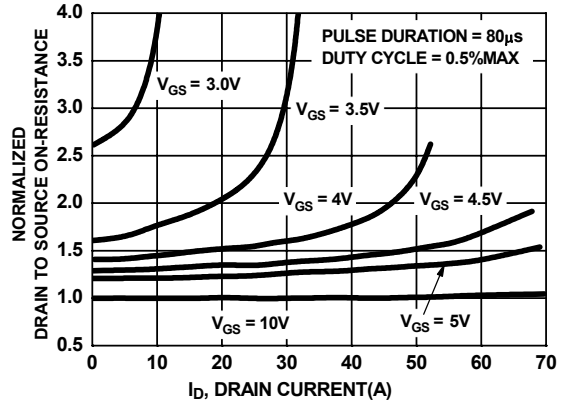


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

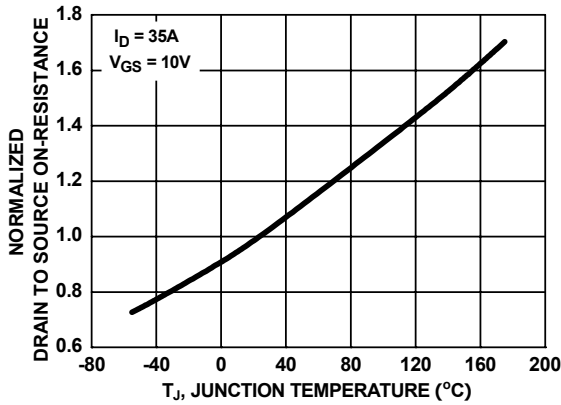


Figure 3. Normalized On Resistance vs Junction Temperature

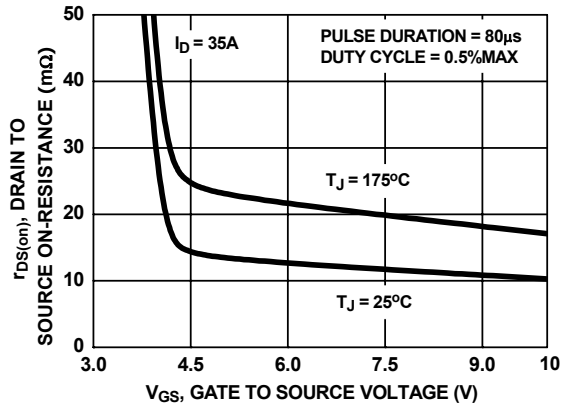


Figure 4. On-Resistance vs Gate to Source Voltage

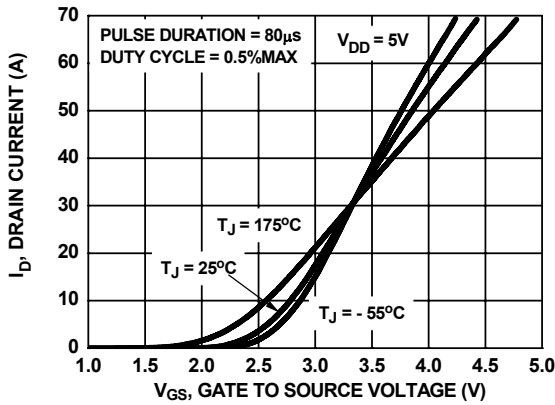


Figure 5. Transfer Characteristics

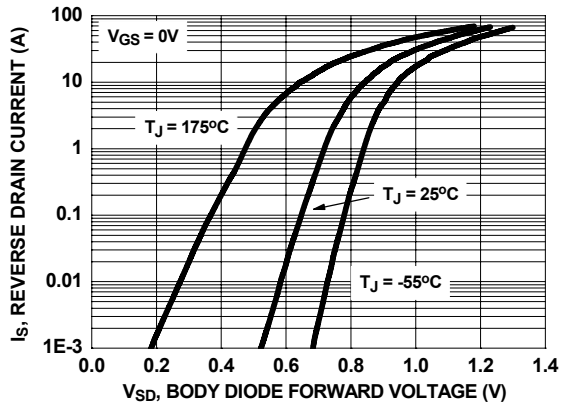


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

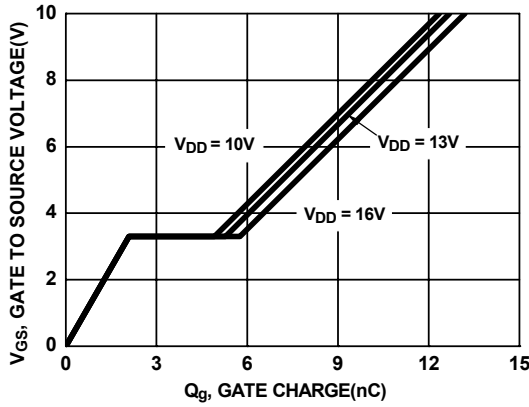


Figure 7. Gate Charge Characteristics

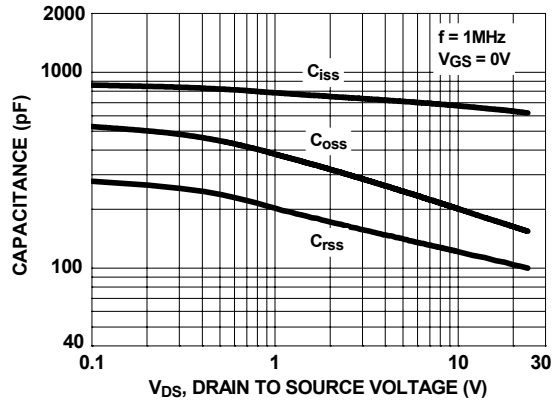


Figure 8. Capacitance vs Drain to Source Voltage

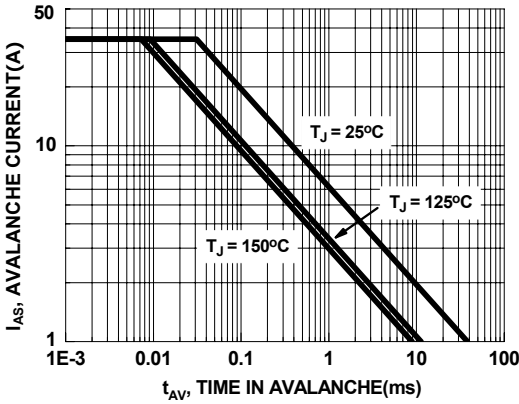


Figure 9. Unclamped Inductive Switching Capability

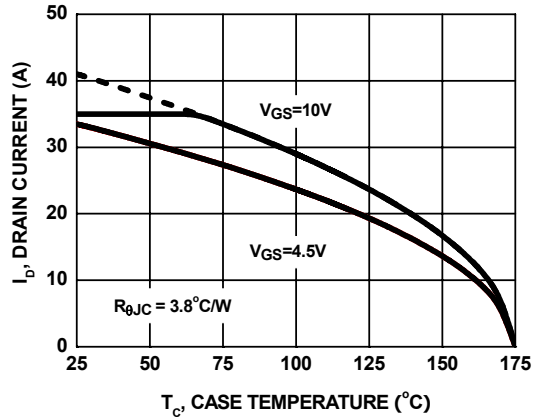


Figure 10. Maximum Continuous Drain Current vs Case Temperature

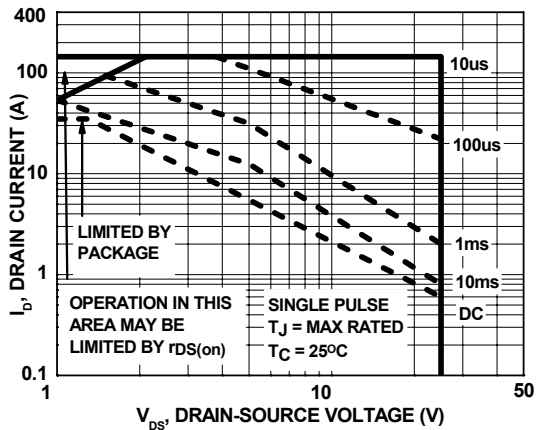


Figure 11. Forward Bias Safe Operating Area

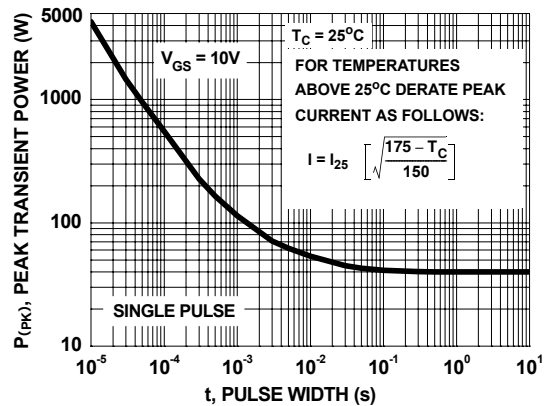


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

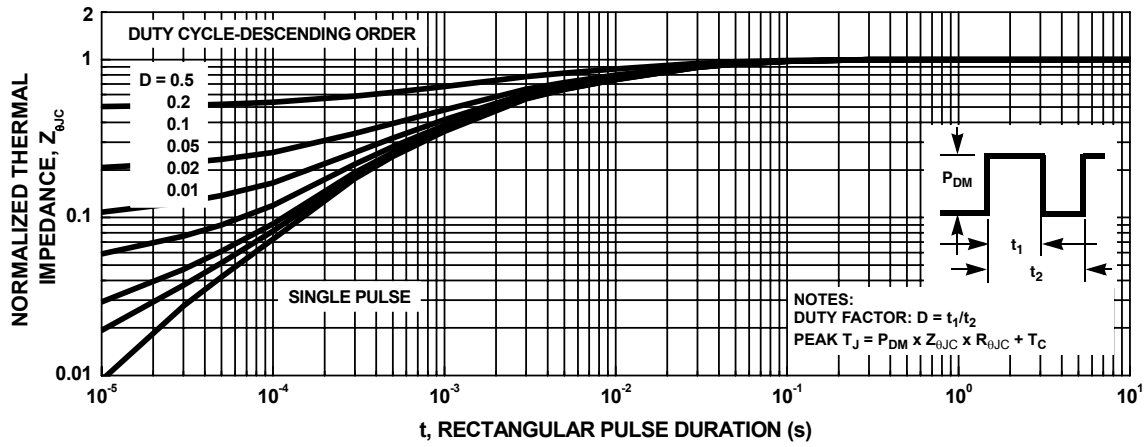
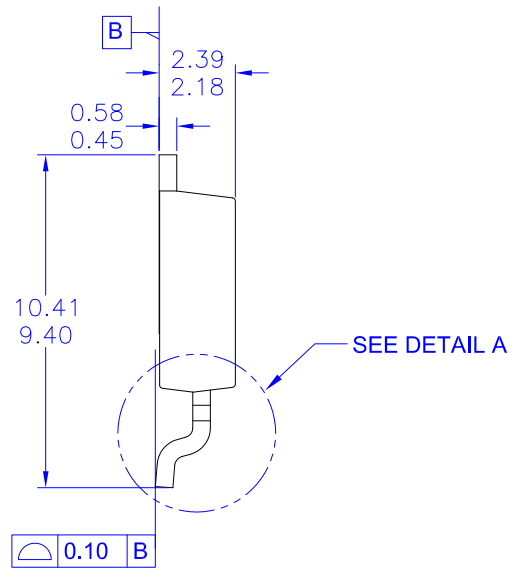
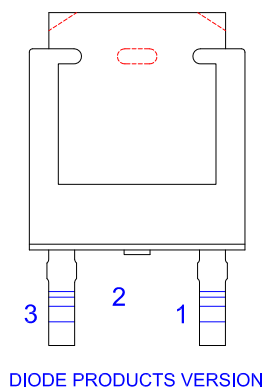
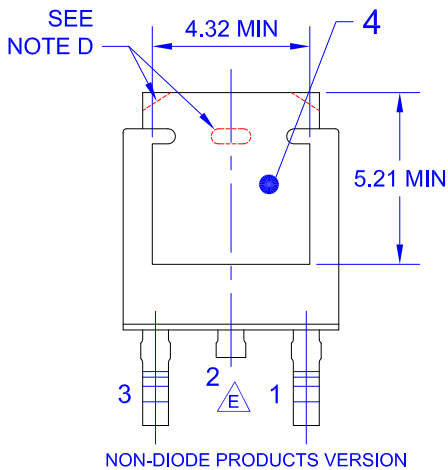
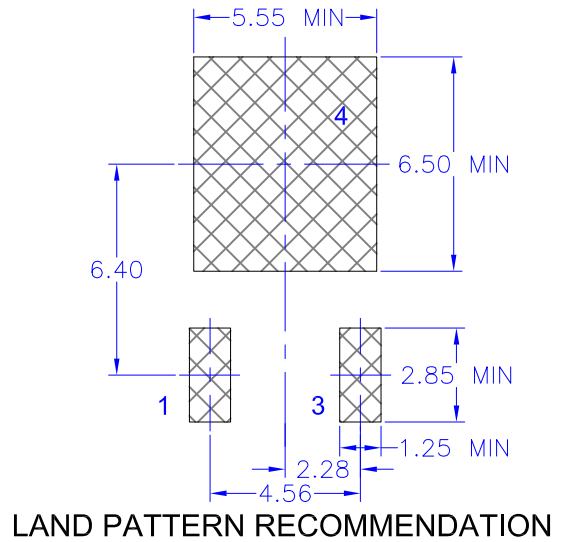
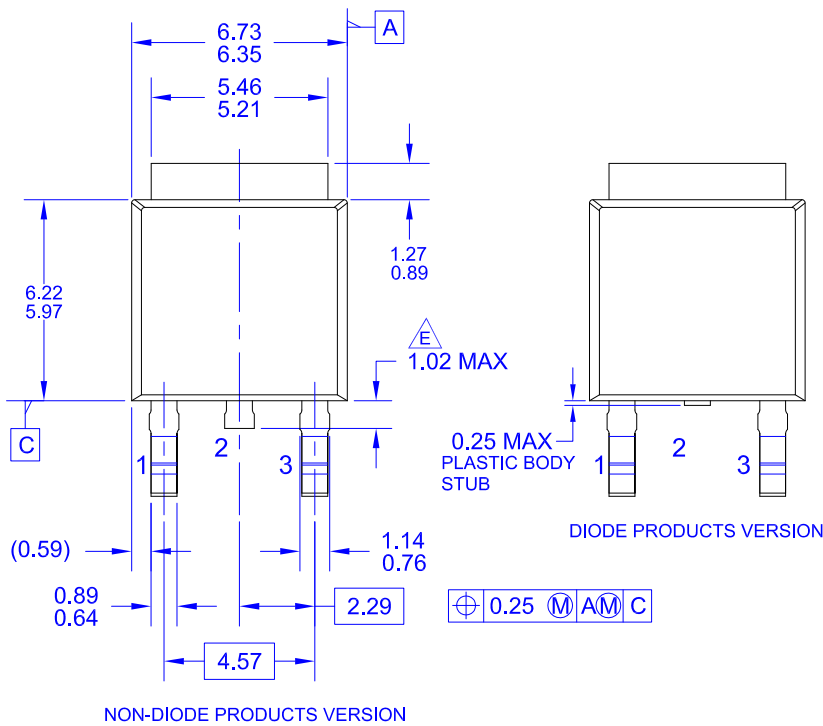
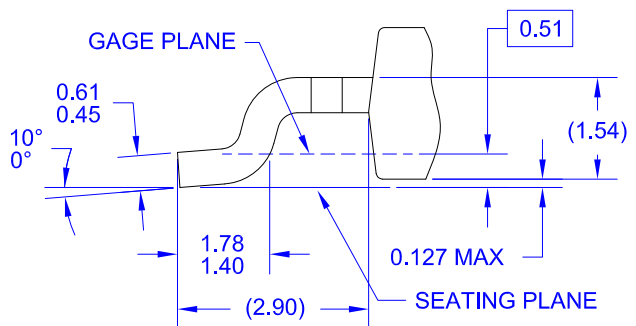


Figure 13. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



DETAIL A
(ROTATED -90°)
SCALE: 12X





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I76