

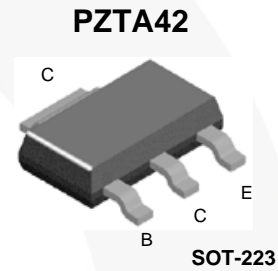
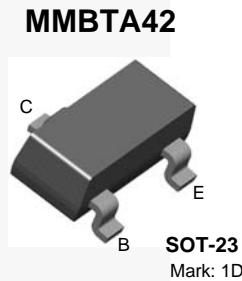
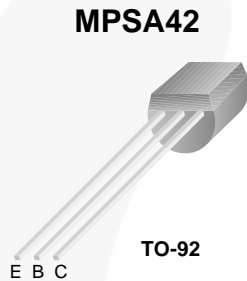


October 2014

# MPSA42 / MMBTA42 / PZTA42 NPN High-Voltage Amplifier

## Features

- This device is designed for application as a video output and other high-voltage applications.
- Sourced from process 48.



## Ordering Information

Part Number	Top Mark	Package	Packing Method
MPSA42	MPSA42	TO-92 3L	Bulk
MMBTA42	1D	SOT-23 3L	Tape and Reel
PZTA42	A42	SOT-223 4L	Tape and Reel

## Absolute Maximum Ratings<sup>(1), (2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CEO}$	Collector-Emitter Voltage	300	V
$V_{CBO}$	Collector-Base Voltage	300	V
$V_{EBO}$	Emitter-Base Voltage	6	V
$I_C$	Collector Current - Continuous	500	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.			Unit
		MPSA42	MMBTA42 <sup>(3)</sup>	PZTA42 <sup>(4)</sup>	
$P_D$	Total Device Dissipation	625	240	1000	mW
	Derate Above $25^\circ\text{C}$	5.00	1.92	8.00	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	515	125	$^\circ\text{C}/\text{W}$

### Notes:

- Device is mounted on FR-4 PCB 1.6 inch x 1.6 inch x 0.06 inch.
- Device is mounted on FR-4 PCB 36 mm x 18 mm x 1.5 mm, mounting pad for the collector lead minimum 6 cm<sup>2</sup>.

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>Off Characteristics</b>					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage <sup>(5)</sup>	$I_C = 1.0\text{ mA}, I_B = 0$	300		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100\text{ }\mu\text{A}, I_E = 0$	300		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100\text{ }\mu\text{A}, I_C = 0$	6		V
$I_{CBO}$	Collector Cut-Off Current	$V_{CB} = 200\text{ V}, I_E = 0$		0.1	$\mu\text{A}$
$I_{EBO}$	Emitter Cut-Off Current	$V_{EB} = 6\text{ V}, I_C = 0$		0.1	$\mu\text{A}$
<b>On Characteristics<sup>(5)</sup></b>					
$h_{FE}$	DC Current Gain	$V_{CE} = 10\text{ V}, I_C = 1.0\text{ mA}$	25		
		$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$	40		
		$V_{CE} = 10\text{ V}, I_C = 30\text{ mA}$	40		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 20\text{ mA}, I_B = 2.0\text{ mA}$		0.5	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 20\text{ mA}, I_B = 2.0\text{ mA}$		0.9	V
<b>Small Signal Characteristics</b>					
$f_T$	Current Gain - Bandwidth Product	$I_C = 10\text{ mA}, V_{CE} = 20\text{ V},$ $f = 100\text{ MHz}$	50		MHz
$C_{cb}$	Collector-Base Capacitance	$V_{CB} = 20\text{ V}, I_E = 0,$ $f = 1.0\text{ MHz}$		3.0	pF

### Notes:

- Pulse test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

## Typical Performance Characteristics

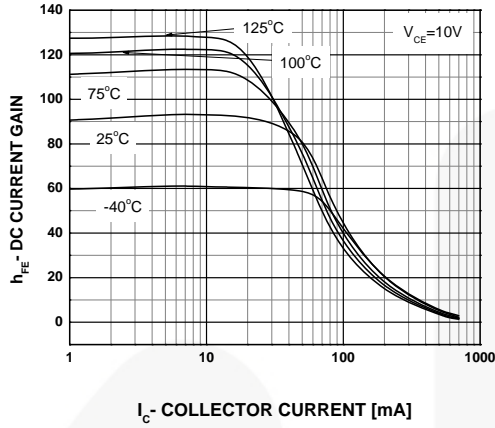


Figure 1. DC Current Gain vs. Collector Current

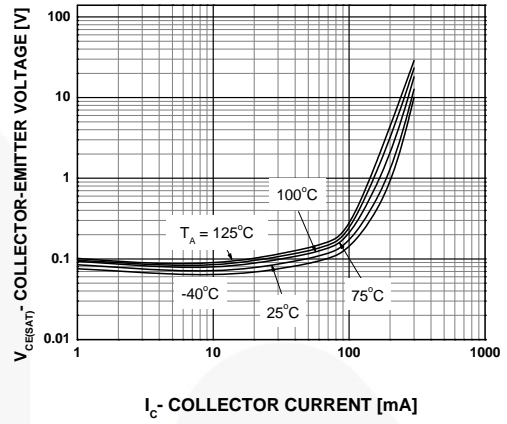


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

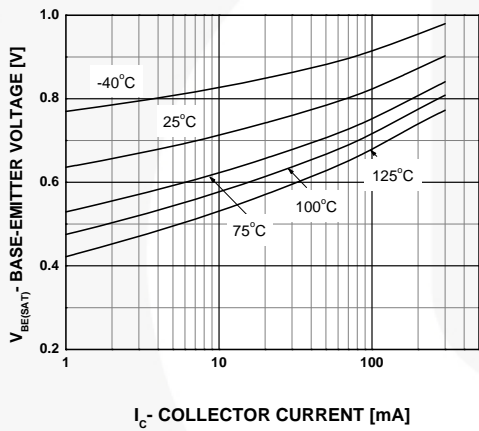


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

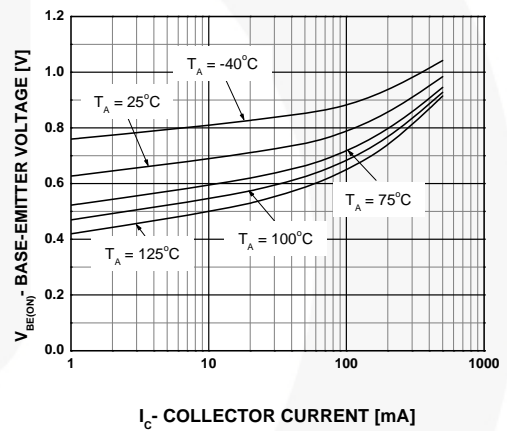


Figure 4. Base-Emitter On Voltage vs. Collector Current

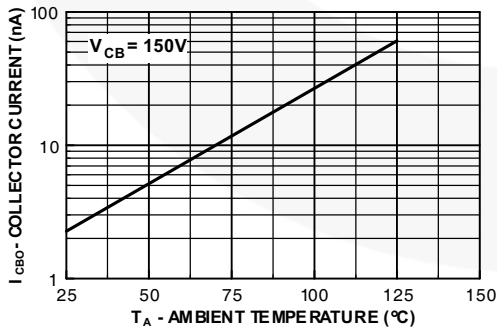


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

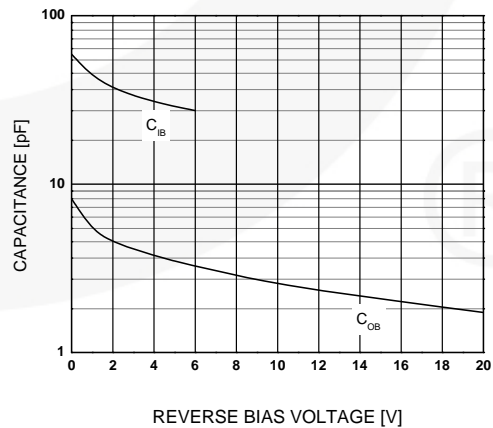


Figure 6. Collector-Base and Emitter-Base Capacitance vs. Reverse-Bias Voltage

### Typical Performance Characteristics (Continued)

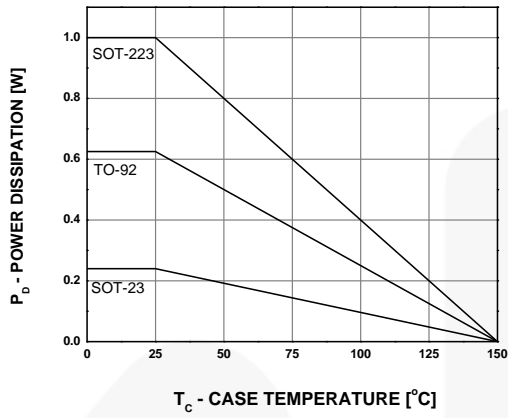
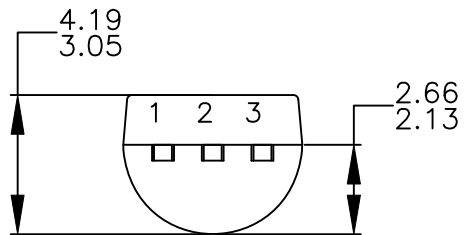
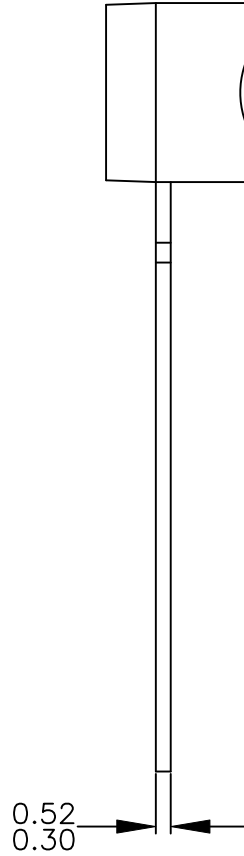
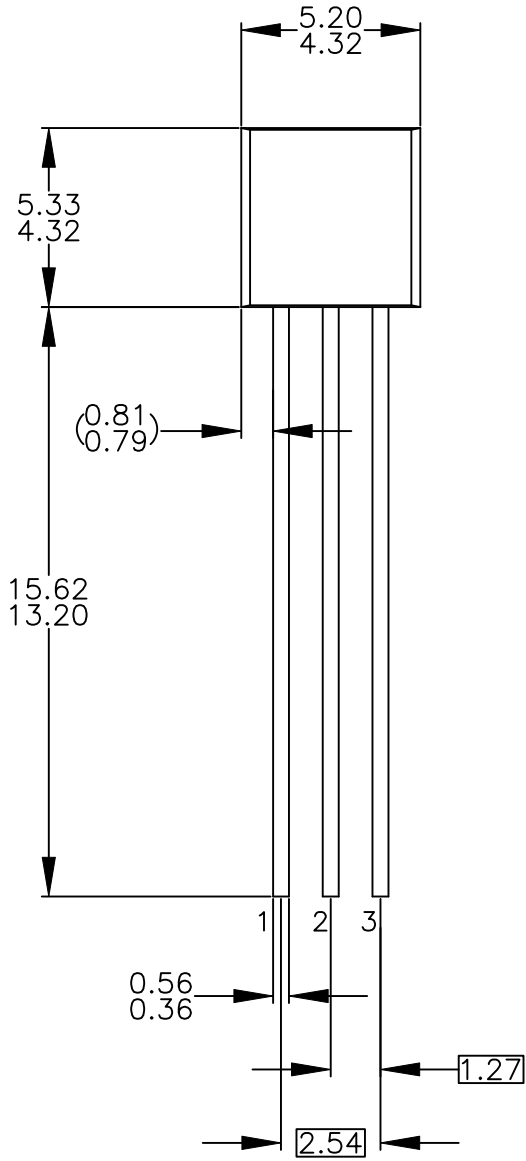


Figure 7. Power Dissipation vs. Ambient Temperature





NOTES: UNLESS OTHERWISE SPECIFIED

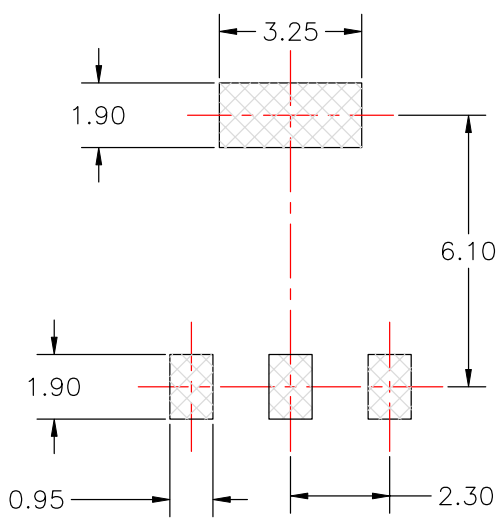
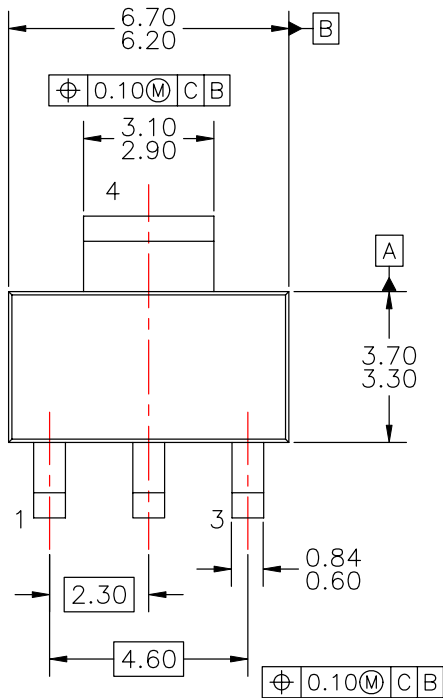
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-2009.
- D) DRAWING FILENAME: MKT-ZA03DREV4.



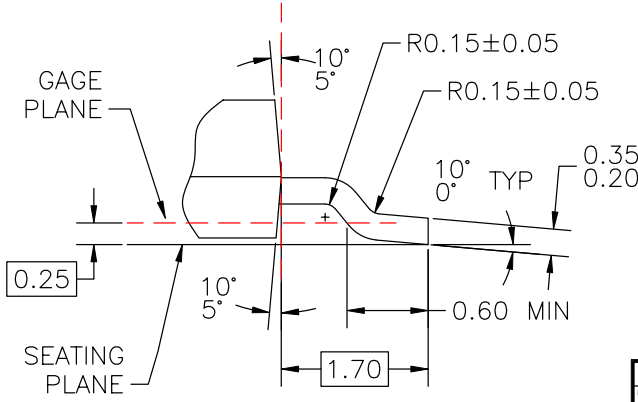
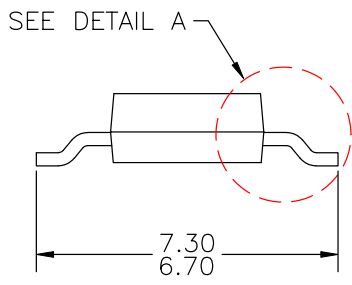
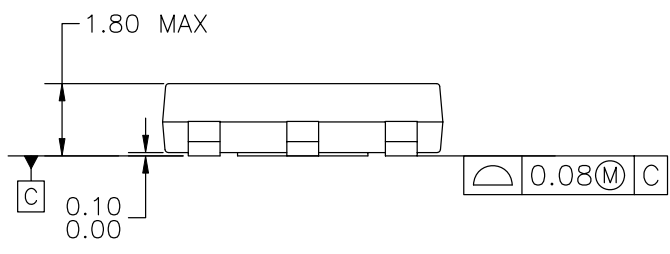
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**APPROVED**  
July-14-2008

REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 <del>±0.03</del> TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 <del>±0.05</del> TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 <del>±0.03</del> TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 <del>±0.33</del> TO 3.30; CHG BODY LN FR 6.53 <del>±0.33</del> TO 6.30; CHG TOTAL PKG WID FR 6.94 <del>±0.33</del> TO 7.30; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



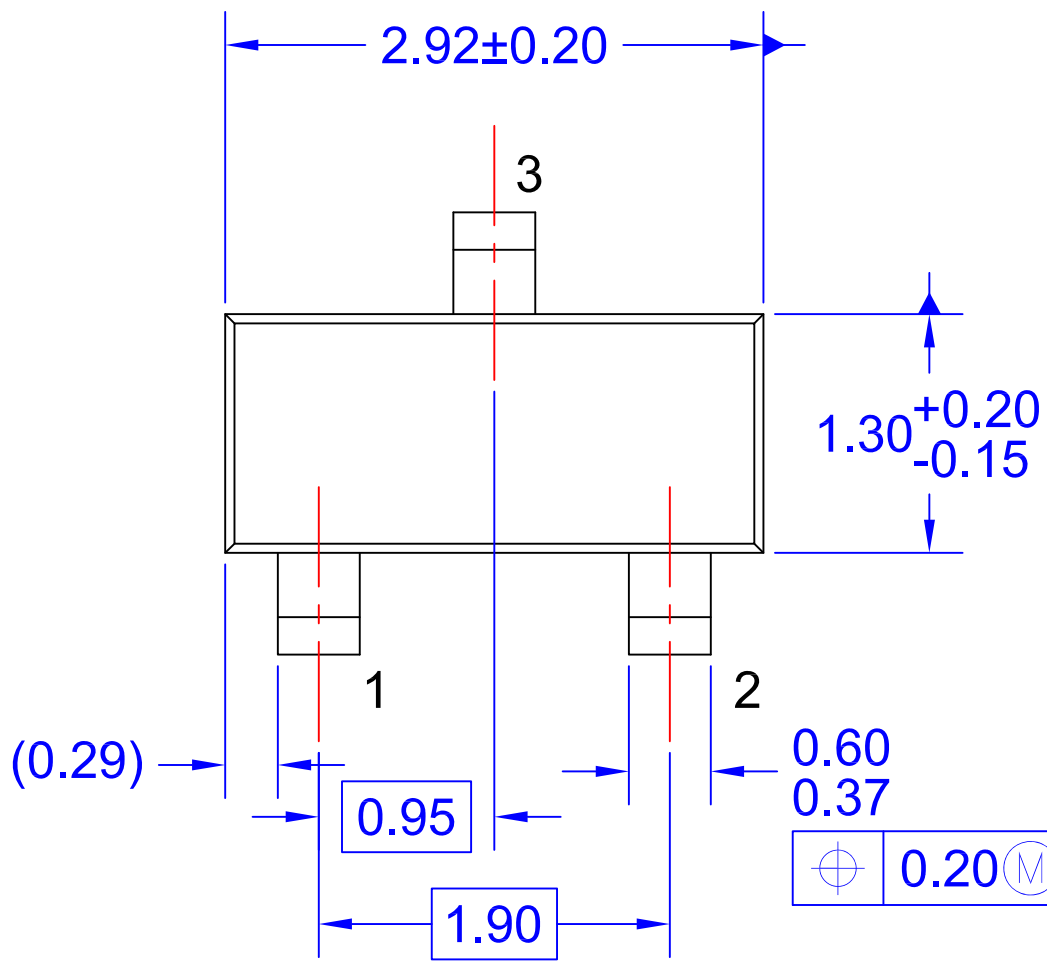
LAND PATTERN RECOMMENDATION



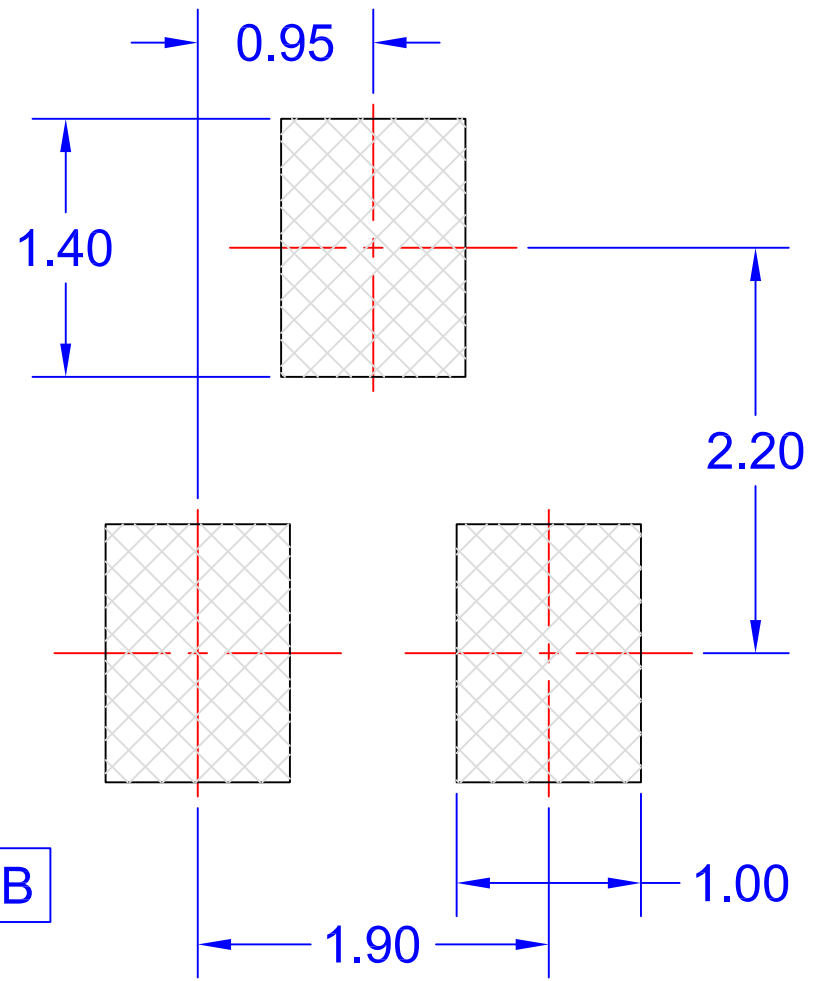
DETAIL A  
SCALE: 2:1

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
  - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - C) ALL DIMENSIONS ARE IN MILLIMETERS.
  - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
  - E) LANDPATTERN NAME: SOT230P700X180-4BN
  - F) DRAWING FILENAME: MKT-MA04AREV2

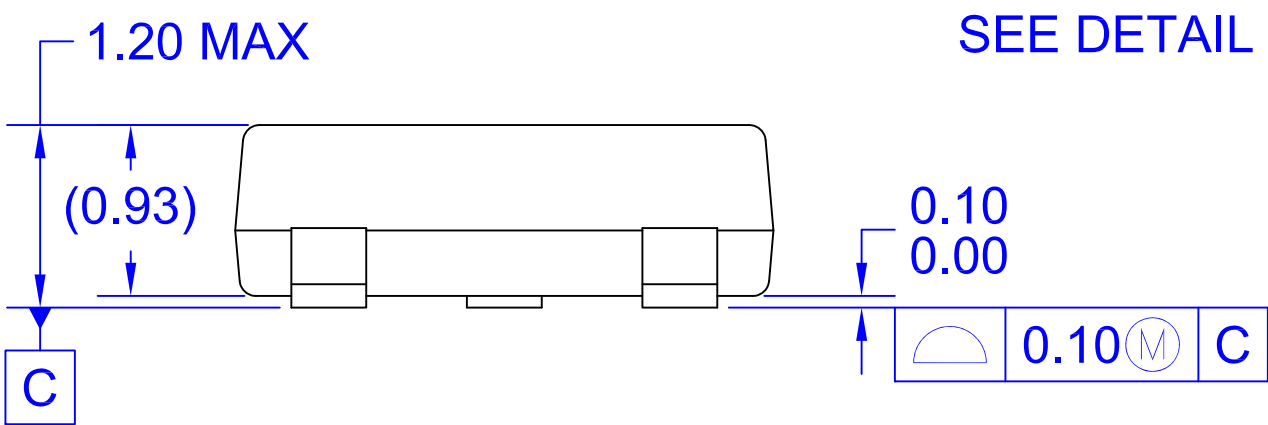
APPROVALS	DATE	<b>FAIRCHILD</b> SEMICONDUCTOR™
DRWN: J.U. COMPARATIVO JR.	26FEB2008	
CHECKED: L.Z. STA CRUZ		
APPROVED: M.R. GESTOLE		
G.S. BAJE		<b>MOLDED PACKAGE</b> <b>SOT-223, 4 LEAD</b>
		SCALE: 1:1
		SIZE: A3
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		REV: 2
		FORMERLY: N/A
		SHEET: 1 OF 1



⊕ 0.20 (M) A B

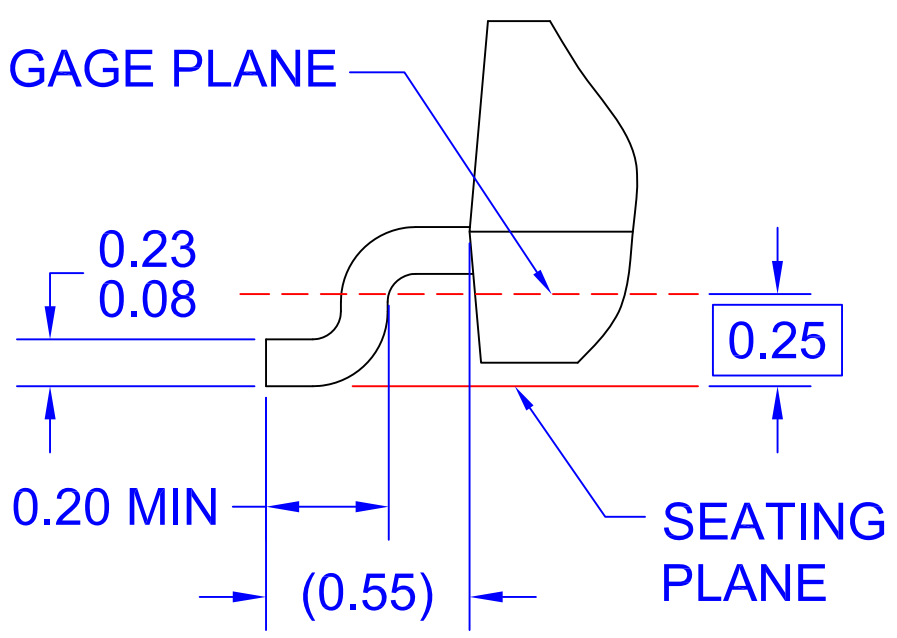
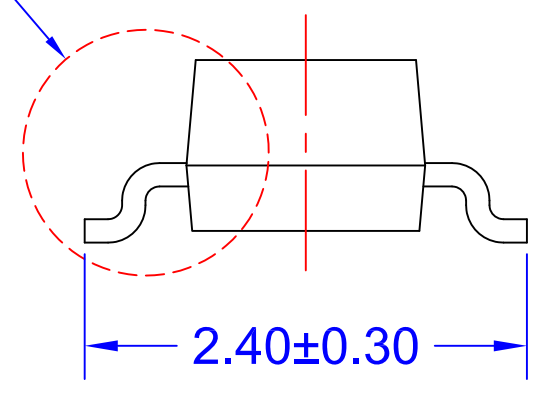


LAND PATTERN RECOMMENDATION



⌒ 0.10 (M) C

SEE DETAIL A



DETAIL A  
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
- E) DRAWING FILE NAME: MA03DREV11





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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