



FDMS6681Z

P-Channel PowerTrench[®] MOSFET

-30 V, -122 A, 3.2 mΩ

Features

- Max $r_{DS(on)}$ = 3.2 mΩ at $V_{GS} = -10$ V, $I_D = -21.1$ A
- Max $r_{DS(on)}$ = 5.0 mΩ at $V_{GS} = -4.5$ V, $I_D = -15.7$ A
- Advanced Package and Silicon combination for low $r_{DS(on)}$
- HBM ESD Protection Level of 8kV Typical(Note 3)
- MSL1 Robust Package Design
- RoHS Compliant

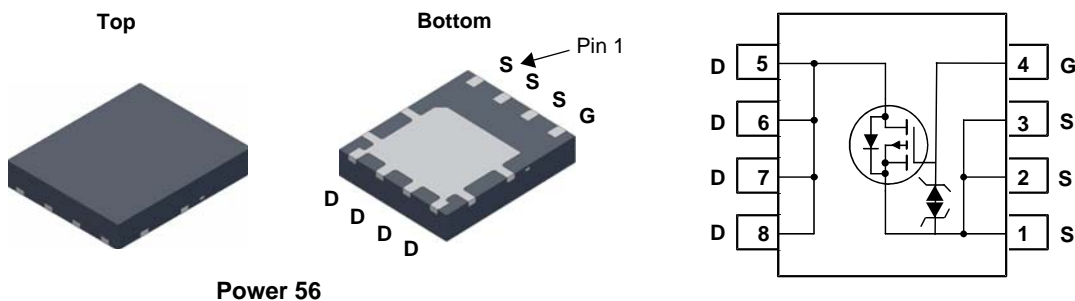


General Description

The FDMS6681Z has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Rated Value	Units
V_{DS}	Drain to Source Voltage		-30	V
V_{GS}	Gate to Source Voltage		±25	V
I_D	Drain Current -Continuous	$T_C = 25$ °C (Note5)	-122	A
		$T_C = 100$ °C (Note5)	-77	
		$T_A = 25$ °C (Note 1a)	-21.1	
		(Note4)	-600	
P_D	Power Dissipation	$T_C = 25$ °C	73	W
		$T_A = 25$ °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS6681Z	FDMS6681Z	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		20		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.7	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}, I_D = -22.1\text{ A}$		2.7	3.2	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -15.7\text{ A}$		4.0	5.0	
		$V_{GS} = -10\text{ V}, I_D = -22.1\text{ A}, T_J = 125\text{ }^\circ\text{C}$		3.9	5.0	
g_{FS}	Forward Transconductance	$V_{DD} = -10\text{ V}, I_D = -22.1\text{ A}$		143		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		7803	10380	pF
C_{oss}	Output Capacitance			1540	2050	pF
C_{rss}	Reverse Transfer Capacitance			1345	2020	pF

Switching Characteristics

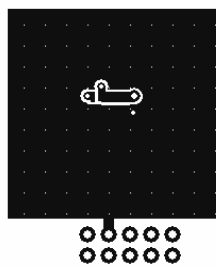
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -22.1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		15	24	ns	
t_r	Rise Time			38	61	ns	
$t_{d(off)}$	Turn-Off Delay Time			260	416	ns	
t_f	Fall Time			197	316	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		172	241	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } -5\text{ V}$	$V_{DD} = -15\text{ V},$ $I_D = -22.1\text{ A}$		97	136	nC
Q_{gs}	Gate to Source Charge				22		nC
Q_{gd}	Gate to Drain "Miller" Charge				46		nC

Drain-Source Diode Characteristics

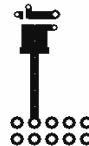
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)		0.68	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -22.1\text{ A}$ (Note 2)		0.79	1.25	V
t_{rr}	Reverse Recovery Time	$I_F = -22.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		44	71	ns
Q_{rr}	Reverse Recovery Charge			39	63	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. $125\text{ }^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Pulsed I_d please refer to Fig 12 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

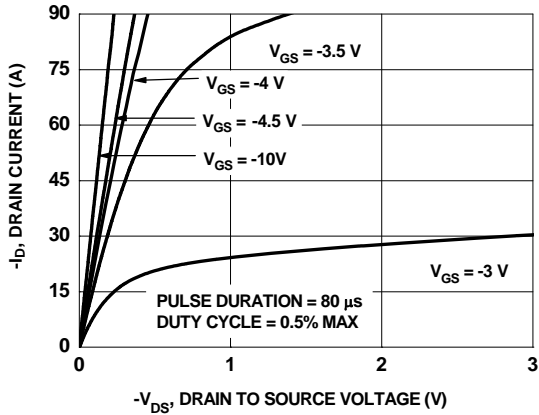


Figure 1. On Region Characteristics

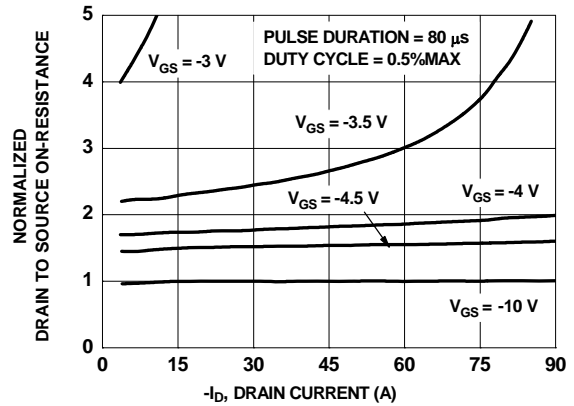


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

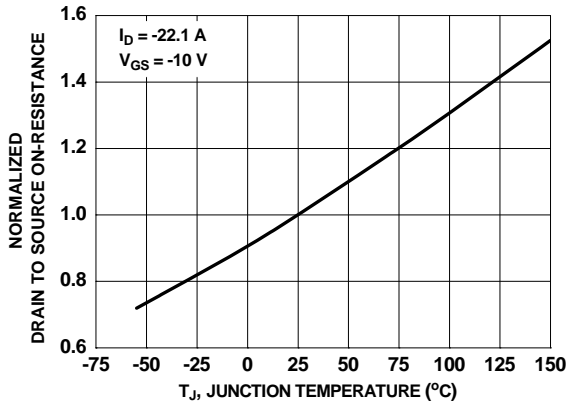


Figure 3. Normalized On Resistance vs Junction Temperature

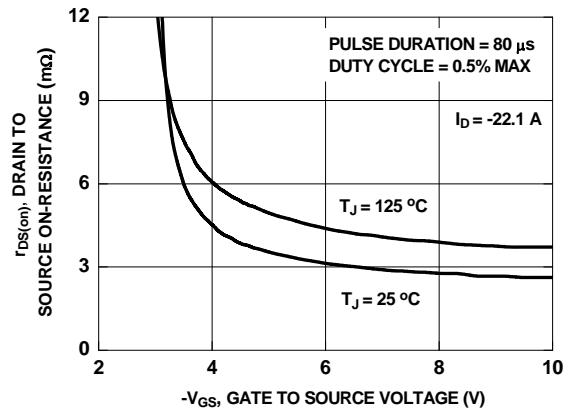


Figure 4. On-Resistance vs Gate to Source Voltage

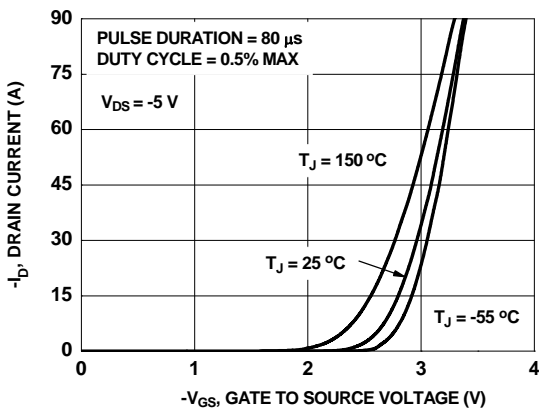


Figure 5. Transfer Characteristics

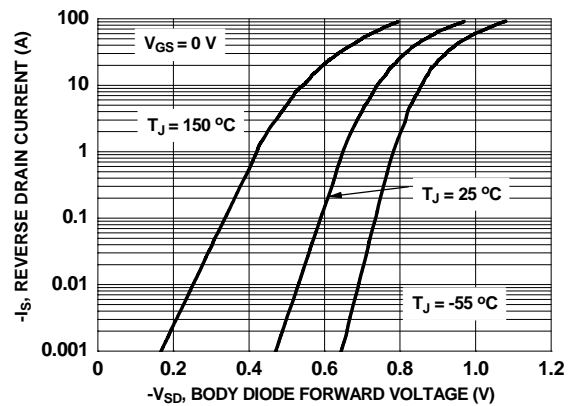


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

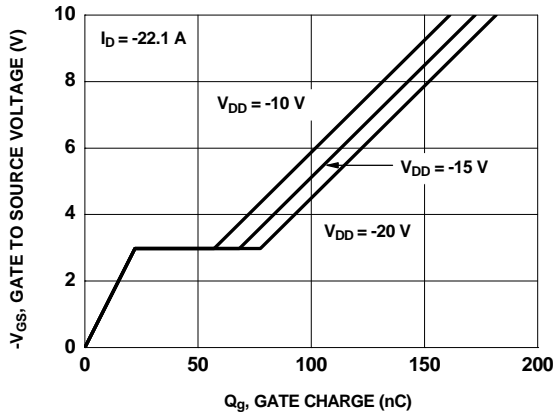


Figure 7. Gate Charge Characteristics

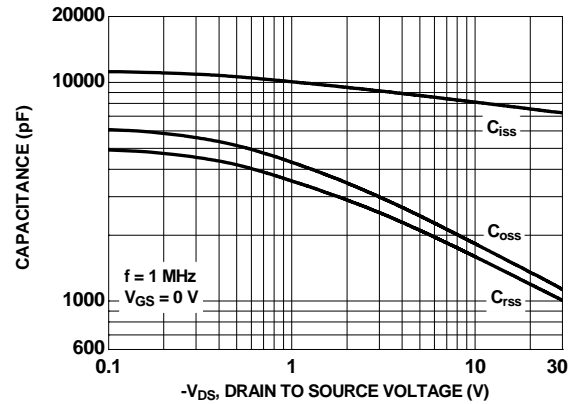


Figure 8. Capacitance vs Drain to Source Voltage

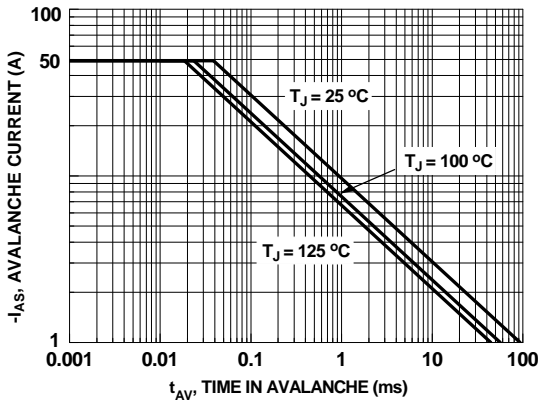


Figure 9. Unclamped Inductive Switching Capability

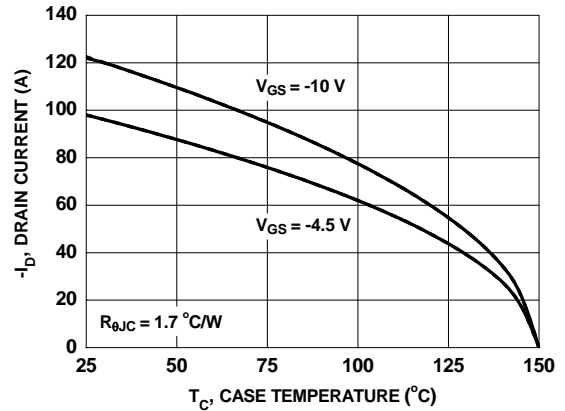


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

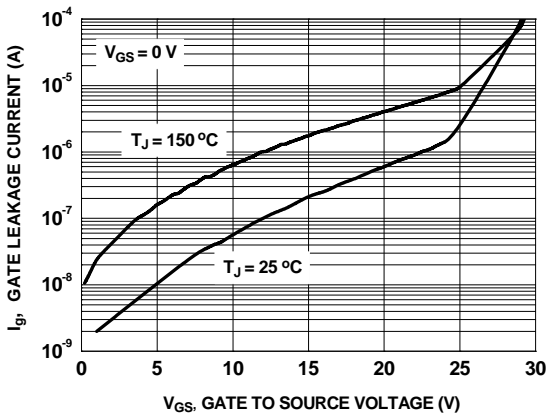


Figure 11. I_{GSS} vs V_{GSS}

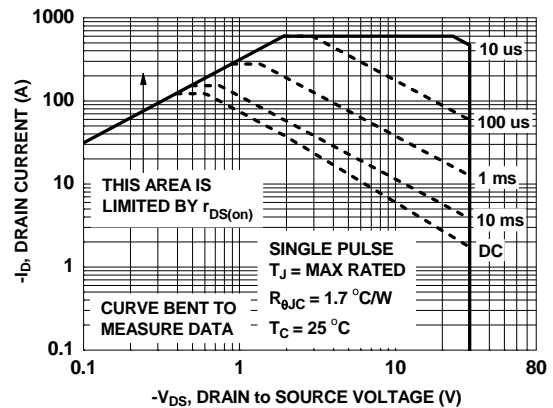


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

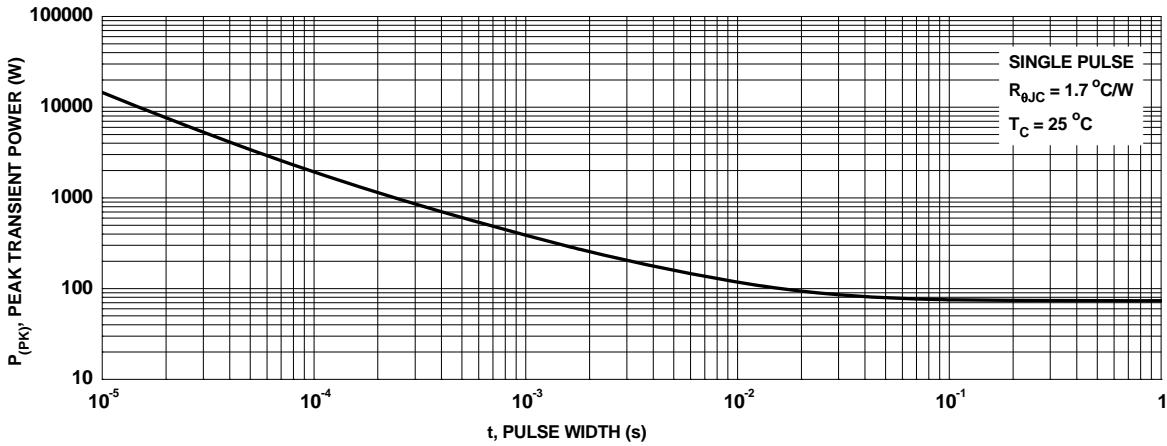


Figure 13. Single Pulse Maximum Power Dissipation

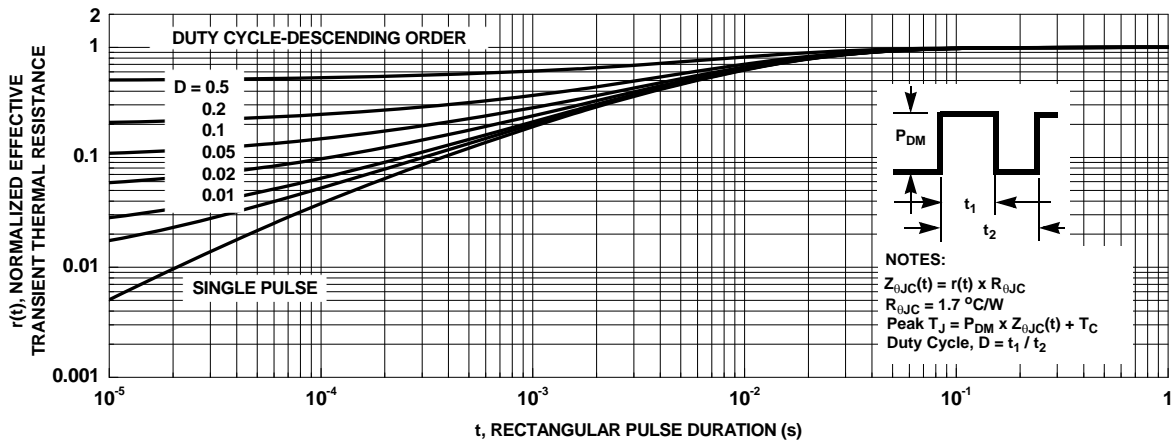
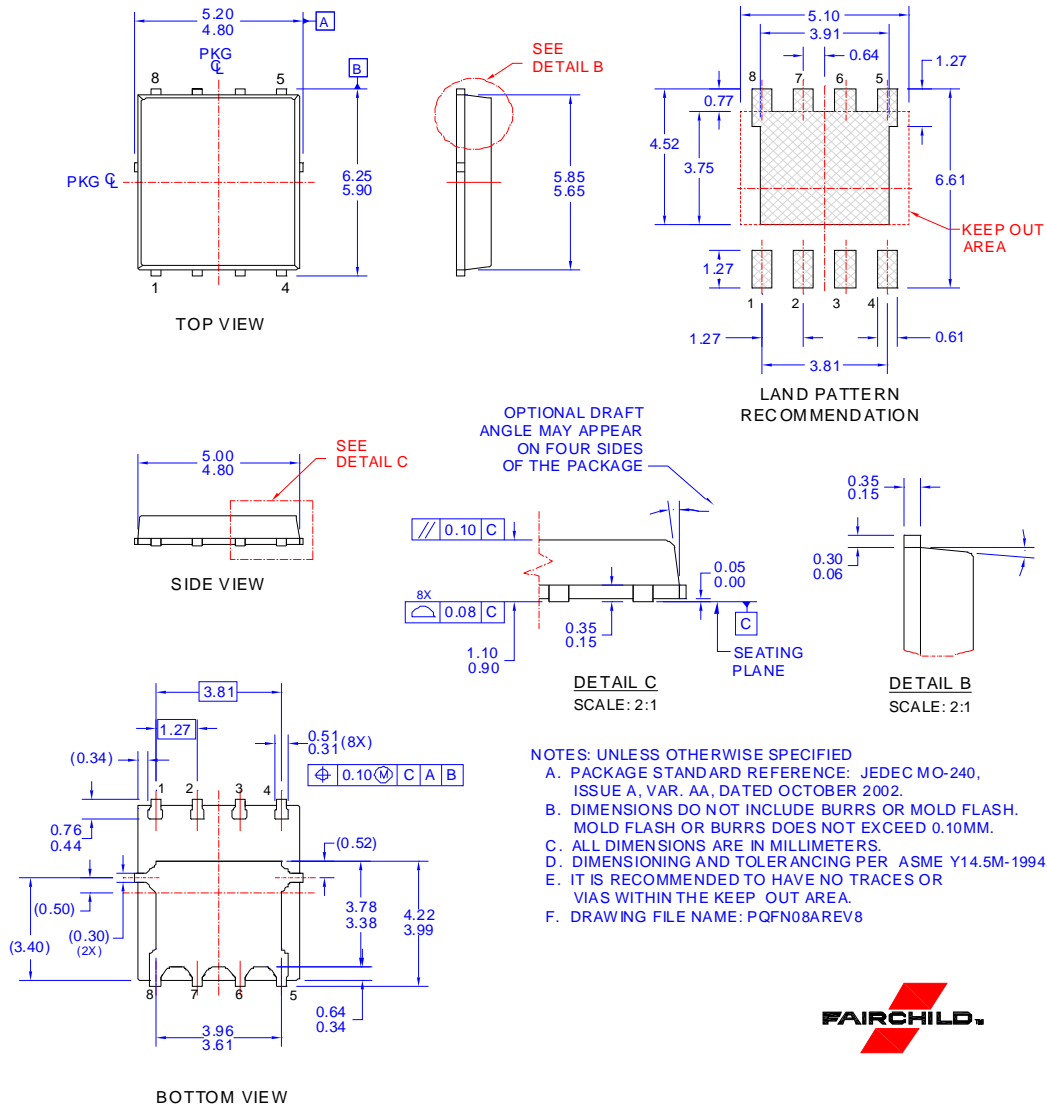
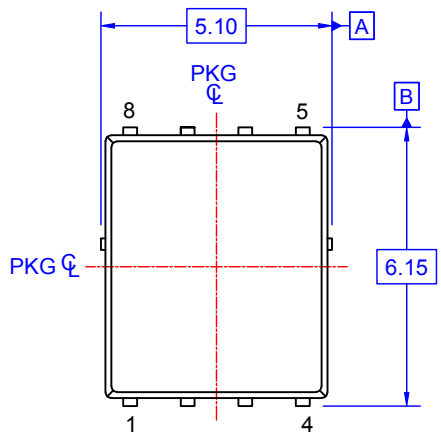


Figure 14. Transient Thermal Response Curve

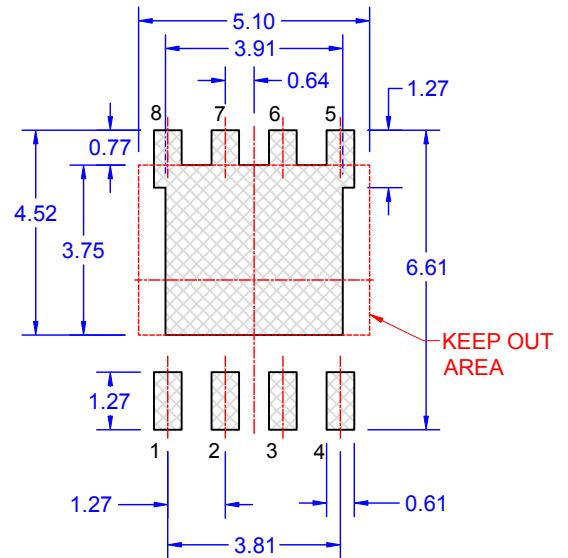
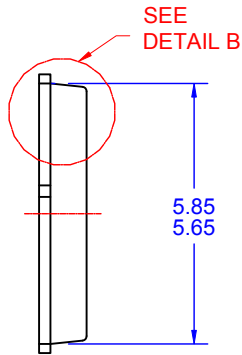
Dimensional Outline and Pad Layout



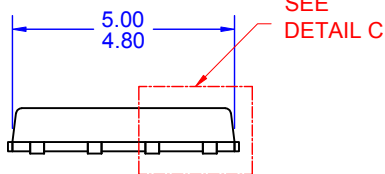
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TOP VIEW

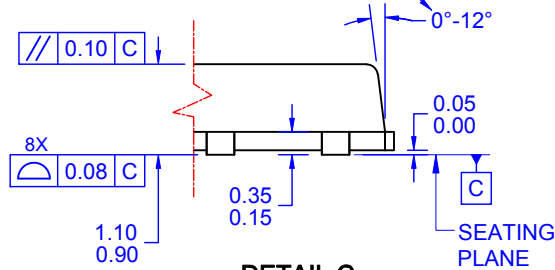


LAND PATTERN RECOMMENDATION



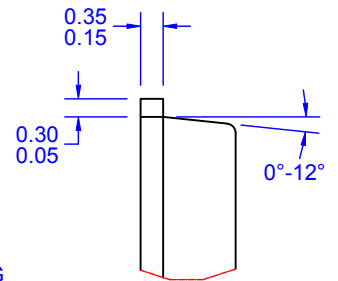
SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



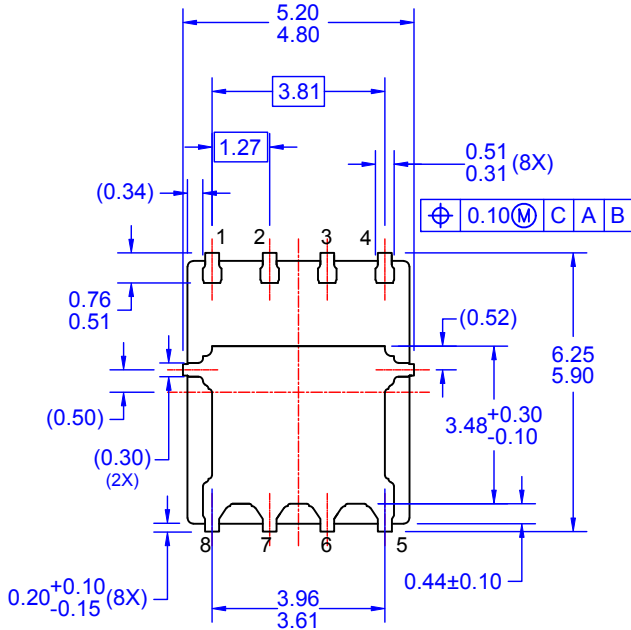
DETAIL C

SCALE: 2:1



DETAIL B

SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV9





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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