Atmel ATBTLC1000-MR110CA

BLE Module

PRELIMINARY DATASHEET

Description

The Atmel® ATBTLC1000-MR110CA is an ultra-low power Bluetooth® Smart (BLE 4.1) module with Integrated Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It can be used as a Bluetooth Low Energy link controller or data pump with external host MCU.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM, the firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

The module contains all circuitry required including a ceramic high gain antenna, 26MHz crystal and PMU circuitry. The customer simply needs to place the module on his board and provide power and a 32kHz Real Time Clock or crystal.

This datasheet is only for Production Modules. See separate Errata for modules with A5 silicon.

Features

- Complies with Bluetooth V4.1, ETSI EN 300 328 and EN 300 440 Class 2, FCC CFR47 Part 15, and ARIB STD-T66
- 2.4GHz transceiver and Modem
  - -95dBm/-93dBm programmable receiver sensitivity
  - -20 to +3dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
  - Single wire Debug (SWD) interface
  - 4-channel DMA controller
  - Brown out detector and Power On Reset
  - Watchdog Timer
- Memory
  - 128kB embedded RAM (96kB available for application)
  - 128kB embedded ROM
- Hardware Security Accelerators
  - AES-128
  - SHA-256

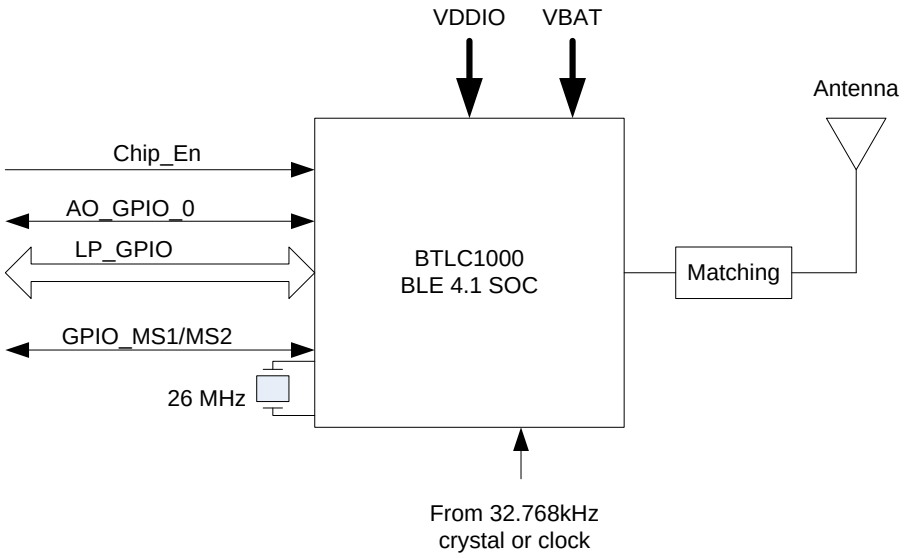
- Peripherals
  - 12 digital and one wake-up GPIO
  - 2x Mixed Signal GPIOs
  - Programmable 96kΩ pull-up or pull-down resistor for each GPIO
  - Retention capable GPIO pads
  - 1x SPI (Master/Slave)
  - 2x I^2C (Master/Slave)
  - 2x UART
  - 1x SPI Flash
  - 3-axis quadrature decoder
  - 4x Pulse Width Modulation (PWM), 3x General Purpose Timers, and 1x Wake-up Timer
  - Two channel 11-bit ADC
- Clock
  - Integrated 26MHz oscillator
  - 26MHz crystal oscillator
  - Fully integrated sleep oscillator
  - 32kHz RTC crystal oscillator
- Ultra Low power
  - Less than 1.15µA (8K RAM retention and RTC running)
  - 3.2mA peak TX current (VBAT = 3.6V, 0dBm TX power)
  - 5mA peak RX current (VBAT = 3.6V, -95dBm sensitivity)
  - Very low average advertisement current (dependent on advertisement interval)
- Integrated Power management
  - 1.8 - 4.3V input range for PMU
  - 1.62 - 4.3V input range for I/O
  - Fully integrated Buck DC-DC converter

Table of Contents

1 Block Diagram

Figure 1-1 shows the block diagram of the ATBTLC1000-MR110CA module.

Figure 1-1. Block Diagram

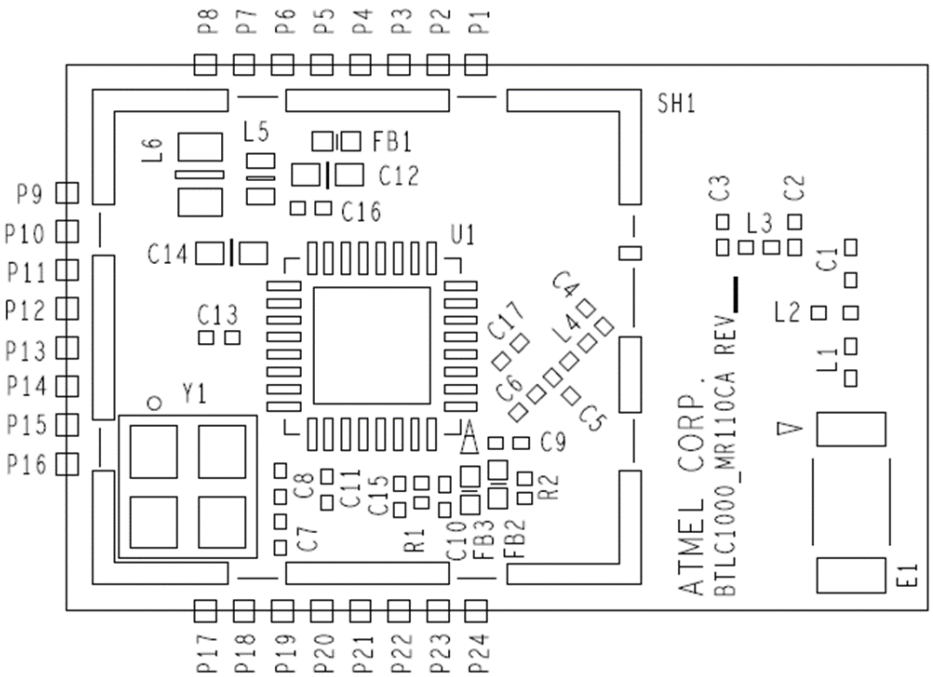


2 Pin-out Information

2.1 Pin Assignment

Figure 2-1 shows the module top view and pin numbering.

Figure 2-1. Top View



2.2 Pin Description

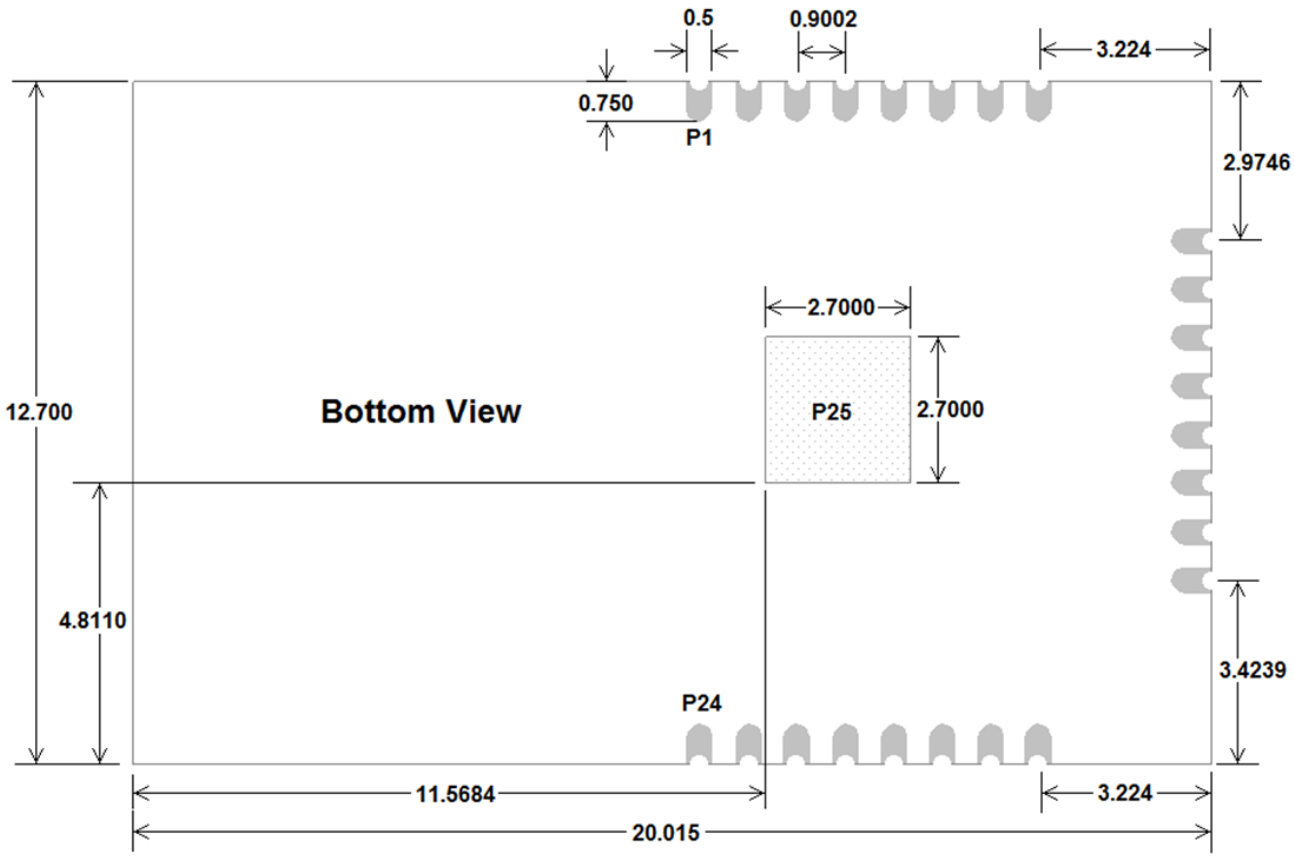
Table 2-1. Pin Description

No.	Name	Type	Description	Notes
1	Ground	Power	Ground Pin. Connect to PCB ground.	
2	LP_GPIO_0	I/O	Used for Single Wire Debug Clock	Debug interface pin. Connect to a header or test point.
3	LP_GPIO_1	I/O	Used for Single Wire Debug Data	Debug interface pin. Connect to a header or test point.
4	LP_GPIO_2	I/O	General Purpose I/O	Default function is Host UART RxD
5	LP_GPIO_3	I/O	General Purpose I/O	Default function is Host UART TxD
6	VBAT	Power	Power Supply Pin for the on chip Power Management Unit (PMU). Connect to a 1.8V – 4.2V power supply.	
7	LP_GPIO_8	I/O	General Purpose I/O	Default function is I2C_SDA
8	LP_GPIO_9	I/O	General Purpose I/O	Default function is I2C_SCL
9	Ground	Power	Ground Pin. Connect to PCB ground.	
10	LP_GPIO_10	I/O	General Purpose I/O	Default function is SPI_SCK
11	LP_GPIO_11	I/O	General Purpose I/O	Default function is SPI_MOSI
12	LP_GPIO_12	I/O	General Purpose I/O	Default function is SPI_SSN
13	Ground		Ground Pin. Connect to PCB ground.	
14	LP_GPIO_13	I/O	General Purpose I/O	Default function is SPI_MISO
15	GPIO_MS1	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
16	GPIO_MS2	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
17	Chip_En	Control	Chip Enable. A high level turns on the On Chip PMU and enables operation of the device. Low disables the device and turns off the PMU.	Control this pin with a host GPIO. If not used, tie to VDDIO
18	RTC_CLKP		Positive Pin for Real Time Clock Crystal	Connect to a 32.768KHz Crystal
19	RTC_CLKN		Negative Pin for Real Time Clock Crystal	Connect to a 32.768KHz Crystal
20	AO_GPIO_0	I/O	Always on GPIO_0. Used to wake up the device from sleep.	
21	LP_GPIO_16	I/O	General Purpose I/O	Default function is Debug UART RxD
22	VDDIO	Power	Power Supply Pin for the I/O pins. Connect to a 1.8V – 3.6V power supply.	I/O supply can be less than or equal to VBAT
23	LP_GPIO_18	I/O	General Purpose I/O	Default function is Debug UART TxD
24	Ground	Power	Ground Pin. Connect to PCB ground.	
25	Paddle	Power	Center Ground Paddle	Connect to inner PCB ground plane with an array of vias

2.3 Module Outline Drawing

Figure 2-2 shows the bottom view of the module and the module dimensions. All dimensions are in mm.

Figure 2-2. Module Dimensions (millimeters) – Bottom View



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3-1. ATBTLC1000MR110CA Absolute Maximum Ratings

Symbol	Characteristic	Min	Max	Unit
VDDIO	I/O Supply Voltage	-0.3	4.6	V
VBATT	Battery Supply Voltage	-0.3	5.0	V
V_{IN}(1)	Digital Input Voltage	-0.3	VDDIO	V
V_{AIN}(2)	Analog Input Voltage	-0.3	1.5	V
V_{ESDHBM}(3)	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	V
T_A	Storage Temperature	-65	150	°C
	Junction Temperature		125	°C

Notes:
1. VIN corresponds to all the digital pins.
2. VAIN corresponds to the following analog pins: VDDRF_RX, VDDAMS, RFIO, XO_N, XO_P, VDD_SXDIG, VDD_VCO.
3. For VESDHBM, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins include all digital pins only
   - VESDHBM is ±1kV for Class1 pins. VESDHBM is ±2kV for Class2 pins

3.2 Recommended Operating Conditions

Table 3-2. ATBTLC1000-MR110CA Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Units
VDDIO	I/O Supply Voltage Low Range	1.62	1.80	4.3	V
VBATT	Battery Supply Voltage	1.8 (note 1)	3.6	4.3	V
	Operating Temperature	-40		85	°C

Note: 1. VBATT supply must be greater than or equal to VDDIO.

3.3 Restrictions for Power States

When VDDIO is off (either disconnected or at ground potential), a voltage must not be applied to the device pins. This is because each pin contains an ESD diode from the pin to the VDDIO supply. This diode will turn on when a voltage higher than one diode-drop is supplied to the pin. This in turn will try to power up the part through the VDDIO supply.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than 0.3V below ground to any pin.

3.4 Power-up Sequence

The power-up sequence for ATBTLC1000 is shown in Figure 3-1. The timing parameters are provided in Table 3-3.

Figure 3-1. Power-up Sequence

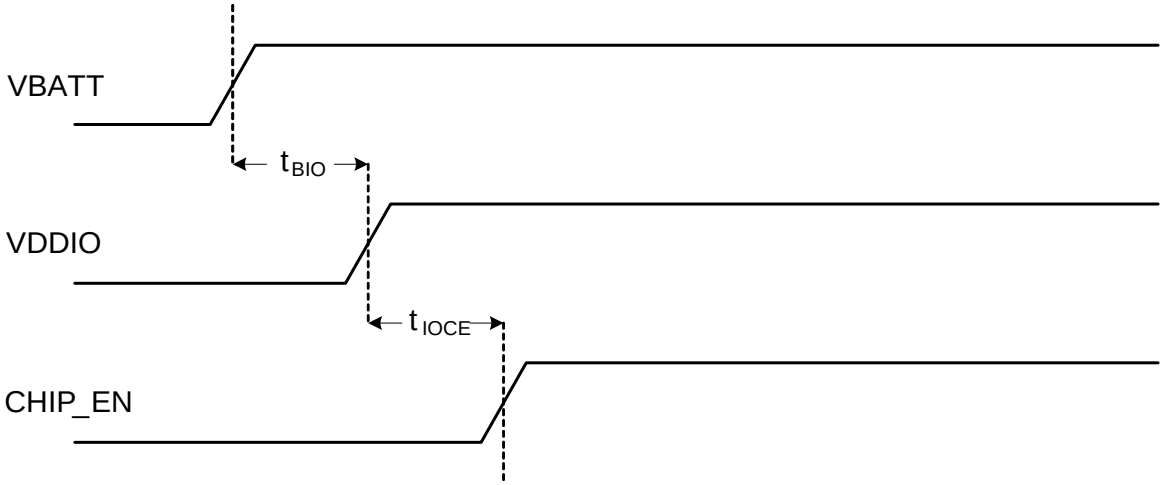


Table 3-3. Power-up Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together.
t_{IOCE}	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.

3.5 RTC Pins

Module pins 18 and 19 (RTC_CLKP and RTC_CLKN, respectively) are used for a 32.768KHz crystal. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the low drift of the 32.768kHz crystal oscillator clock and the fact that it can be accurately calibrated (±25ppm), the power consumption of the ATBTLC1000 can be minimized by leaving radio circuits in low power sleep mode for as long as possible until they need to wake up for the next connection timed event.

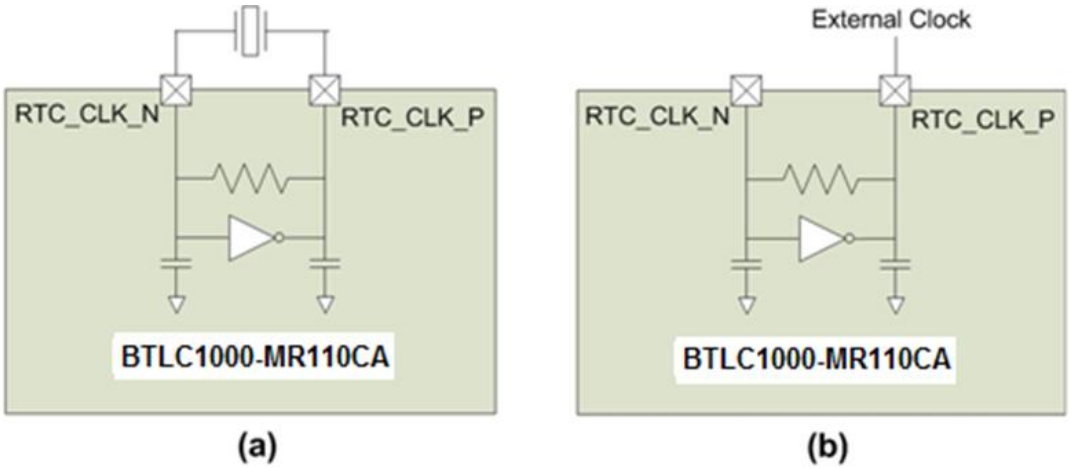
The block diagram in Figure 3-2(a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

Typically, the crystal should be chosen to have a load capacitance of 7pF to minimize the oscillator current. The ATBTLC1000 device has switchable on chip capacitance that can be used to adjust the total load the crystal sees to meet its load capacitance specification. Refer to the ATBTLC1000 datasheet for more information.

Alternatively, if an external 32.768KHz clock is available, it can be used to drive the RTC_CLKP pin instead of using a crystal. The XO has 5.625F internal capacitance on the RTC_CLKP pin. To bypass the crystal oscillator an external signal capable of driving 5.625pF can be applied to the RTC_CLK_P terminal as shown in

Figure 3-2(b). This signal must be 1.2V maximum. RTC_CLK_N must be left unconnected when driving an external source into RTC_CLK_P.

Figure 3-2. ATBTLC1000 Connections to Low Frequency Crystal Oscillator



(a) Crystal oscillator is used (b) Crystal oscillator is bypassed

Table 3-4. ATBTLC1000-MR110CA 32.768KHz External Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillation frequency		32.768		KHz	Must be able to drive 6pF load @ desired frequency
VinH	0.7		1.2	V	High level input voltage
VinL	0		0.2	V	Low level input voltage
Stability – Temperature	-250		+250	ppm	

4 Characteristics

4.1 Device States

Table 4-1. ATBTLC1000-MR110CA Device States

Device State	CHIP_EN	VDDIO	$I_{VBATT\ (typical)}$	$I_{VDDIO\ (typical)}$	Remark
BLE_On_Transmit	On	On	3.2mA	0.0µA	VBATT = 3.6V
BLE_On_Receive	On	On	5mA	0.0µA	VBATT = 3.6V
Ultra Low Power	On	On	1.25µA	0.0µA	With 8KB retention memory, BLE Timer and RTC enabled
Power_Down	GND	On	<0.1µA	<0.01µA	Chip Enable Off

4.2 Receiver Performance

Table 4-2. ATBTLC1000-MR110CA Receiver Performance

Parameter	Min.	Typ.	Max.	Unit
Frequency	2,402		2,480	MHz
Sensitivity (max. RX Gain setting)		-95		dBm
Maximum Receive Signal Level		0		dBm
CCI		13		dB
ACI (N±1)		0		dB
N+2 Blocker (Image)		-20		dB
N-2 Blocker		-30		dB
N+3 Blocker (Adj. Image)		-32		dB
N-3 Blocker		-44		dB
N±4 or greater	-45			dB
Intermod (N+3, N+6)		-33		dBm
OOB (2GHz < f < 2.399GHz)		-10		dBm
OOB (f < 2GHz)		-10		dBm

Note: 1. Expected values for production silicon.

All measurements performed at 3.6V Vbatt and 25ºC, with tests following Bluetooth V4.1 standard tests.

4.3 Transmitter Performance

Table 4-3. ATBTLC1000-MR110CA Transmitter Performance

Parameter	Min.	Typ.	Max.	Unit
Frequency	2,402		2,480	MHz
Output Power Range	-20		3.5	dBm
Max Output Power		+4		dBm
In-band Spurious (N±2)		-40		dBm
In-band Spurious (N±3)		-50		dBm
2nd Harmonic Pout		-45		dBm
Frequency Dev		250		kHz

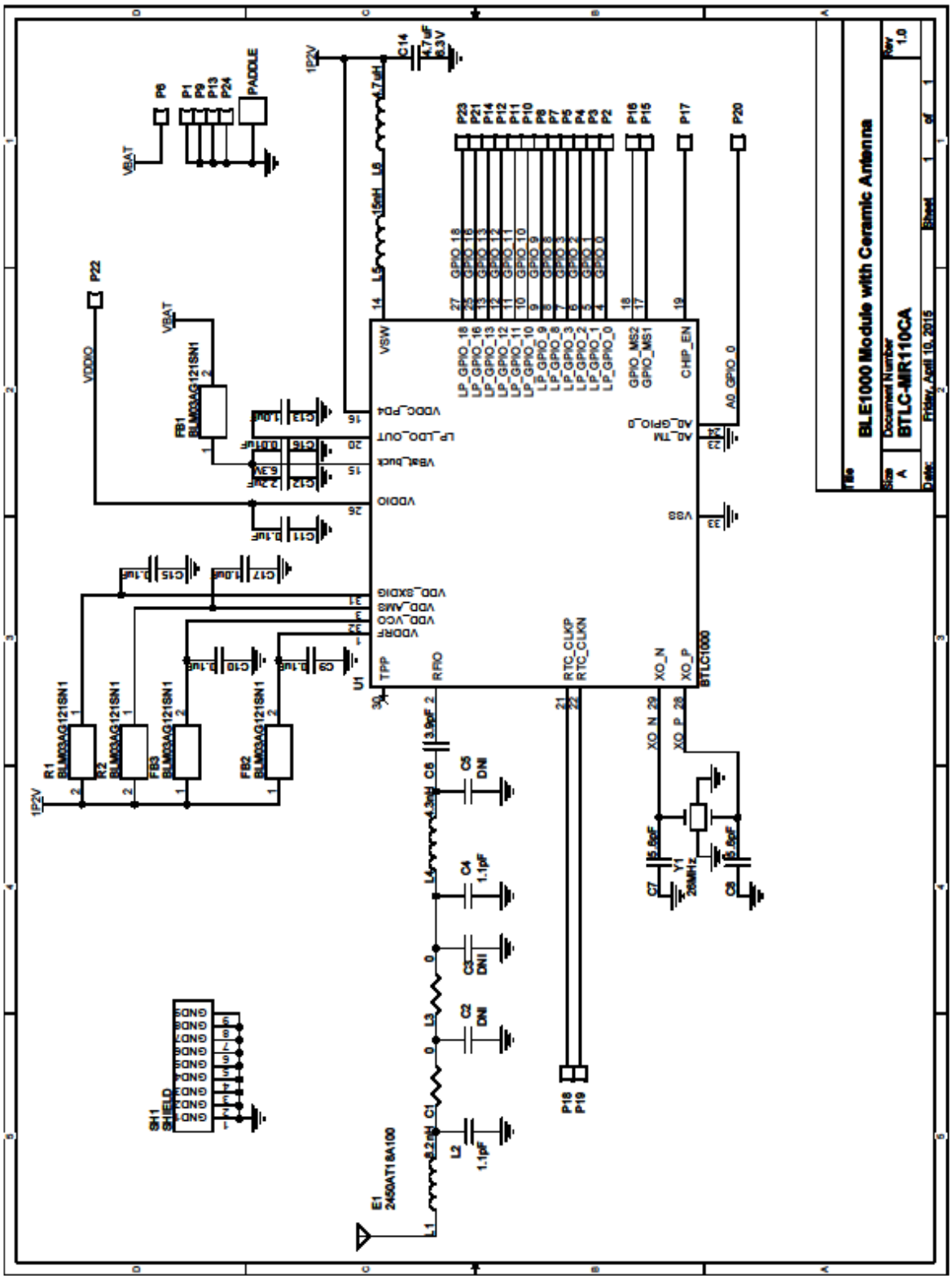
Note: 1. Expected values for production silicon.

All measurements performed at 3.6V Vbatt and 25ºC, with tests following Bluetooth V4.1 standard tests.

5 Module Schematic

Figure 5-1 shows the module schematic.

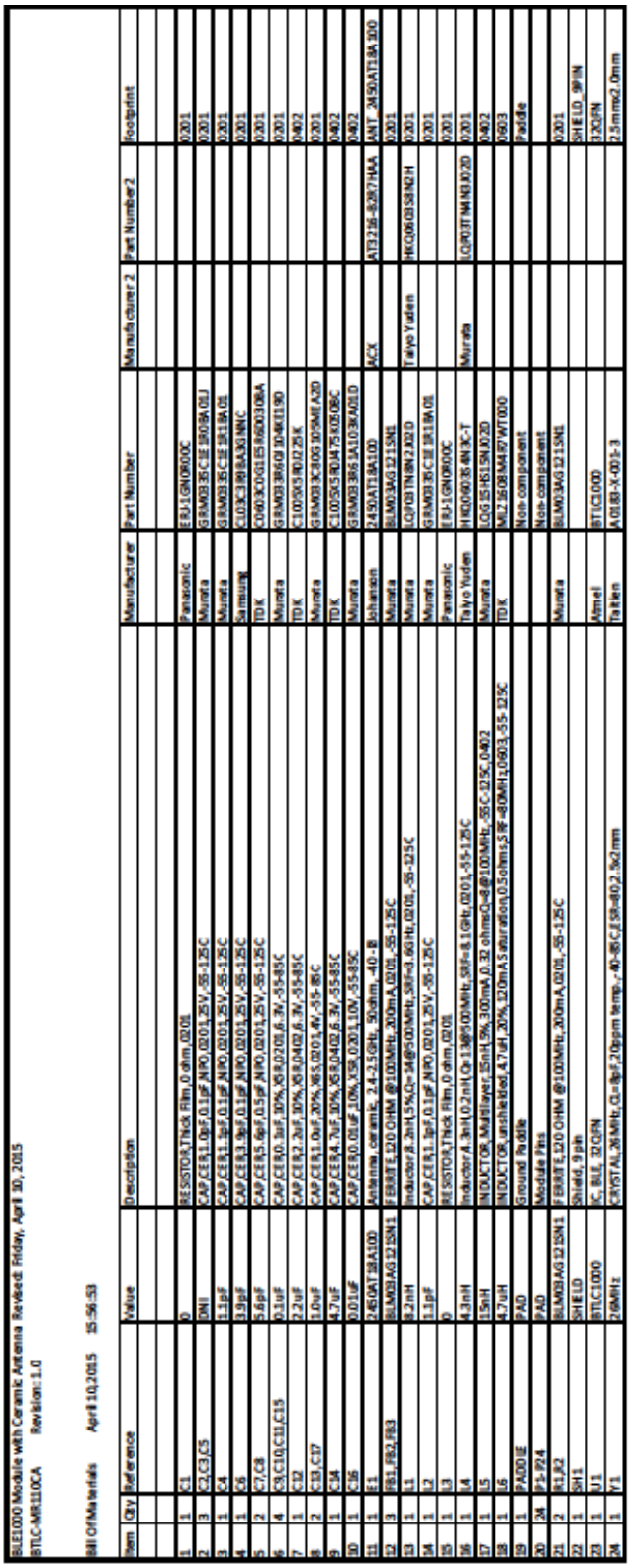
Figure 5-1. Module Schematic



6 Module Bill of Materials

Figure 6-1 shows the module Bill of Materials.

Figure 6-1. Module Bill of Materials



BLE1000 Module with Ceramic Antenna Revised: Friday, April 10, 2015
BTLC-MR110CA Revision: 1.0

Bill Of Materials April 10,2015 15:56:53

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Manufacturer 2	Part Number2	Footprint
1	1	C1	0	RESISTOR,Thick Film,0 ohm,,0201	Panasonic	ERJ-1GN0R00C			0201
2	3	C2,C3,C5	DNI	CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J			0201
3	1	C4	1.1pF	CAP,CER,1.1pF,0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R1BA01			0201
4	1	C6	1.9pF	CAP,CER,1.9pF,0.1pF,NPO,0201,25V,-55-125C	Samsung	CL03C1R9BA3GNNC			0201
5	2	C7,C8	5.6pF	CAP,CER,5.6pF,0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E5R6D030BA			0201
6	4	C9,C10,C11,C15	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-85C	Murata	GRM033R60J104KE19D			0201
7	1	C12	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K			0402
8	2	C13,C17	1.0uF	CAP,CER,1.0uF,20%,X6S,0201,4V,-55-85C	Murata	GRM033C80G105ME A2D			0201
9	1	C14	4.7uF	CAP,CER,4.7uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J475K050BC			0402
10	1	C16	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-85C	Murata	GRM033R61A103KA01D			0402
11	1	E1	2450AT18A100	Antenna, ceramic, 2.4-2.5GHz, 50ohm, -40 - 8	Johanson	2450AT18A100	ACX	AT3216-B2R7HAA	ANT_2450AT18A100
12	3	FB1,FB2,FB3	BLM03AG121SN1	FERRITE,120 OHM @100MHz,,200mA,0201,-55-125C	Murata	BLM03AG121SN1			0201
13	1	L1	8.2nH	Inductor,8.2nH,5%,Q=34@500MHz,SRF=3.6GHz,0201,-55-125C	Murata	LQP03TN8N2J02D	Taiyo Yuden	HKQ0603S8N2H	0201
14	1	L2	1.1pF	CAP,CER,1.1pF,0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R1BA01			0201
15	1	L3	0	RESISTOR,Thick Film,0 ohm,,0201	Panasonic	ERJ-1GN0R00C			0201
16	1	L4	4.3nH	Inductor,4.3nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55+125C	Taiyo Yuden	HKQ0603S4N3C-T	Murata	LQP03TN4N3D02D	0201
17	1	L5	15nH	INDUCTOR,Multilayer,15nH,5%,300mA,0.32 ohmsQ=8@100MHz,-55C-125C,0402	Murata	LQG15HS15NJ02D			0402
18	1	L6	4.7uH	INDUCTOR,unshielded,4.7uH,20%,120mA,Saturation,0.5ohms,SRF=80MHz,0603,-55-125C	TDK	MLZ1608M4R7WT000			0603
19	1	PADDLE	PAD	Ground Paddle		Non-component			Paddle
20	24	P1-P24	PAD	Module Pins		Non-component			
21	2	R1,R2	BLM03AG121SN1	FERRITE,120 OHM @100MHz,,200mA,0201,-55-125C	Murata	BLM03AG121SN1			0201
22	1	SH1	SHIELD	Shield, 9 pin					SHIELD_9PIN
23	1	U1	BTLC1000	IC, BLE, 32QFN	Atmel	BTLC1000			32QFN
24	1	Y1	26MHz	CRYSTAL,26MHz,CL=8pF,20ppm temp,-40-85C,ESR=40,2.5x2mm	Taitien	A0E8D-A-C01-3			2.5mmx2.0mm

7 Application Schematics

The ATBTLC1000-MR110CA module is fully self-contained. To use the module, just provide VBAT and VDDIO supplies. Figure 7-1 shows a typical design using the ATBTLC-MR110CA module. The schematic shows several host interfaces: UART, I²C, and SPI as well as an input to the ADC on the GPIO_MS2 pin. A user can choose the interface(s) required for their application. If a 32.768KHz Real Time Clock is not available in the system, a 32.768KHz crystal can be used. Figure 7-2 shows a design using a crystal for the Real Time Clock. The crystal should be specified with a load capacitance, CL=7pF and a total frequency error of 200ppm.

Figure 7-1. Reference Schematic

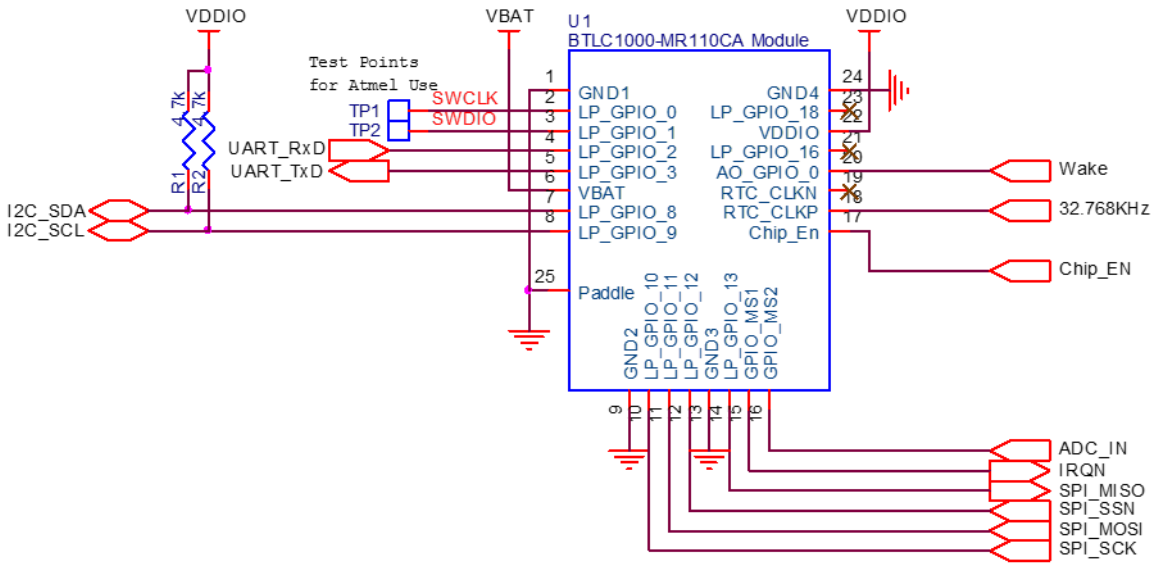
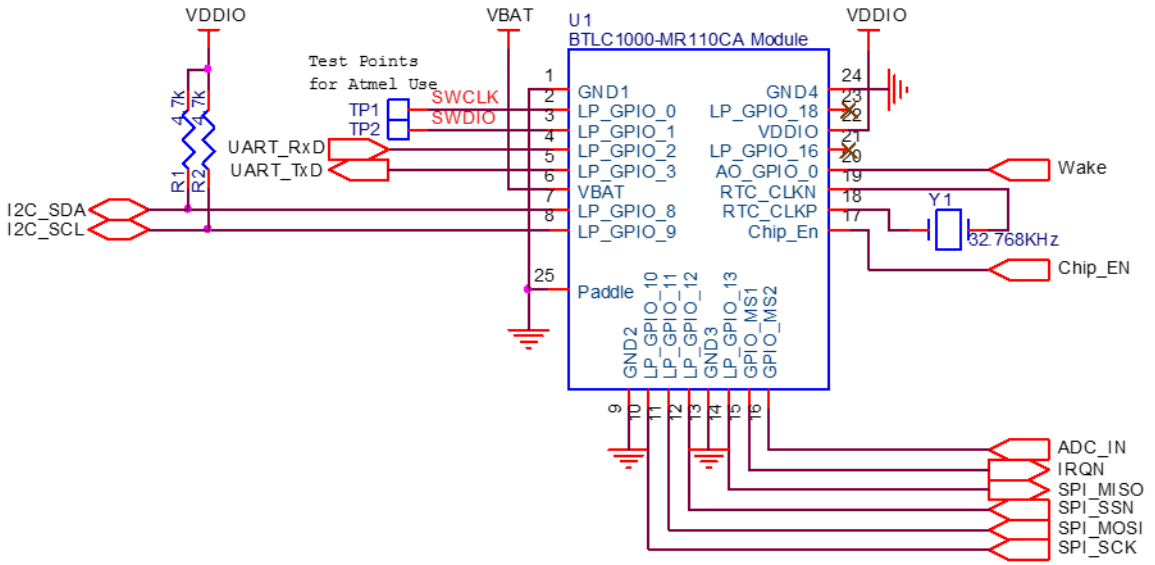


Figure 7-2. Reference Schematic with 32.768KHz Crystal



8 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias. Each ground pin of the module should have a ground via placed either in the pad or right next to the pad going down to the ground plane.
- When the module is placed on the motherboard, a provision for the antenna must be made. There should be nothing under the portion of the module which contains the antenna. This means the antenna should not be placed directly on top of the motherboard PCB. This can be accomplished by, for example, placing the module at the edge of the board such that the module edge with the antenna extends beyond the main board edge by 6.5mm. Alternatively, a cutout in the motherboard can be provided under the antenna. The cutout should be at least 22 x 6.5mm. Ground vias spaced 2.5mm apart should be placed all around the perimeter of the cutout. No large components should be placed near the antenna.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4 – 2.5GHz frequency band far away from the antenna or better - shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

8.1 Power and Ground

Dedicate one layer as a ground plane. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to insure the lowest possible inductance. The power pins of the module should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have it's own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

9 Interferers

One of the biggest problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also, make sure that no traces route underneath the RF portion of the ATBTLC1000. Also, make sure that no traces route underneath any of the RF traces from the antenna to the ATBTLC1000 input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

10 Reference Documentation and Support

10.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents are available on the Atmel web or integrated into the development tools.

Table 10-1. Reference Documents

Title	Content
Datasheet	This document
ATBTLC SOC Preliminary Datasheet	Datasheet for the ATBTLC1000 SOC contained on this module
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Programmer Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/ or contact the nearest Atmel field representative.

11 Revision History

Doc Rev.	Date	Comments
42514A	09/2015	Initial document release.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**