

# **Dust Networks**

## **Eterna LTP5901 / LTP5902 Integration Guide**

# Table of Contents

<b>About This Guide</b> .....	<b>3</b>
Audience .....	3
Related Documents .....	3
Conventions and Terminology .....	3
Revision History .....	3
<b>1 Design Guidelines</b> .....	<b>4</b>
Schematic Design .....	4
Manager Variations –IPRA, -IPRB, -IPRC .....	4
PCB Layout .....	8
Eterna LTP5901 Recommended Land Pattern (Chip Antenna) .....	9
Eterna LTP5902 Recommended Land Pattern (MMCX) .....	11
Antenna ESD Considerations .....	13
Supply Design .....	13
Voltage Supervision and Reset .....	13
<b>2 Manufacturing Guidelines</b> .....	<b>14</b>
Reflow .....	14
Solder Paste/Cleaning .....	14
Packaging .....	14

## List of Figures

Figure 1	Eterna Example Schematic .....	4
Figure 2	Eterna Extended Memory Example Schematic (page 1 of 2) .....	6
Figure 3	Eterna Extended Memory Example Schematic (page 2 of 2) .....	7
Figure 4	LTP5901 Land Pattern (Chip Antenna) .....	10
Figure 5	LTP5902 Land Pattern (MMCX) .....	12

## List of Tables

Table 1	Programming Header .....	4
Table 2	External Memory Reference Bill of Materials .....	7

# About This Guide

This document provides the design guidelines essential for incorporating either an Eterna LTP5901 or LTP5902 module. The document covers design, layout, EMI, and some manufacturing considerations.

## Audience

This document is intended for system developers, hardware designers, and layout engineers.

## Related Documents

The following related documents are available:

- [Eterna Serial Programmer Guide](#)
- [ETERNA2 User's Guide](#)

## Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

## Revision History

Revision	Date	Description
<b>040-0119 rev 1</b>	6/7/2012	Initial version
<b>040-0119 rev 2</b>	7/18/2012	Updated references
<b>040-0119 rev 3</b>	8/20/2012	Corrected keep out for LTP5901 land pattern
<b>040-0119 rev 4</b>	4/2/2013	Added support documentation for external SRAM.
<b>040-0119 rev 5</b>	5/8/2013	Added hyper link to programmer.
<b>040-0119 rev 6</b>	10/24/2013	Update SDRAM schematics and BOM

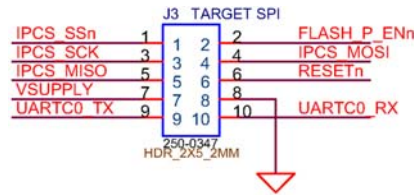
# 1 Design Guidelines

## Schematic Design

The LTP5901 and LTP5902 require little external circuitry, as the devices references, decoupling and power supply filtering are integrated. The LTP5901 and LTP5902 have been modularly certified for operation in many geographies – see the [ETERNA2 User's Guide](#) for the currently supported geographies and regulatory related specifications. If further certifications may be necessary, it is essential to provide a method to deliver specific radio test APIs via the API UART interface during testing. Test connections should be included in the schematic if the product does not provide a natural means of delivering the API calls.

During the design phase, it is recommended to include a header to allow for updating of Eterna's software.

The schematic shown in Figure 1 includes the signal connections necessary for the programming header. The part number for the header is provided in Table 1.



**Figure 1 Eterna Example Schematic**

**Table 1 Programming Header**

Reference	Value	Vendor	Vendor P/N
J3	5x2 header	Molex	87831-1020

## Manager Variations –IPRA, -IPRB, -IPRC

Without the addition of external SRAM, Eterna IP managers are limited to supporting networks of 32 or fewer motes. Eternal memory may be added to Eterna IP Manager products to:

- a. manage networks of up to 100 motes – and / or –
- b. increase throughput of the manager from 24 to 36 packets per second

The LTP5901/LTP5902-IPRA is limited to supporting a maximum of 32 motes and a maximum throughput of 24 packets per second. The LTP5901/LTP5902-IPRA does not support the use of external RAM.

The LTP5901/LTP5902-IPRC natively supports up to 32 motes with a maximum throughput of 36 packets per second. A license key can be purchased to raise the limit of the LTP5901/LTP5902-IPRC maximum network size to 100 motes. Contact your Linear Sales

representative for details on how to order license key certificates. The certificate contains a product key and instructions for requesting the generation of a license key, which typically takes one to two business days to receive a license key. License keys are entered via either the **set config** command documented in [SmartMesh IP Manager CLI Guide](#) or the **setLicense** command documented in the [SmartMesh IP Manager API Guide](#). The LTP5901/LTP5902-IPRC requires the use of external RAM.

The LTC5800-IPRB supports networks of up to 100 motes and has a maximum throughput of 36 packets per second. The LTP5901/LTP5902-IPRB requires the use of external RAM.

The schematic shown in Figure 2 and Figure 3 includes all the external connections and components necessary to add the external RAM. The connections differ from the LTP5901-IPRA as follows:

- 1) CLI access is on UARTC1, not UARTC0
- 2) Mapping of external bus signals to Eterna's general purpose function pins
- 3) The Memory, latches and pulse generators shown in Figure 3

The reference Bill of Materials (BOM) for the additional components needed for the external memory interface is shown in Table 2.

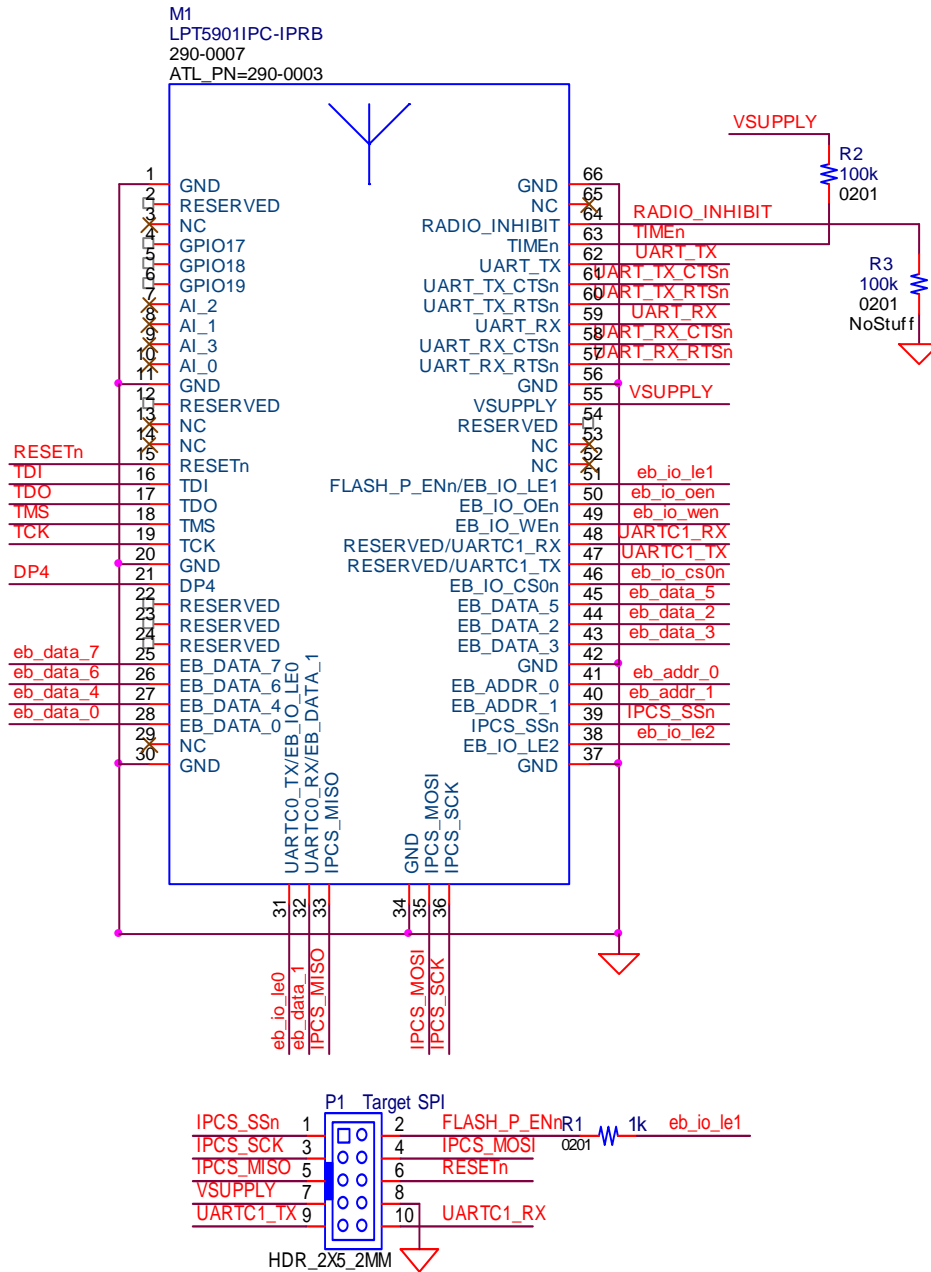
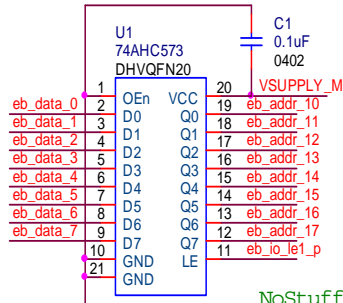
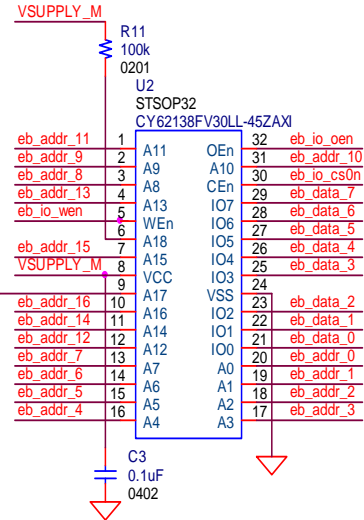
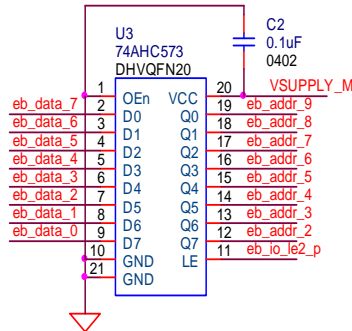


Figure 2 Eterna Extended Memory Example Schematic (page 1 of 2)

25 mil traces for VSUPPLY\_M



NoStuff R25 for 128KB



Note:  
Cypress STSOP-32 pin 1 is at pin 9, or A17

Pulse Generator Circuits

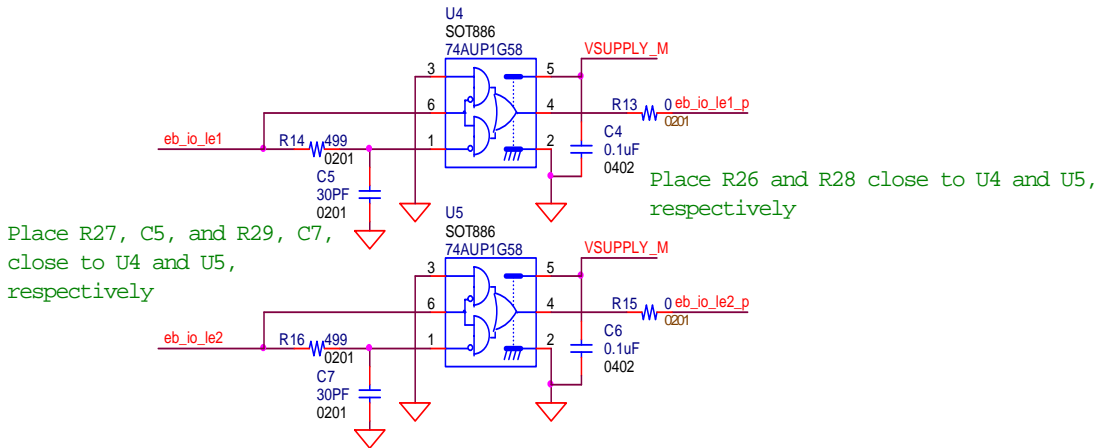


Figure 3 Eterna Extended Memory Example Schematic (page 2 of 2)

Eterna's External memory function has been tested with the BOM options shown in Table 2. The RAM components shown have been selected for low power operation and their use will result in an increase of a few  $\mu\text{A}$  of current consumption. For designs that are not energy constrained, substitution of general purpose RAMs with equal or faster speed grades should be possible. Substitution of the multi-function logic and octal latch components should be done carefully to maintain the timing generated by the pulse generation circuits.

Table 2 External Memory Reference Bill of Materials

Reference	Value	Vendor	Vendor P/N
R12, R13, R15	0	Panasonic	ERJ-1GE0R00C

Reference	Value	Vendor	Vendor P/N
R2, R3, R11	100 kOhm	Panasonic	ERJ-1GEJ104C
R14, R16	499 Ohm	Vishay	CRCW0201499RFKED
R1	1 kOhm	Panasonic	ERJ-1GEJ102C
R10	237 Ohm	Vishay	CRCW0402237RFKED
C5, C7	30 pF	Murata	GRM0335C1E300JD01 D
C1, C2, C3, C4, C6	100 nF	Murata	GRM155R71C104KA88 D
U2	128K x 8-bit RAM	Cypress	CY62128EV30LL- 45ZAXI
U2 Alternate	128K x 8-bit RAM	Renesas	R1LV0108ESA-5SI#B0
U4, U5	Multifunction Logic	NXP	74AUP1G58GM, 132
U1, U3	Octal Latch	NXP	74AHC573BQ,115
P1	5x2 header	Molex	87831-1020
M1	ETERNA Module (32-mote network, chip antenna)	Linear	LTP5901IPC-IPRC
M1 (alt. application)	ETERNA Module (100-mote network, chip antenna)	Linear	LTP5901IPC-IPRB
M1 (alt. application)	ETERNA Module (32-mote network, MMCX connector)	Linear	LTP5902IPC-IPRC
M1 (alt. application)	ETERNA Module (100-mote network, MMCX connector)	Linear	LTP5902IPC-IPRB

## PCB Layout

Eterna-based designs should adhere to the following layout-sensitive guidelines:

1. The Eterna modules include exposed test points, and pads on the bottom (mounting) side of the PCB. Exposed metal should be avoided in the on the top surface of the mating PCB in the area where the module will be mounted.
2. The LTP5901 includes a chip antenna with layout designed to work over 1 mm thick FR4, as used in the LTP5902. It is recommended to maintain an opening free of FR4 and any conductive material as far as practically possible to maximize the radio performance.
3. The LTP5902 includes a through hole mounted MMCX connector. A sufficient opening in the mating PCB must be provided – see the LTP5902 recommended land pattern later in this document for details.
4. Eterna's radios can be sensitive to EMI generated by DC/DC converters. It is recommended that such inductors are placed a minimum of 2 inches from the radio and antenna or MMCX connector. If space constraints prevent this degree of separation, inductor selection can reduce the EMI generated. Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but

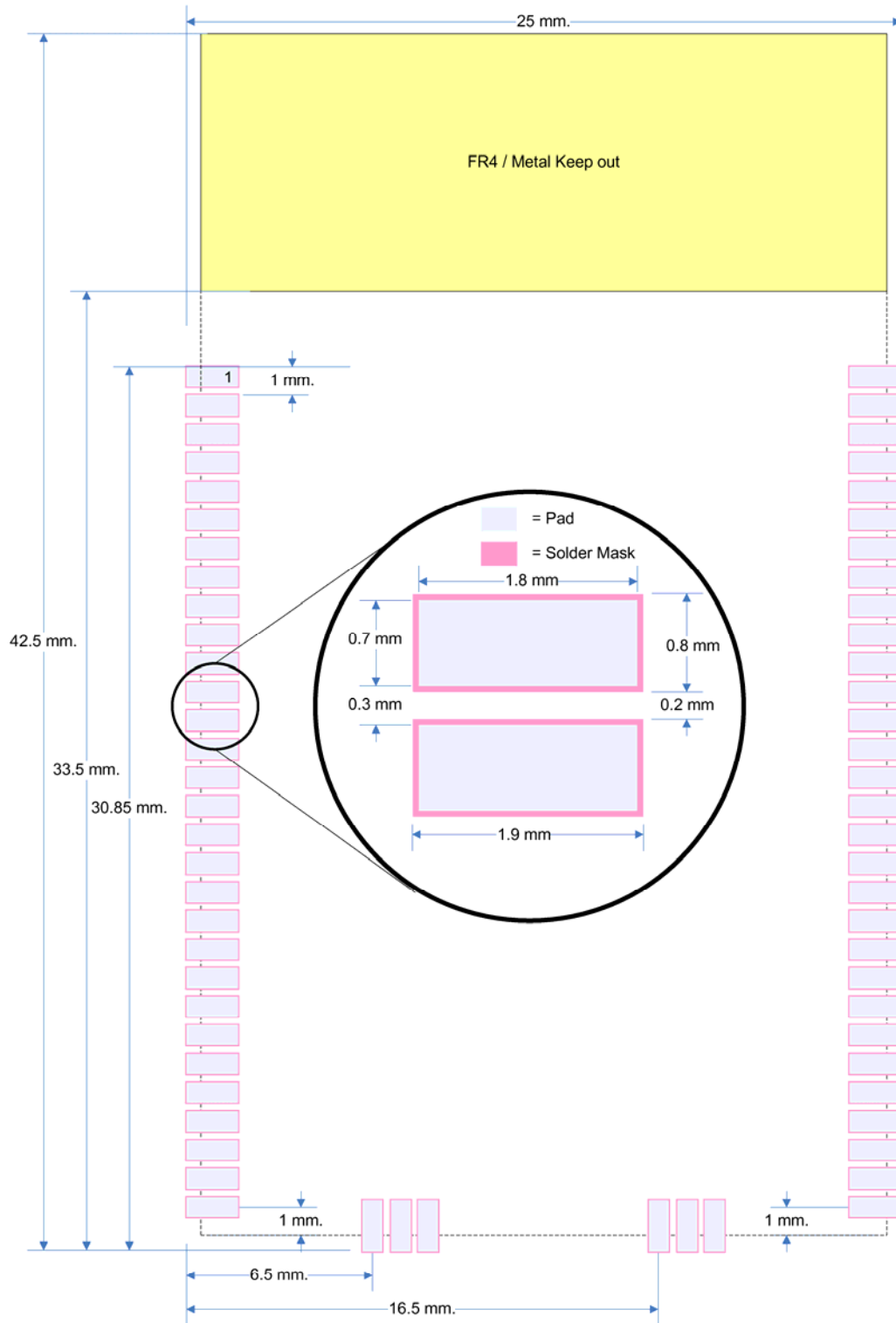


generally cost more than powdered iron core inductors with similar electrical characteristics.

### **Eterna LTP5901 Recommended Land Pattern (Chip Antenna)**

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5901 and that tolerances for metal etch are commonly more precise than solder mask deposition, it is recommended to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

Land Pattern dimensions are illustrated in Figure 4.

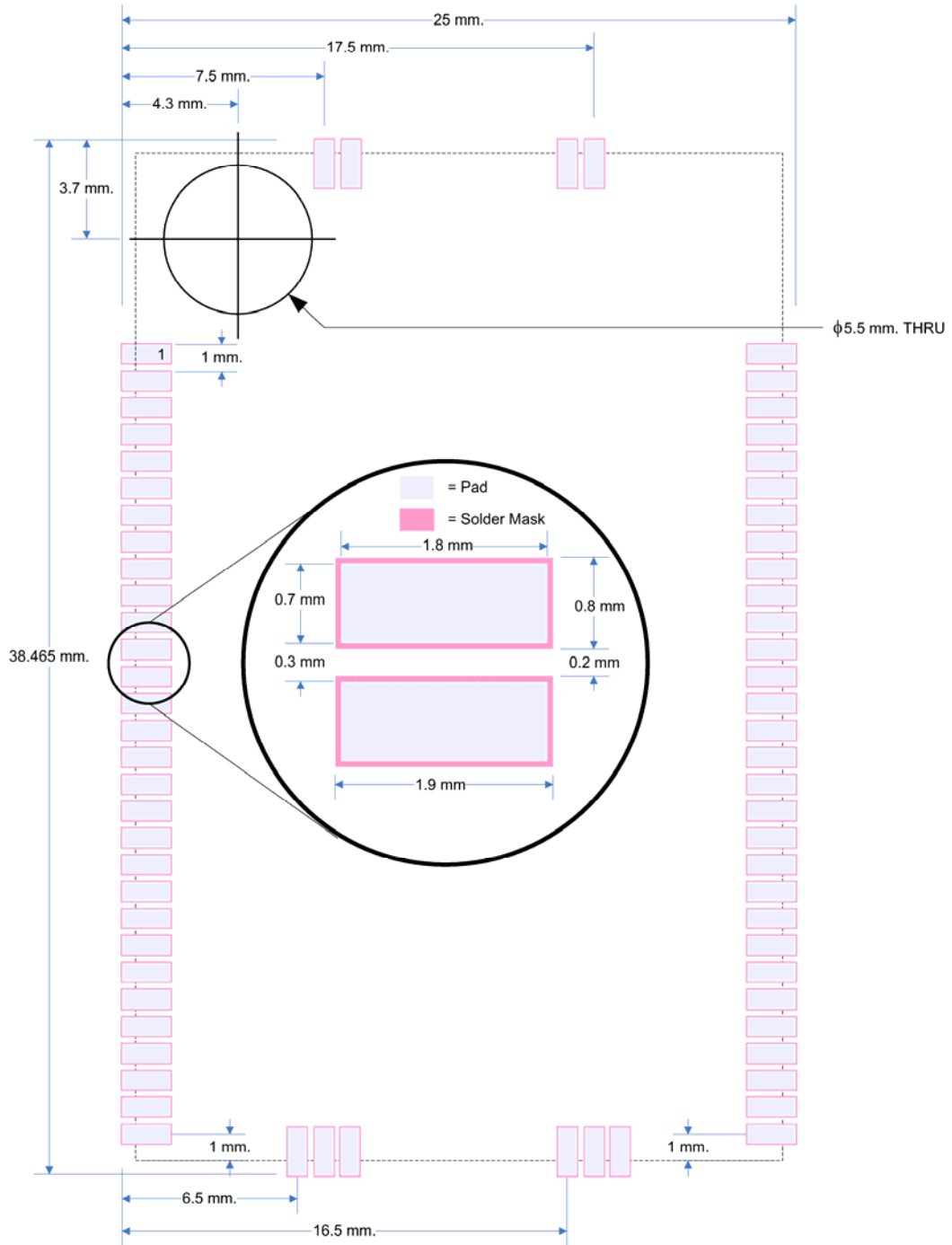


**Figure 4 LTP5901 Land Pattern (Chip Antenna)**

### **Eterna LTP5902 Recommended Land Pattern (MMCX)**

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5902 and that tolerances for metal etch are commonly more precise than solder mask deposition, it is recommended to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

Land Pattern dimensions are illustrated in Figure 5.



**Figure 5 LTP5902 Land Pattern (MMCX)**

## Antenna ESD Considerations

The antenna pin is a particularly sensitive node for electro-static discharge (ESD) since it must detect small, high-frequency signals. ESD damage may result in decreased receive or transmit performance, or other system failure. Many applications for Eterna have an exposed antenna that provides an entry point for ESD events. Proper consideration of antenna design as well as antenna protection can substantially improve ESD robustness in harsh environments.

A radome (protective covering) made of highly resistive material may be used to prevent direct contact with the antenna and/or dissipate charge. To avoid ESD events caused by triboelectric charging generated by wind passing over the antenna in dry climates, the radome design should consider bulk and surface resistivity as well as the size of the gap between the antenna metal and the interior of the radome.

In general, DC-grounded antennas (the antenna and ground have a DC short) provide superior protection to ESD events. DC-grounded antennas are highly recommended in harsh environments. Additionally, a DC path-to-earth ground should be provided whenever possible to help bleed off accumulated charge from the antenna as well as leak charge from the radome.

While these general guidelines should improve robustness to ESD events, individual implementations may have unique factors that complicate ESD protection.

## Supply Design

Due to the heavy duty cycling, Eterna's current consumption can change substantially over a short period. This does not represent an issue for systems with supplies having low source impedance (less than 5 Ohms). Regulated supplies, however, may have difficulty in the sudden changes in current consumption (more than an order of magnitude in less than 1  $\mu$ s), resulting in transient voltages on the supply co-incident with the higher current consumption of the radio operation. To ensure proper operation of the radio, a supply should be able to ramp from 250  $\mu$ A to 10 mA in less than 1  $\mu$ s without generating a transient greater than 200 mV. For systems with regulated supplies, consultation with Linear Technology is strongly recommended.

Eterna can be configured to support current limited supplies. Contact Linear Technology for details.

## Voltage Supervision and Reset

Eterna includes a power-on reset to safely set its own state during power up, and includes a brown-out circuit that immediately halts flash erase cycles and interrupts flash write cycles at the next 32-bit boundary, generating an interrupt to the CPU and maintaining state for the CPU to correct should the power supply return to normal operating levels. In the interest of avoiding flash corruption, it is **not** considered best practice to connect the RESETn lead to a voltage supervisor or to asynchronously assert RESETn without previously suspending network and flash activity.

## 2 Manufacturing Guidelines

### Reflow

Given that Eterna modules are assembled using either “SAC305”, “Alpha OM-338 CSP” or “SMIC ECO M705-GRN360” No Clear Solder Paste, careful adherence to J-STD-020 to avoid reflowing the modules during the assembly process is necessary. The solder joint quality of the “castellations” where they contact the mating PCB should meet IPC-A-610 Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations.

### Solder Paste/Cleaning

“No Clean” soldering paste is strongly recommended, as it does not require cleaning following the soldering process. Cleaning the populated modules is strongly discouraged due to the potential issues that may result. Residuals under the module are difficult to remove with any cleaning process. Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module, potentially resulting in combination with soldering flux residuals leading to short circuits between neighboring pads. Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals under the shield, which is not accessible for post-washing inspection. Ultrasonic cleaning could damage the module permanently.

### Packaging

The LTP5901 and LTP5902 modules are MSL3, however baking is required when parts are packaged in individual ESD bags.

### Trademarks

SmartMesh Industrial and Eterna are trademarks of Dust Networks, Inc. The Dust Networks logo, Dust, Dust Networks, and SmartMesh are registered trademarks of Dust Networks, Inc. The Linear logo is a registered trademark of Linear Technology Corporation. All third-party brand and product names are the trademarks of their respective owners and are used solely for informational purposes.

ARM and Cortex are trademarks or registered trademarks of ARM Limited in the EU and other countries.

### Copyright

This documentation is protected by United States and international copyright and other intellectual and industrial property laws. It is solely owned by Dust Networks, Inc. and its licensors and is distributed under a restrictive license. This product, or any portion thereof, may not be used, copied, modified, reverse assembled, reverse compiled, reverse engineered, distributed, or redistributed in any form by any means without the prior written authorization of Dust Networks, Inc.

RESTRICTED RIGHTS: Use, duplication, or disclosure by the U.S. Government is subject to restrictions of FAR 52.227-14(g) (2)(6/87) and FAR 52.227-19(6/87), or DFAR 252.227-7015 (b)(6/95) and DFAR 227.7202-3(a), and any and all similar and successor legislation and regulation.

### Disclaimer

This documentation is provided "as is" without warranty of any kind, either expressed or implied, including but not limited to, the implied warranties of merchantability or fitness for a particular purpose.

This documentation might include technical inaccuracies or other errors. Corrections and improvements might be incorporated in new versions of the documentation.

Dust Networks does not assume any liability arising out of the application or use of any products or services and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

Dust Networks products are not designed for use in life support appliances, devices, or other systems where malfunction can reasonably be expected to result in significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Dust Networks customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify and hold Dust Networks and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Dust Networks was negligent regarding the design or manufacture of its products.

Dust Networks reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products or services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Dust Network's terms and conditions of sale supplied at the time of order acknowledgment or sale.

Dust Networks does not warrant or represent that any license, either express or implied, is granted under any Dust Networks patent right, copyright, mask work right, or other Dust Networks intellectual property right relating to any combination, machine, or process in which Dust Networks products or services are used. Information published by Dust Networks regarding third-party products or services does not constitute a license from Dust Networks to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Dust Networks under the patents or other intellectual property of Dust Networks.

Dust Networks, Inc is a wholly owned subsidiary of Linear Technology Corporation.

© Dust Networks, Inc. 2012. All Rights Reserved.

Document Number: 040-0119 Eterna LTP5901 and LTP5902 Integration Guide  
Last Revised: October 24, 2013