Document Number: TWR-LS1021AGS
Rev. 3, 10/2015

TWR-LS1021A Getting Started

1 Introduction

This document describes how to connect the *QorIQ LS1021A Tower System Module (TWR-LS1021A-PB)* board and verify its basic operations such as the switches, connectors, jumpers, push buttons and LED settings, and the instructions for connecting the peripheral devices.

NOTE

It is assumed that you are familiar with the LS1021A device and the content of the *TWR-LS1021A Reference Manual* (document TWR-LS1021ARM).

The prototype part number of the LS1021A tower board system is *X-TWR-LS1021A-PB* and the production part number is *TWR-LS1021A-PB*.

The figures listed below show the main features of the secondary and primary sides of the TWR-LS1021A-PB board.

Contents

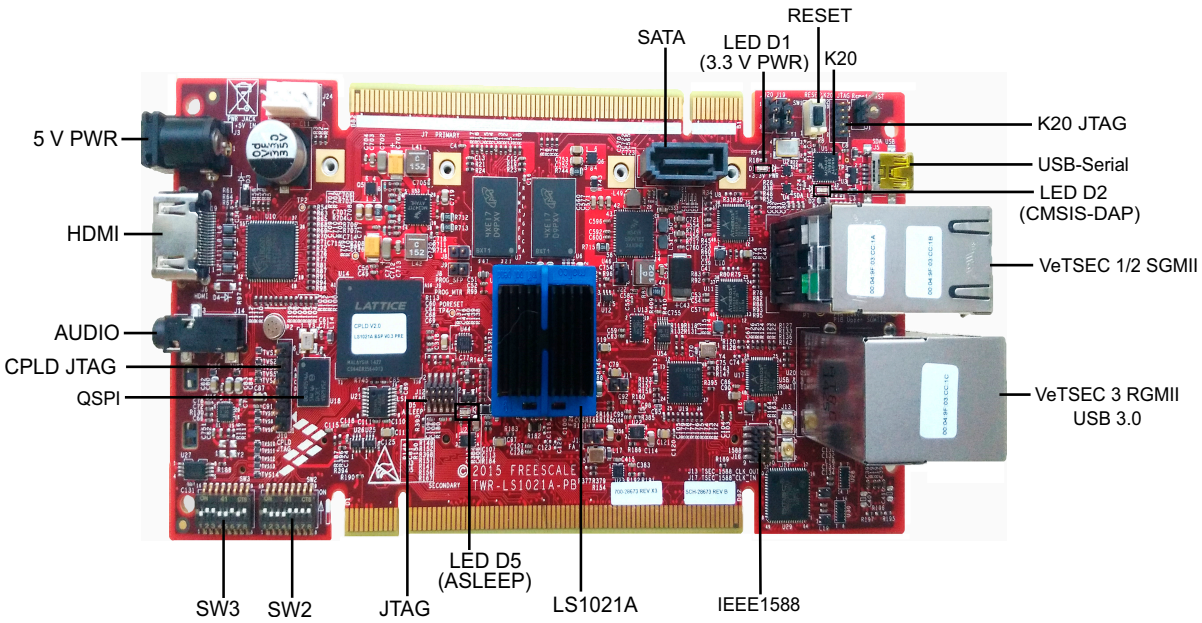

Figure 1. Primary side main features

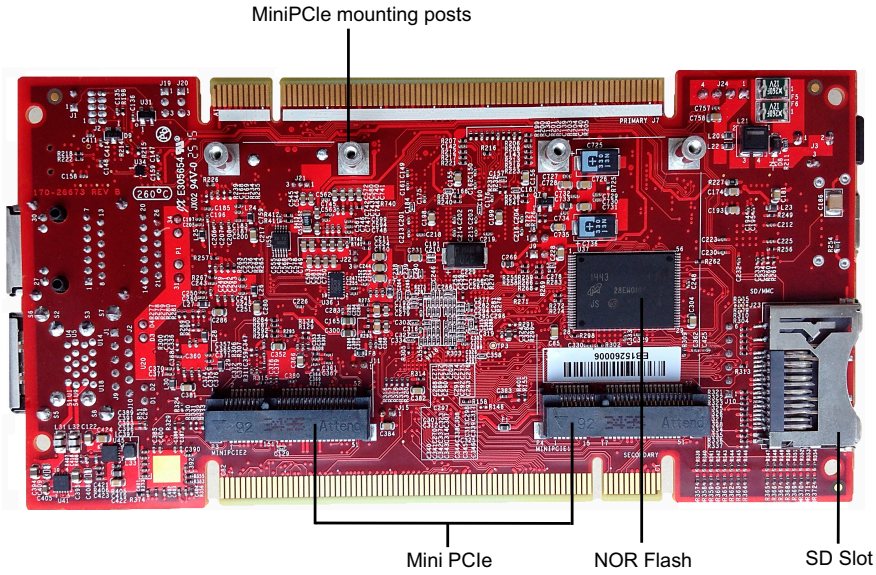

Figure 2. Secondary side main features

1.1 Related documentation

The following table lists the additional documents and resources that you can refer, for more information on the TWR-LS1021A-PB board.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Related documentation

Document	Description
LS1021A QorIQ Advanced Multicore Processor Data Sheet (document LS1021A)	This document lists the electrical characteristics, hardware design considerations, pin assignments, package information, and ordering information for the LS1021A processor.
LS1021A QorIQ Integrated Multicore Processor Reference Manual (document LS1021ARM)	This document describes the LS1021A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information.
The SystemID Format for Power Architecture™ Development Systems (document AN3638)	This document describes the SystemID, a non-volatile memory device implemented on the Freescale Semiconductor Power Architecture™ technology-based evaluation and development platforms.
TWR-LS1021A Reference Manual (document TWR-LS1021ARM)	This document describes the architecture, tower elevator connections, CPLD system controller architecture, board configuration and debug support for the QorIQ LS1021A tower system.

2 Switches and jumpers configuration

The TWR-LS1021A-PB board has two 8-way dual in line package (DIP) switch. The default DIP switch positions provide the working set up values for the board. You need to check the default positions and verify that the board is operational before changing the switches. The figure below shows the settings for the switches with their default positions.

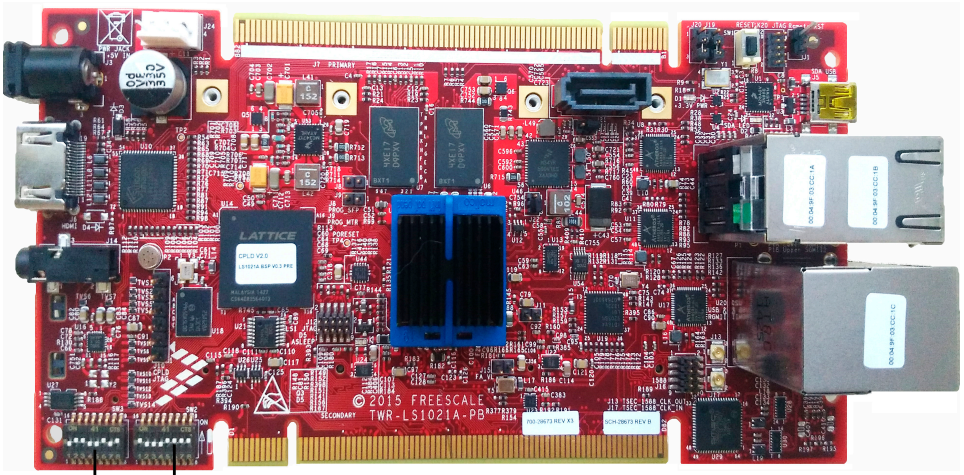

Figure 3. Default switch configuration

The table below lists and describes the default switch configurations for the TWR-LS1021A-PB board.

Table 2. Default switch settings

Feature	Settings [OFF=0 ON=1]	Option	Comments
S2.1	ON	RCW Source is NOR	NOR RCW_SEL 0 : NOR flash is disabled »1 : NOR flash is enabled (default)
S2.2	OFF	Reserved	Must be 0 [OFF]
S2.3	OFF	RCW Source is SDHC	SDHC RCW_SEL »0 : SDHC is disabled (default) 1 : SDHC is enabled
S2.4	OFF	RCW Source is QSPI	QSPI RCW_SEL »0 : QSPI is disabled (default) 1 : QSPI is enabled
S2.5	ON	Bus select is NOR or QSPI	IFC/QSPI Bus selection 0 : IFC is disabled, QSPI is enabled »1 : IFC is enabled, QSPI is disabled (default)
S2.6	ON	Differential system clock selection	Differential system clock selection 0 : Differential sysclk is selected »1 : Single-ended sysclk is selected (default)
S2.7	ON	IFC_CS1 or SPI1_PCS0 selection	IFC_CS1/SPI1_PCS0 selection 0 : IFC_CS1 is disabled, SPI1_PCS0 is enabled »1 : IFC_CS1 is enabled, SPI1_PCS0 is disabled (default)
S2.8	ON	DIPSW_IN1	CMSIS-DAP enablement control 0 : Uses the K20 IO pin to control the SDA_SWD_EN connection »1 : Ties to high to disable the CMSIS-DAP connection (default)
S3.1	OFF	96 MHz SYSCLK select or not	96 MHz SYSCLK Selection »0 : Does not select the 96 MHz as SYSCLK (default) 1 : 96 MHz as SYSCLK is selected
S3.2	ON	TEST_SEL_DRV	Drive TEST_SEL signal 0 : Non-compliant mode to support boundary scan is selected » 1 : JTAG compliant mode is selected (default)
S3.3	ON	CLKGEN_FS0 System clock frequency setting	CLKGEN_FS[0:1] 00 = 66.66 MHz 01 = 80.00 MHz »10 = 100.00 MHz (default) 11 = 83.33 MHz
S3.4	OFF	CLKGEN_FS1 System clock frequency setting	
S3.5	OFF	NOR bank select BANK_SEL	BANK_SEL » 0 : Vbank0 is selected (default) 1 : Vbank1 is selected
S3.6	ON	Signal multiplexed selection MUX_SEL	MUX_SEL 0 : 2D-ACE and LPUART1 are selected » 1 : SPI2 and UCC1&3 are selected (default)

Table 2. Default switch settings

Feature	Settings [OFF=0 ON=1]	Option	Comments
S3.7	OFF	Reserved	Must be 0 [OFF]
S3.8	ON	Reserved	Must be 1 [ON]

The table below lists the jumper settings on the TWR-LS1021A-PB board.

Table 3. Jumper settings

Jumper	Size	Name/Function	Description
J8	1x2 pin	PWR_PROG_SFP voltage setting	Open: GND (default) Shorted: 1.8 V
J9	1x2 pin	PWR_PROG_MTR voltage setting	Open: GND (default) Shorted: 1.8 V
J11	1x2 pin	TA_BB_TMP_DETECT voltage setting	Open: GND (default) Shorted: 1.0 V
J15	1x2 pin	FA_VL pin voltage setting	Open: GND (default) Shorted: 1.0 V
J19	1x3 pin	Console port TX selection	1-2: LPUART1 is selected 2-3: UART1 is selected (default)
J20	1x3 pin	Console port RX selection	1-2: LPUART1 is selected 2-3: UART1 is selected (default)
J21	1x3 pin	LVDD voltage setting	1-2: LVDD is +2.5 V 2-3: LVDD is +3.3 V (default)
J22	1x3 pin	L1VDD voltage setting	1-2: L1VDD is +2.5 V 2-3: L1VDD is +3.3 V (default)

The figure below shows the jumper settings on the board.

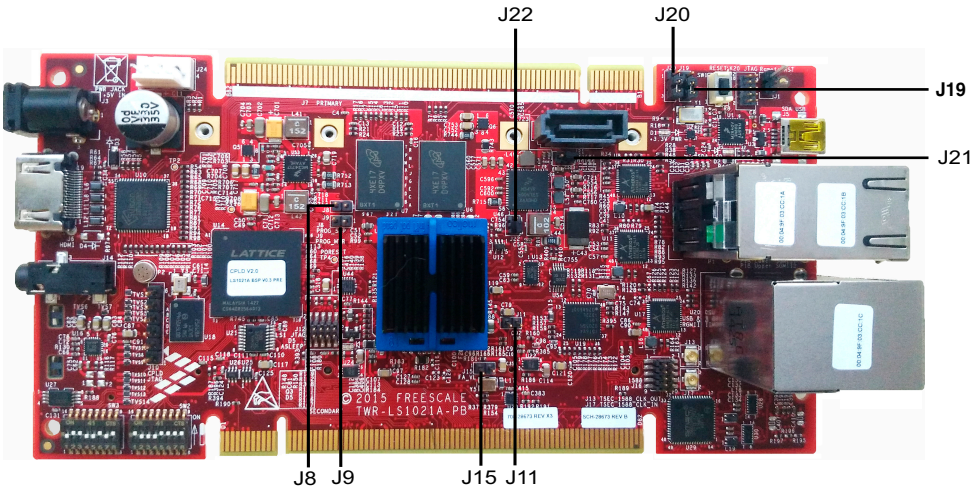

Figure 4. Jumper locations on board

3 Connecting USB UART

The TWR-LS1021A-PB board comes preloaded with the released SDK images in the NOR flash. The serial connectivity for the TWR-LS1021A-PB board is provided through a mini type B USB connector.

NOTE

You need to install the USB drivers on the host PC before using the serial terminal. You can get the drivers from the USB memory stick available in the box, *or*, you can download these drivers from,

https://mbed.org/handbook/Windows-serial-configuration

After installing the drivers, you need to set up a serial terminal using a PC communication program such as hyper terminal as listed below:

- Data rate: 115200 bps
- Number of data bits: 8
- Parity: None
- Number of Stop bits: 1
- Flow Control: Hardware/None

Then, select the first COM port assigned to the Virtual COM port.

4 Initial board start-up

The TWR-LS1021A-PB board is powered through a barrel connector. This barrel should be supplied by a 5 V @5 A supply. For more information, see Figure 1.

NOTE

It is normal for the heatsink on the TWR-LS1021A-PB board to become hot under the standard operating conditions.

To perform the initial board start up and LED check, follow the steps listed below.

1. Turn on the board through the barrel connector.
2. Check for the completion of the reset sequence indicated by the LEDs (see Figure 1 for locations). For a full description of the LED operations, see Table 4.
3. On start-up, the following LED sequence appears on the board:
   a) The LED D1 turns on to indicate that the 3V3 power is available on the board.
   b) The LED D5 turns on then off.
   c) Any Ethernet activity is indicated by the LEDs on the RJ45 connector.
   d) The LED D2 indicates that the CMSIS-DAP USB driver is loaded. If it is blinking, than the serial port is not available. You need to start up the board at J3, than insert the USB cable on the board.

The table below lists the LED operations.

Table 4. LED operation

Description	Ref	Color	LED on	LED off
3V3 Power	D1	Green	3V3 turn on	3V3 turn off
LS1021A ASLEEP	D5	Green	ASLEEP	Out of asleep
CMSIS-DAP status	D2	Green	CMSIS-DAP driver is loaded	CMSIS-DAP driver is not loaded
Ethernet eTSEC1	P1 down	Green/Orange	ON – Link Blink - Activity	No Link
Ethernet eTSEC2	P1 up	Green/Orange	ON – Link Blink - Activity	No Link
Ethernet eTSEC3	U20 up (above USB)	Green/Orange	ON – Link Blink - Activity	No Link

5 Board software configuration

The NOR flash on the TWR-LS1021A-PB board is divided in two banks. There are different images in each banks that supports the different functionality.

NOTE

The TWR-LS1021A-PB board comes pre-programmed with the NOR flash image.

The bank0 is programmed with the RCW support for the QE, and the bank1 is programmed with the RCW support for the 2D-ACE. The default is bank0.

The table below shows the switches and jumper settings on the TWR-LS1021A-PB board for the bank0 and bank1.

Table 5. Switches and jumper settings for NOR flash banks

	SW2[1:8]	SW3[1:8]	J19	J20
BANK0 (default)	10001111	01100101	2-3	2-3
BANK1	10001111	01101001	1-2	1-2

NOTE

If you enables the 2D-ACE, you have to use the lpuart as the console. The bootup information displays on the lpuart console by default. For more information on how to enable the 2D-ACE output, see the *2D-ACE Display Device Driver User Manual*, available in the Yocto source ISO folder of the USB flash drive shipped with the board.

You can also access the content available in the USB flash drive shipped with the board, from the following location:

http://www.freescale.com/TWR-LS1021A

The figure below shows the settings for the bank0 and bank1.

	SERDES Lane A	SERDES Lane B	SERDES Lane C	SERDES Lane D	GROUP2 EC3	GROUP3 EC2	GROUP4 EC1	GROUP1 QE/TDM	UART	I2C
Bank1	PCIE#1 (X1)	SATA	PCIe#2 (X1)	SGMII 2	EC3- RGMII	CAN3, 4	SAI	2D-ACE	LPUART	I2C 1,2,3
Bank0	PCIE#1 (X1)	SATA	SGMII 1	SGMII 2	EC3- RGMII	CAN3, 4	CAN1, 2	UCC	UART	I2C 1,2,3

Figure 5. NOR Flash configurations on bank0 and bank1

The figure below shows the TWR-LS1021A-PB block diagram.

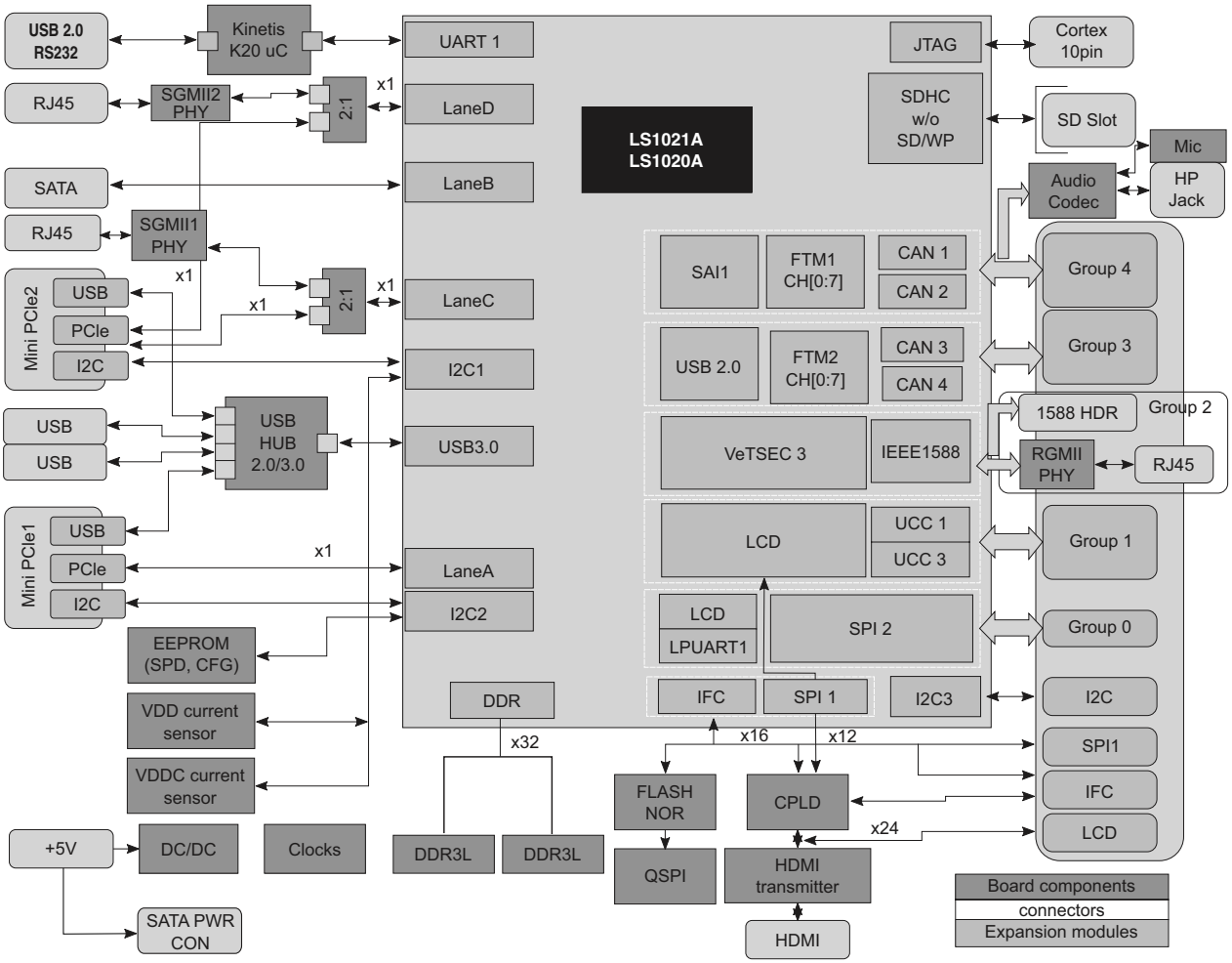

Figure 6. TWR-LS1021A-PB block diagram

6 JTAG connectivity unit

This section explains the following two methods to configure the JTAG connectivity unit supported by the CodeWarrior Development Studio for QorIQ LS series on the TWR-LS1021A-PB board:

- Section 6.1, “Connecting JTAG using CodeWarrior TAP”

- Section 6.2, “Enabling CMSIS-DAP”

6.1 Connecting JTAG using CodeWarrior TAP

To connect the JTAG using the CodeWarrior TAP, perform the following steps:

1. Connect the JTAG connectivity unit to the J12 JTAG connector on the board. The Pin 1 is marked on the board.
2. Switch on the power to the board.
3. Check for the completion of the reset sequence (see Section 4, “Initial board start-up). Ensure that the LED D5 turns off.
4. Follow the on-screen instructions.

The JTAG using the CodeWarrior TAP is connected to your board.

6.2 Enabling CMSIS-DAP

The TWR-LS1021A-PB board supports the CMSIS-DAP interface. The CMSIS-DAP interface provides a standard access to the Coresight debug access port (DAP) of the ARM® Cortex® microcontroller through the USB.

The board is implemented with the CMSIS-DAP as an on-board interface chip that provides a direct USB connection to the debugger running on your host machine on one end, and the JTAG connection to the target device to access the Coresight DAP on the other end.

To enable the CMSIS-DAP interface on your board:

1. You have to change the switch SW2[8] = 0.
2. Ensure that your CW TAP device is not plugged in.
3. Attach the micro USB cable to the J5 USB serial connector.

This provides a serial connectivity and the CMSIS-DAP connection (optional).

For the detailed setup procedure, see the *CodeWarrior Development Studio for QorIQ LS series - ARM V7 ISA Getting Started Guide* (document CWARMV7GS) from the following location:

`http://cache.freescale.com/files/soft_dev_tools/doc/quick_ref_guide/CWARMv7GS.pdf`

7 TWR-LS1021A-PB OOBE demo

The out-of-box-experience (OOBE) is a demo program which shows the wireless networking, graphics and audio playing functionality of the TWR-LS1021A-PB. The image files for the demo are available in the SD card shipped with the board. You need to insert the SD card into the board to run the demo.

For the detailed instructions to run the demo, see the *TWR-LS1021A OOBE Demo Quick Start Guide.pdf* under `\OOBE-demo\` folder in the USB flash drive shipped with the board.

You can also access the content available in the USB flash drive shipped with the board, from the following location:

`http://www.freescale.com/TWR-LS1021A`

8 Revision History

The table below lists the revision history of this document.

Table 6. Revision history

Revision number	Date	Topic cross-reference	Change description
Rev. 3	10/2015	Section 6.2, “Enabling CMSIS-DAP”	Updated this section.
Rev. 2	07/2015		Updated the TWR-LS1021A instances to TWR-LS1021A-PB.
		Figure 1 Primary side main features	Updated the TWR-LS1021A board images with the TWR-LS1021A-PB board images.
		Figure 3 Default switch configuration	Updated the figure for the default settings on SW3[1:8].
		Table 2 Default switch settings	Updated the table for the S2.6, S2.8, and S3.6 switch settings and descriptions.
		Table 3 Jumper settings	Updated the table for the J8, J9, J11, J15, J19, J20, J21, and J22 jumper settings.
		Figure 4 Jumper locations on board	Updated the figure for the J8, J9, J11, J15, J21, and J22 jumper locations.
		Figure 5 NOR Flash configurations on bank0 and bank1	Updated the figure for the TWR-LS1021A-PB board settings.
		Figure 6 TWR-LS1021A-PB block diagram	Updated the figure for the TWR-LS1021A-PB block diagram.
Rev. 1	11/2014	Figure 1 Primary side main features	Updated the figure for the LED locations.
		Figure 3 Default switch configuration	Updated the figure for the default settings on SW3[1:8].
		Table 2 Default switch settings	Updated the table for S3.6.
		Section 3, “Connecting USB UART”	Updated the section for the serial terminal set up details.
		Section 5, “Board software configuration”	Updated the section for the switches and jumper settings, output device as 2D-ACE and two block diagrams, Figure 5 NOR Flash configurations on bank0 and bank1 and Figure 6 TWR-LS1021A-PB block diagram.
		Section 6, “JTAG connectivity unit”	Updated the content to create the sub-section, Section 6.1, “Connecting JTAG using CodeWarrior TAP”.
		Section 6.2, “Enabling CMSIS-DAP”	Added a new sub-section to describe how to enable the CMSIS-DAP support.
		Section 7, “TWR-LS1021A-PB OOBE demo”	Added a new section to introduce the OOBE demo.
Rev. 0	09/2014		Initial public release.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Warranty:

Visit freescale.com/warranty for complete warranty information.

Document Number: TWR-LS1021AGS REV 3
Agile Number: 926-28673