

PCIE16X-800EVK User Guide

PCIE 16X Lane Card Evaluation Kit

General Description:

The PCIE16X-800EVK is a PCIe add-in riser card for PCIe 16x applications. It provides a complete platform to evaluate 4 - DS80PCI800SQ, 8 channels PCIe repeater for PCIe system protocol and lane negotiation validation. The card has a 16X PCIe edge fingers at J1 which plugs into a motherboard that has a PCIe 16X connector. The card also has a PCIe 16X connector at J2 for endpoint connection (PCIe graphic card or SATA/SAS raid controller card).

Features:

- 8 channel PCIe repeater up to 8 Gbps (GEN 3)
- Low power consumption, with option to power down unused channels
- Adjustable receive equalization
- Adjustable transmit VOD and De-emphasis
- IDLE detection — squelch function auto mutes the output
- Programmable via pin selection or SMBus interface
- Single supply operation: VIN = 3.3V±10% or VDD = 2.5V ±5%
- -40°C to +85°C Operation
- >6 kV HBM ESD Rating
- High speed signal flow-thru pin-out package - SQA54A: 54-pin LLP (10 mm x 5.5 mm, 0.5 mm pitch)

Applications:

- Extends FR-4 Backplane Trace for PCIe Applications

PCIE16X-800EVK Demo Kit Contents:

- End User License Agreement
- PCIE16X-800EVK User Guide Rev 1.2
- PCIE16X-800EVK Board

Ordering Information:

SMA Evaluation Kit: PCIE16X-800EVK



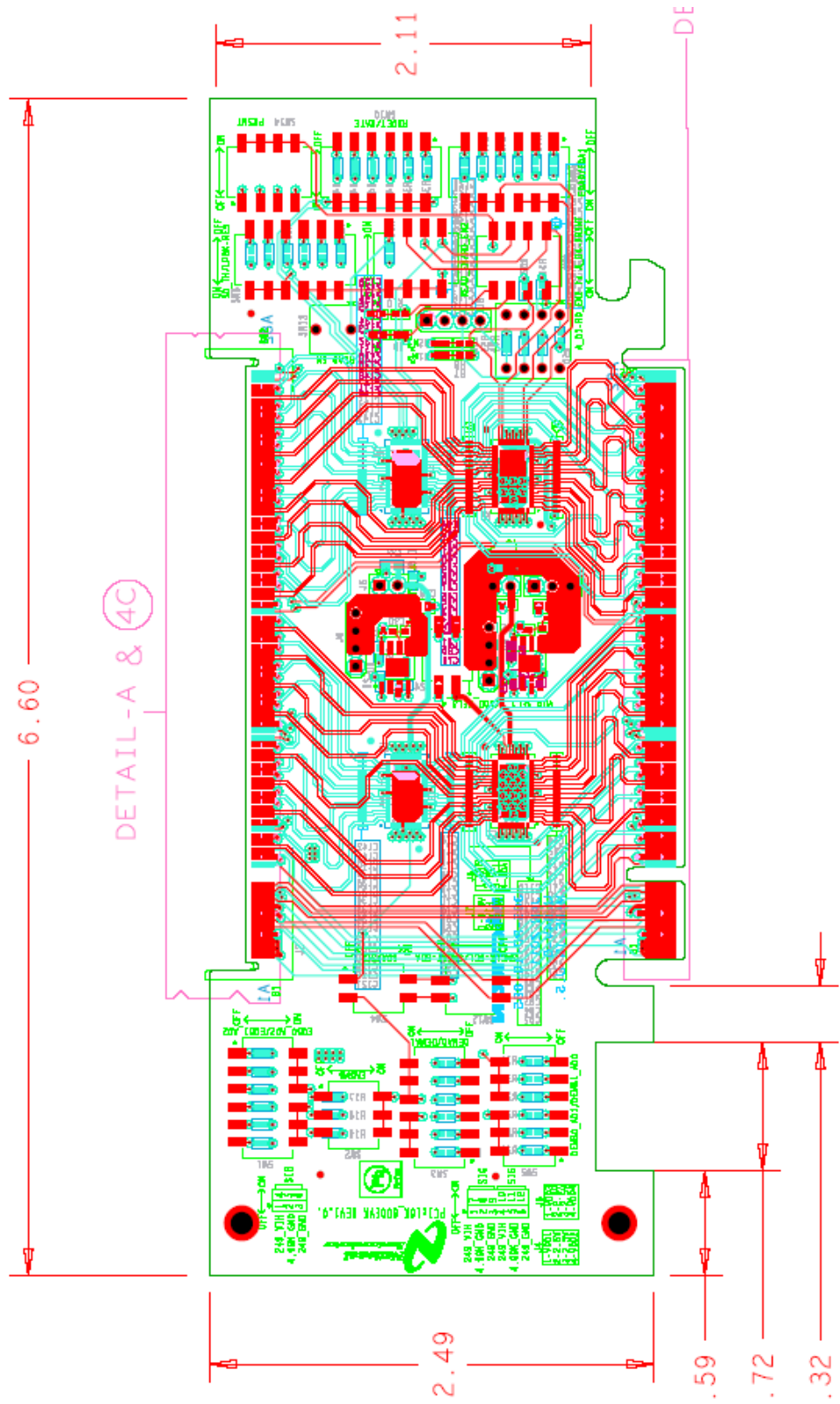


Figure 1. PCIE16X-800EVK Evaluation Board



Table 1. Switches to set the 4-level input control pins

4 – level Input Settings	Setting for 3 pin switches (3-2-1)
0 – Tie 249 ohm to GND	ON – OFF – OFF
R – Tie 5k ohm to GND	OFF – ON – OFF
F – FLOAT (open)	OFF – OFF – OFF
1 – Tie 249 ohm to VIH	OFF – OFF – ON

The following switches are used to set the input condition for the 4-level inputs:

SW1, SW2, SW3, SW5, SW6, SW10, SW11.

There are 3 switches connected to an input signal pin. Each switch when set to the ON position sets the pin to one of the 4-level setting. The 6 pin switches are assigned similar to the 3 pin switches. The only difference is 2 signal pins are connected and thus 6-5-4 is for the one signal pin and 3-2-1 is for another signal pin. Please note only 1 switch at the ON position is allowed.

Table 2. Connection and Control Description

Component	Name	Function
J1	PCIE TX/RX	High speed differential TX/RX from/to Root Complex
J2	PCIE TX/RX	High speed differential TX/RX to/from End Point
J3, J5	3.3V to VIN	3.3V DC Power – VIN to DS80PCI800SQ Jumper ON = 3.3V mode operation Jumper OFF = 2.5V mode operation
J4, J6	2.5V to VDD	2.5V DC Power – VDD to DS80PCI800SQ Jumper ON (1-2, 3-4) = 2.5V mode operation Jumper OFF (1-2, 3-4) = 3.3V mode operation
J7	VIN or VDD	Jumper VIH: set 1-2 = VIN (3.3V) or set 2-3 = VDD (2.5V)
J8	SDA, SCL	Optional SMBUS access pins. See the datasheet for additional information on SMBUS.
J9	EEPROM	Optional socket for EEPROM
SW1	EQB[1:0] or AD[3:2]	PIN MODE – EQ control for channel B inputs SMBUS MODE – AD[3:2] device address bits
SW2	ENSMB	ENSMB = LOW – PIN MODE ENSMB = HIGH – SMBUS (slave mode) ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM)
SW3	DEMA[1:0]	PIN MODE – DE control for channel A outputs
SW4	SDA/SCL	“ON” position connects SDA and SCL lines to the device pin.
SW5	DEMB[1:0] or AD[1:0]	PIN MODE – DE control for channel B outputs SMBUS MODE – AD[1:0] device address bits
SW6	SD_TH and LPBK - RES	SD_TH – Signal detect threshold level (FLOAT = Default level) LPBK function for PCI402 and RESERVED for PCI800 (FLOAT = Normal operation)
SW7	VDD_SEL1_2 VDD_SEL3_4	VDD_SEL – Enable or disable the internal 3.3V to 2.5V regulator for U1 and U2. ON connects to GND to enable the internal LDO regulator for 3.3V mode operation.
SW8	READ_EN, RD_EN2, RD_EN3 and RD_EN4	For manual control of loading the external EEPROM and daisy chain the READ_EN to the ALL_DONE pins. Pin1 = ON connects the SW13 push button to the READ_EN of U1. Pin2,3,4 = OFF
SW9	A_D1 to RD_EN2 ... A_D3 to RD_EN4	Pin1 = ON connects the ALL_DONE of U1 to READ_EN of U2. Pin2 = ON connects the ALL_DONE of U2 to READ_EN of U3. Pin3 = ON connects the ALL_DONE of U3 to READ_EN of U4. Pin4 = OFF
SW10	RXDET and RATE	RXDET – Input internal 50 ohm to VDD terminations RXDET = F (AUTO RX Detect), RXDET = 1 (50 ohm input termination). RATE = 0 (GEN1,2) = 2.5G / 5.0G. RATE = R (GEN3) = 8.0G. RATE = F (AUTO Detect). The RATE auto detect circuit requires the idle and active signal which occurs during the link training negotiation.
SW11	EQA[1:0]	PIN MODE – EQ control for channel A inputs



SW12	SDA/SCL to SMCLK/SMDAT	"ON" connect the SDA/SCL bus to the PCIe SMCLK and SMDAT bus. Default is "OFF".
SW13	READ_EN	ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM) SW6: SD_TH becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to "ON" position (pull to GND). To manually control the start, set SW6 to "OFF" position and set SW8 pin1 to "ON" and pin2 to "OFF" position and push the SW13 button for the high to low transition to start the loading. When the loading is complete the LEDs – D1 thru D4 light should turn OFF.
SW14	PRSNT	"ON" connects the PCIe PRSNT signal to the device PRSNT pin. For 16X, set all the switches to the "ON" position.

Quick Start User Guide:

1. Connect J1 – PCIe 16x edge finger to the motherboard (root complex)
2. Connect J2 - PCIe 16x connector to an add-in card (end point).
3. For 3.3V mode operation, set J3 jumper to ON and do not use J4 (leave jumper OFF).
For 2.5V mode operation, set J3 jumper to OFF and set J4 jumper to ON (1-2 and 3-4).
4. Set jumper – J7 for VIH connection to VIN (3.3V) or VDD (2.5V). Default is 1-2 set to ON for VIH = 3.3V.
5. Set SW7 – VDD_SEL1_2 and VDD_SEL3_4 to "ON" position for 3.3V mode operation.
6. Set the control pins for normal operation
 - SW10 – RXDET = F (continuous receiver detection): set switches (3-2-1) = (OFF-OFF-OFF).
RXDET = 1 (50 ohm input termination): set switches (3-2-1) = (OFF-OFF-**ON**).
 - SW10 – RATE = F (enable rate detection): set switches (6-5-4) to (OFF-OFF-OFF).
RATE = R (GEN3 mode): set switches (6-5-4) = (OFF-**ON**-OFF).
RATE = 0 (GEN1,2 mode): set switches (6-5-4) = (**ON**-OFF-OFF).
 - SW6 – SD_TH = F (default signal detect threshold level): set switches (3-2-1) = (OFF-OFF-OFF).
 - SW6 – LPBK - RES = F (normal operation): set switches (6-5-4) = (OFF-OFF-OFF).
 - SW8: Set switches to "OFF" position.
 - SW9: Set switches to "OFF" position.
 - SW14 – PRSNT = GND (enables the device): set switches to "ON" position.

5. Set the input equalization level.

For external pin mode control of the equalization level:
Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:

Set EQB[1:0] with SW1 for the B bank of inputs (top 2 left inputs of DS80PCI800).
SW1 (6-5-4),(3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQB[1:0] = R,R = 14.6 dB at 4 GHz (level 6).
Set EQA[1:0] with SW11 for the A bank of inputs (bottom 2 left inputs of DS80PCI800).
SW8 (6-5-4),(3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQA[1:0] = R,R = 14.6 dB at 4 GHz (level 6).
The table below is the 16 possible EQ settings when in pin mode.

Level	EQA/B[1:0]	SW1 - EQB[1:0] SW11 - EQA[1:0]						EQ (dB) at 4 GHz
		6	5	4	3	2	1	
1	0, 0	ON	OFF	OFF	ON	OFF	OFF	4.9
2	0, R	ON	OFF	OFF	OFF	ON	OFF	7.9
3	0, F	ON	OFF	OFF	OFF	OFF	OFF	9.9
4	0, 1	ON	OFF	OFF	OFF	OFF	ON	11.0
5	R, 0	OFF	ON	OFF	ON	OFF	OFF	14.3
6	R, R	OFF	ON	OFF	OFF	ON	OFF	14.6
7	R, F	OFF	ON	OFF	OFF	OFF	OFF	17.0



8	R,1	OFF	ON	OFF	OFF	OFF	ON	18.5
9	F,0	OFF	OFF	OFF	ON	OFF	OFF	18.0
10	F,R	OFF	OFF	OFF	OFF	ON	OFF	22.0
11	F,F	OFF	OFF	OFF	OFF	OFF	OFF	24.4
12	F,1	OFF	OFF	OFF	OFF	OFF	ON	25.8
13	1,0	OFF	OFF	ON	ON	OFF	OFF	27.4
14	1,R	OFF	OFF	ON	OFF	ON	OFF	29.0
15	1,F	OFF	OFF	ON	OFF	OFF	OFF	31.4
16	1,1	OFF	OFF	ON	OFF	OFF	ON	32.7

6. Set the output VOD and De-emphasis level.

For external pin mode control for the VOD and De-emphasis level (Gen1&2 only):

Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).

SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.

Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:

Set DEMB[1:0] with SW5 for the B bank of outputs (top 2 right outputs of DS80PCI800).

SW5 (6-5-4),(3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMB[1:0] = 0,1 (VOD=1.0V, DE=0 dB).

Set DEMA[1:0] with SW3 for the A bank of outputs (bottom 2 right outputs of DS80PCI800).

SW3 (6-5-4),(3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMA[1:0] = 0,1 (VOD=1.0V, DE=0 dB).

The table below is the 16 possible settings of VOD and DE when in pin mode.

In Gen 1/2, the de-emphasis level can be set with the DEMx[1:0] pins, but is not available in Gen 3.

Level	DEMA/B[1:0]	SW5 - DEMB[1:0] SW3 - DEMA[1:0]						GEN1,2	
		6	5	4	3	2	1	VOD (Vp-p)	DE (dB)
1	0,0	ON	OFF	OFF	ON	OFF	OFF	0.8	0
2	0,R	ON	OFF	OFF	OFF	ON	OFF	0.9	0
3	0,F	ON	OFF	OFF	OFF	OFF	OFF	0.9	-3.5
4	0,1	ON	OFF	OFF	OFF	OFF	ON	1.0	0
5	R,0	OFF	ON	OFF	ON	OFF	OFF	1.0	-3.5
6	R,R	OFF	ON	OFF	OFF	ON	OFF	1.0	-6
7	R,F	OFF	ON	OFF	OFF	OFF	OFF	1.1	0
8	R,1	OFF	ON	OFF	OFF	OFF	ON	1.1	-3.5
9	F,0	OFF	OFF	OFF	ON	OFF	OFF	1.1	-6
10	F,R	OFF	OFF	OFF	OFF	ON	OFF	1.2	0
11	F,F	OFF	OFF	OFF	OFF	OFF	OFF	1.2	-3.5
12	F,1	OFF	OFF	OFF	OFF	OFF	ON	1.2	-6
13	1,0	OFF	OFF	ON	ON	OFF	OFF	1.3	0
14	1,R	OFF	OFF	ON	OFF	ON	OFF	1.3	-3.5
15	1,F	OFF	OFF	ON	OFF	OFF	OFF	1.3	-6
16	1,1	OFF	OFF	ON	OFF	OFF	ON	1.3	-9

For SMBUS mode control of the EQ, VOD and De-emphasis level:

Set ENSMB = 1 (1kohm to VIH) by using the SW2 (3-2-1) = (OFF-OFF-**ON**).

Set SW4 pin1,2 to the ON position so the SMBUS signals are connected.

Set SW3 pin1 thru pin6 switches to the OFF position so they do not connect to the SDA and SCL line.

Set the SW1 and SW5 for the AD[3:0] pins. AD[3:0]=0000 sets device slave address = B0'hex.

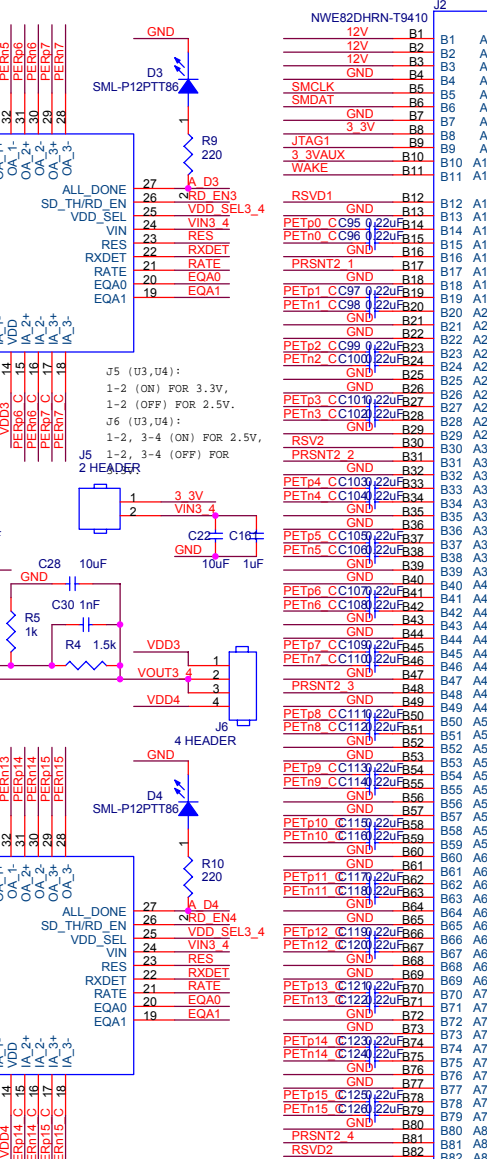
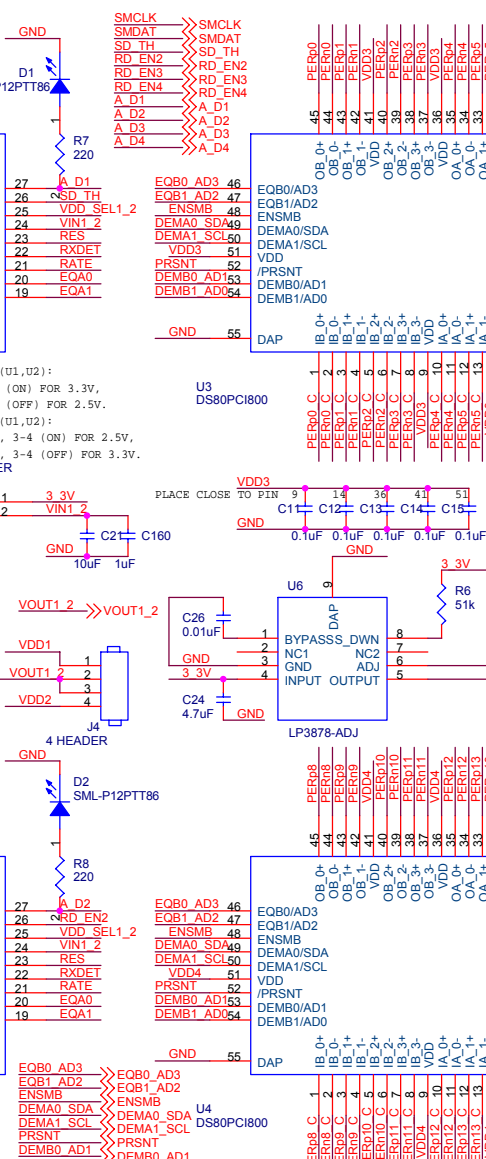
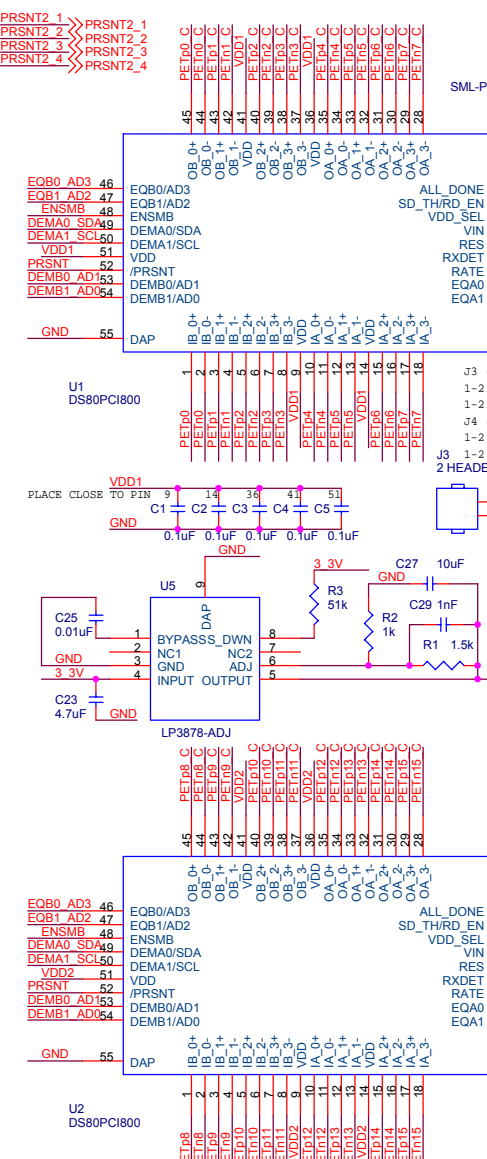
Connect SDA, SCL and GND to J17. Please refer to datasheet for register map for EQ, VOD and DEM.



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12V	B1	B1	A1	A2	PRSN1
12V	B2	B2	A2	A2	12V
12V	B3	B3	A3	A3	12V
GND	B4	B4	A4	GND	
SMCLK	B5	B5	A5	A5	JTAG2
SMDAT	B6	B6	A6	A6	JTAG3
3.3V	B7	B7	A7	A7	JTAG4
JTAG1	B8	B8	A8	A8	JTAG5
3.3VAUX	B10	B10	A10	A10	3.3V
WAKE	B11	B11	A11	A11	PERST
RSVD1	B12	B12	A12	GND	
PETp0 C31	B13	B13	A13	REFCLKp	
PETn0 C36	B14	B14	A14	REFCLKn	
GND	B15	B15	A15	GND	
PRSN2_1	B16	B16	A16	PERP0_C	
GND	B17	B17	A17	PERN0_C	
PETp1 C33	B18	B18	A18	GND	
PETn1 C38	B19	B19	A19	RSVD	
GND	B20	B20	A20	GND	
PETp2 C35	B21	B21	A21	PERP1_C	
PETn2 C36	B22	B22	A22	PERN1_C	
GND	B23	B23	A23	GND	
PETp3 C37	B24	B24	A24	PERP2_C	
PETn3 C38	B25	B25	A25	PERN2_C	
RSV2	B26	B26	A26	GND	
PRSN2_2	B27	B27	A27	GND	
GND	B28	B28	A28	GND	
PETp4 C39	B29	B29	A29	PERP3_C	
PETn4 C40	B30	B30	A30	PERN3_C	
GND	B31	B31	A31	GND	
PRSN2_3	B32	B32	A32	RSVD3	
GND	B33	B33	A33	RSVD4	
PETp5 C41	B34	B34	A34	PERP4_C	
PETn5 C42	B35	B35	A35	PERN4_C	
GND	B36	B36	A36	GND	
PETp6 C43	B37	B37	A37	PERP5_C	
PETn6 C44	B38	B38	A38	PERN5_C	
GND	B39	B39	A39	GND	
PETp7 C45	B40	B40	A40	PERP6_C	
PETn7 C46	B41	B41	A41	PERN6_C	
PRSN2_4	B42	B42	A42	GND	
GND	B43	B43	A43	GND	
PETp8 C47	B44	B44	A44	PERP7_C	
PETn8 C48	B45	B45	A45	PERN7_C	
GND	B46	B46	A46	GND	
PRSN2_5	B47	B47	A47	GND	
GND	B48	B48	A48	GND	
PETp9 C49	B49	B49	A49	PERP8_C	
PETn9 C50	B50	B50	A50	PERN8_C	
GND	B51	B51	A51	GND	
PETp10 C51	B52	B52	A52	PERP9_C	
PETn10 C52	B53	B53	A53	PERN9_C	
GND	B54	B54	A54	GND	
PETp11 C53	B55	B55	A55	PERP10_C	
PETn11 C54	B56	B56	A56	PERN10_C	
GND	B57	B57	A57	GND	
PETp12 C55	B58	B58	A58	PERP11_C	
PETn12 C56	B59	B59	A59	PERN11_C	
GND	B60	B60	A60	GND	
PETp13 C57	B61	B61	A61	PERP12_C	
PETn13 C58	B62	B62	A62	PERN12_C	
GND	B63	B63	A63	GND	
PETp14 C59	B64	B64	A64	PERP13_C	
PETn14 C60	B65	B65	A65	PERN13_C	
GND	B66	B66	A66	GND	
PETp15 C61	B67	B67	A67	PERP14_C	
PETn15 C62	B68	B68	A68	PERN14_C	
GND	B69	B69	A69	GND	
PRSN2_6	B70	B70	A70	PERP15_C	
RSVD2	B71	B71	A71	PERN15_C	
B82	B82	B82	A82	GND	



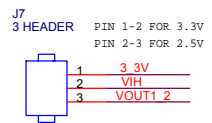
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12V	B3	B3	A3	A3	12V
GND	B4	B4	A4	GND	
SMCLK	B5	B5	A5	A5	JTAG2
SMDAT	B6	B6	A6	A6	JTAG3
3.3V	B7	B7	A7	A7	JTAG4
JTAG1	B8	B8	A8	A8	JTAG5
3.3VAUX	B10	B10	A10	A10	3.3V
WAKE	B11	B11	A11	A11	PERST
RSVD1	B12	B12	A12	GND	
PETp0 C95	B13	B13	A13	REFCLKp	
PETn0 C96	B14	B14	A14	REFCLKn	
GND	B15	B15	A15	GND	
PRSN2_1	B16	B16	A16	PERP0_C	
GND	B17	B17	A17	PERN0_C	
PETp1 C97	B18	B18	A18	GND	
PETn1 C98	B19	B19	A19	RSVD	
GND	B20	B20	A20	GND	
PETp2 C99	B21	B21	A21	PERP1_C	
PETn2 C100	B22	B22	A22	PERN1_C	
GND	B23	B23	A23	GND	
PETp3 C101	B24	B24	A24	PERP2_C	
PETn3 C102	B25	B25	A25	PERN2_C	
GND	B26	B26	A26	GND	
PETp4 C103	B27	B27	A27	PERP3_C	
PETn4 C104	B28	B28	A28	PERN3_C	
GND	B29	B29	A29	GND	
RSV2	B30	B30	A30	GND	
PRSN2_2	B31	B31	A31	GND	
GND	B32	B32	A32	GND	
PETp5 C105	B33	B33	A33	PERP4_C	
PETn5 C106	B34	B34	A34	PERN4_C	
GND	B35	B35	A35	GND	
PETp6 C107	B36	B36	A36	PERP5_C	
PETn6 C108	B37	B37	A37	PERN5_C	
GND	B38	B38	A38	GND	
PETp7 C109	B39	B39	A39	PERP6_C	
PETn7 C110	B40	B40	A40	PERN6_C	
GND	B41	B41	A41	GND	
PETp8 C111	B42	B42	A42	PERP7_C	
PETn8 C112	B43	B43	A43	PERN7_C	
GND	B44	B44	A44	GND	
PRSN2_3	B45	B45	A45	GND	
GND	B46	B46	A46	GND	
PETp9 C113	B47	B47	A47	PERP8_C	
PETn9 C114	B48	B48	A48	PERN8_C	
GND	B49	B49	A49	GND	
PETp10 C115	B50	B50	A50	PERP9_C	
PETn10 C116	B51	B51	A51	PERN9_C	
GND	B52	B52	A52	GND	
PETp11 C117	B53	B53	A53	PERP10_C	
PETn11 C118	B54	B54	A54	PERN10_C	
GND	B55	B55	A55	GND	
PETp12 C119	B56	B56	A56	PERP11_C	
PETn12 C120	B57	B57	A57	PERN11_C	
GND	B58	B58	A58	GND	
PETp13 C121	B59	B59	A59	PERP12_C	
PETn13 C122	B60	B60	A60	PERN12_C	
GND	B61	B61	A61	GND	
PETp14 C123	B62	B62	A62	PERP13_C	
PETn14 C124	B63	B63	A63	PERN13_C	
GND	B64	B64	A64	GND	
PETp15 C125	B65	B65	A65	PERP14_C	
PETn15 C126	B66	B66	A66	PERN14_C	
GND	B67	B67	A67	GND	
PRSN2_4	B68	B68	A68	PERP15_C	
RSVD2	B69	B69	A69	PERN15_C	
B82	B82	B82	A82	GND	

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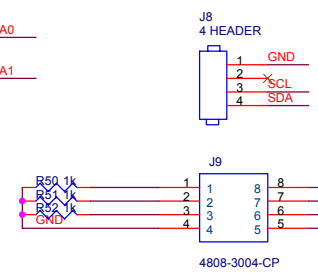
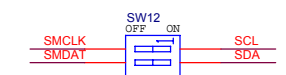
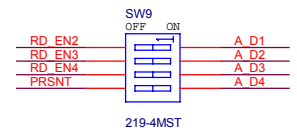
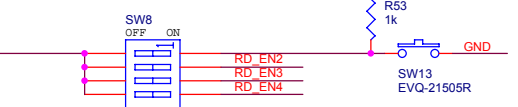
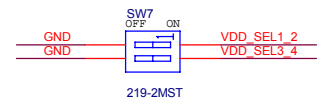
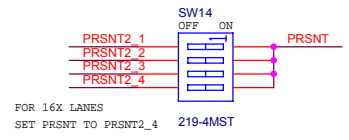
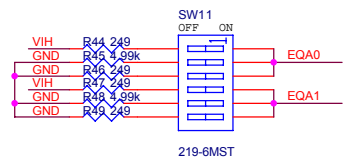
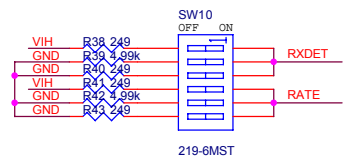
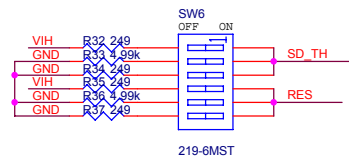
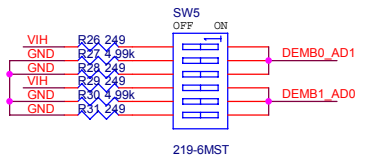
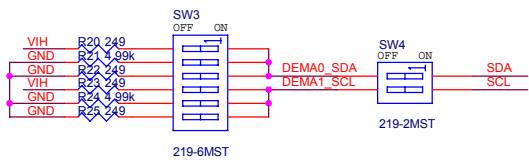
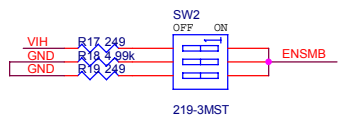
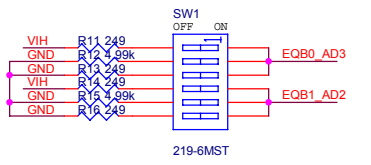
EQB0_AD3 >> EQB0_AD3
 EQB1_AD2 >> EQB1_AD2
 ENSMB >> ENSMB
 DEMA0_SDA >> DEMA0_SDA
 DEMA1_SCL >> DEMA1_SCL
 PRSNT >> PRSNT
 DEMB0_AD1 >> DEMB0_AD1
 DEMB1_AD0 >> DEMB1_AD0
 EQA1 >> EQA1
 EQA0 >> EQA0
 RATE >> RATE
 RXDET >> RXDET
 RES >> RES
 VDD_SEL1_2 >> VDD_SEL1_2
 VDD_SEL3_4 >> VDD_SEL3_4
 VOUT1_2 >> VOUT1_2
 3.3V >> 3.3V

SMCLK >> SMCLK
 SMDAT >> SMDAT
 SD_TH >> SD_TH
 RD_EN2 >> RD_EN2
 RD_EN3 >> RD_EN3
 RD_EN4 >> RD_EN4
 A_D1 >> A_D1
 A_D2 >> A_D2
 A_D3 >> A_D3
 A_D4 >> A_D4

PRSNT2_1 >> PRSNT2_1
 PRSNT2_2 >> PRSNT2_2
 PRSNT2_3 >> PRSNT2_3
 PRSNT2_4 >> PRSNT2_4



PLACE ALL Rs CLOSE TO SW
 SW IN THE OFF POSITION = OPEN



PIN MODE SETTINGS:
 SW1 - EQB0, EQB1
 SW2 - ENSMB = 1K TO GND
 SW3 - DEMA0, DEMA1
 SW4 - OFF POSITION
 SW5 - DEMB0, DEMB1
 SW6 - SD_TH, RES
 SW7 - ON (GND) FOR 3.3V
 SW8 - RD_EN2-4=ON (SD_TH)
 SW9 - OFF POSITION
 SW10 - RXDET, RATE
 SW11 - EQA0, EQA1
 SW12 - OFF POSITION
 SW13 - OFF POSITION
 SW14 - PRSNT2_4=ON

SMBUS SLAVE MODE SETTINGS:
 SW1 - AD3, AD2
 SW2 - ENSMB = 1K TO VDD
 SW3 - OFF POSITION
 SW4 - ON POSITION (SDA, SCL)
 SW5 - AD1, AD0
 SW6 - SD_TH, RES
 SW7 - ON (GND) FOR 3.3V
 SW8 - RD_EN2-4=ON (SD_TH)
 SW9 - OFF POSITION
 SW10 - RXDET, RATE
 SW11 - EQA0, EQA1
 SW12 - OFF POSITION WHEN USING SPA BOARD
 SW13 - OFF POSITION
 SW14 - PRSNT2_4=ON

SMBUS MASTER (READ EEPROM) MODE SETTINGS:
 SW1 - AD3, AD2
 SW2 - ENSMB = FLOAT
 SW3 - OFF POSITION
 SW4 - ON POSITION (SDA, SCL)
 SW5 - AD1, AD0
 SW6 - OFF POSITION
 SW7 - ON (GND) FOR 3.3V
 SW8 - SD_TH=ON, RD_EN2-4=OFF
 SW9 - ON POSITION (ALL_DONE TO RD_EN, ALL_DONE4 TO PRSNT)
 SW10 - RXDET, RATE
 SW11 - EQA0, EQA1
 SW12 - OFF POSITION
 SW13 - GND TO START THE READ PROCESS
 SW14 - OFF POSITION

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