

Automotive-grade N-channel 400 V, 0.063 Ω typ., 38 A MDmesh™ DM2 Power MOSFET in a D²PAK package

Datasheet - production data

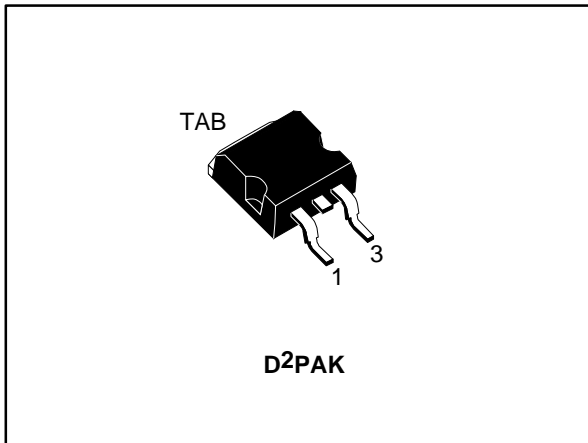
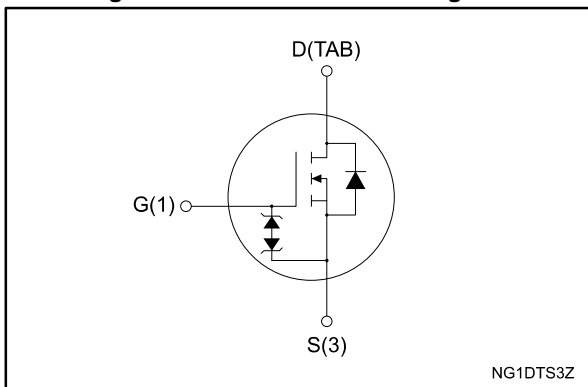


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB45N40DM2AG	400 V	0.072 Ω	38 A	250 W

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB45N40DM2AG	45N40DM2	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _{case} = 25 °C	38	A
	Drain current (continuous) at T _{case} = 100 °C	24	
I _{DM} ⁽¹⁾	Drain current (pulsed)	152	A
P _{TOT}	Total dissipation at T _{case} = 25 °C	250	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	50	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Operating junction temperature		

Notes:

(1) Pulse width is limited by safe operating area.

(2) I_{SD} ≤ 38 A, di/dt=800 A/μs; V_{DS} peak < V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}.

(3) V_{DS} ≤ 320 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR} ⁽¹⁾	Avalanche current, repetitive or not repetitive	7	A
E _{AS} ⁽²⁾	Single pulse avalanche energy	1100	mJ

Notes:

(1) pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	400			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 400\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 400\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 19\text{ A}$		0.063	0.072	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	2600	-	pF
C_{oss}	Output capacitance		-	180	-	
C_{rss}	Reverse transfer capacitance		-	3.5	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }320\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	300	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 320\text{ V}$, $I_{\text{D}} = 38\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	56	-	nC
Q_{gs}	Gate-source charge		-	13	-	
Q_{gd}	Gate-drain charge		-	28	-	

Notes:

(1) $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 200\text{ V}$, $I_{\text{D}} = 19\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	20	-	ns
t_{r}	Rise time		-	6.7	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	68	-	
t_{f}	Fall time		-	9.8	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 38\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	95		ns
Q_{rr}	Reverse recovery charge		-	0.4		μC
I_{RRM}	Reverse recovery current		-	8.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	185		ns
Q_{rr}	Reverse recovery charge		-	1.62		μC
I_{RRM}	Reverse recovery current		-	17.5		A

Notes:

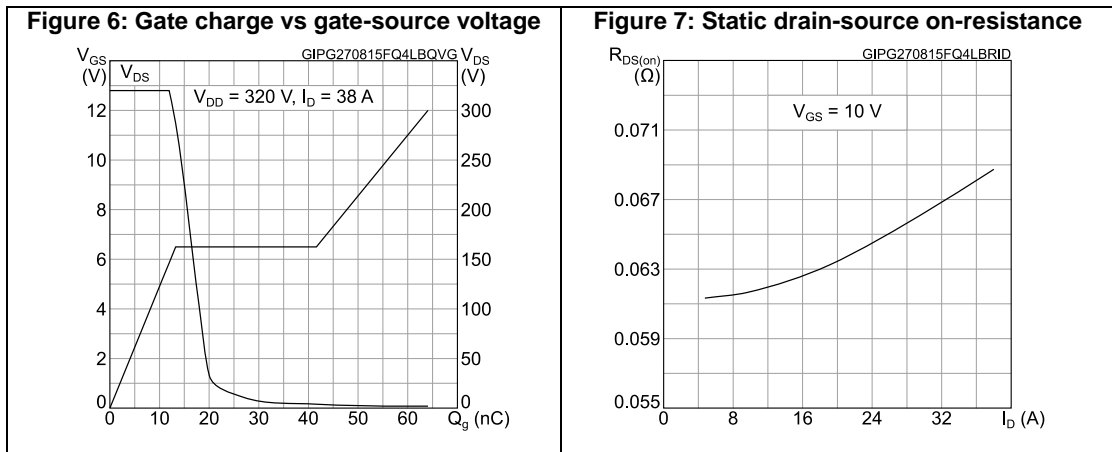
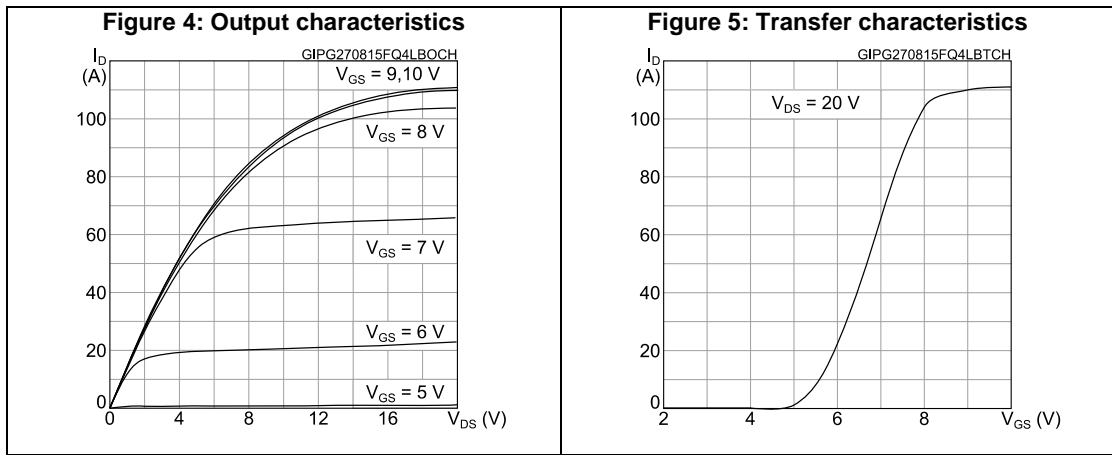
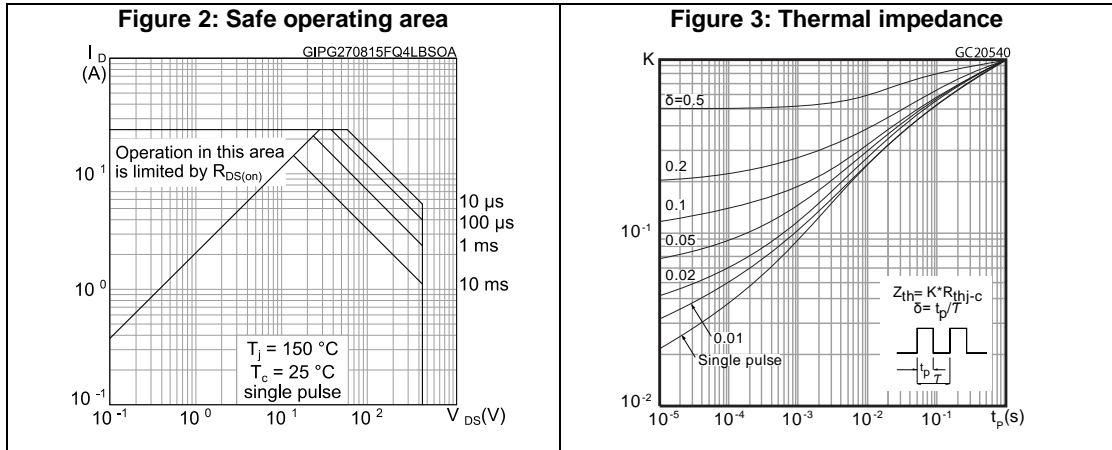
- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

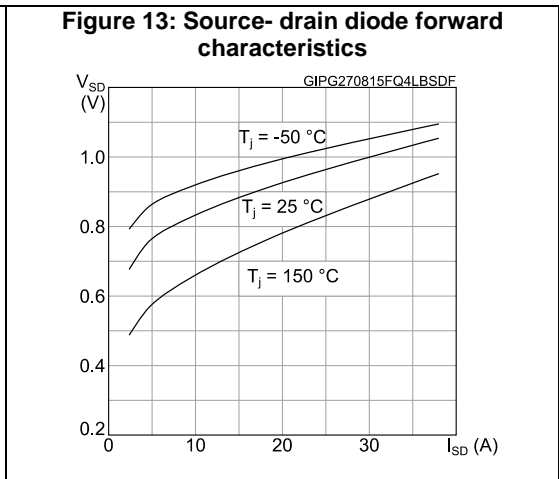
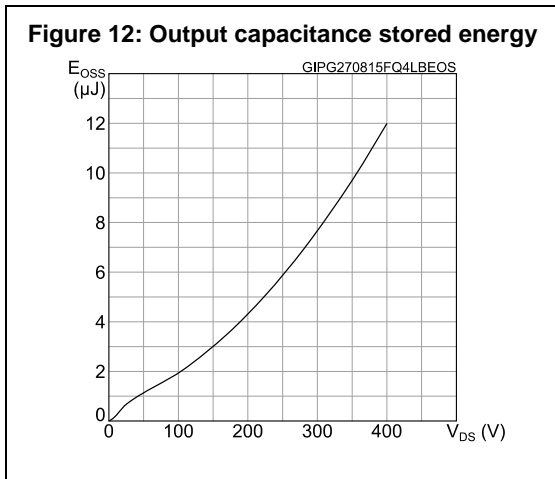
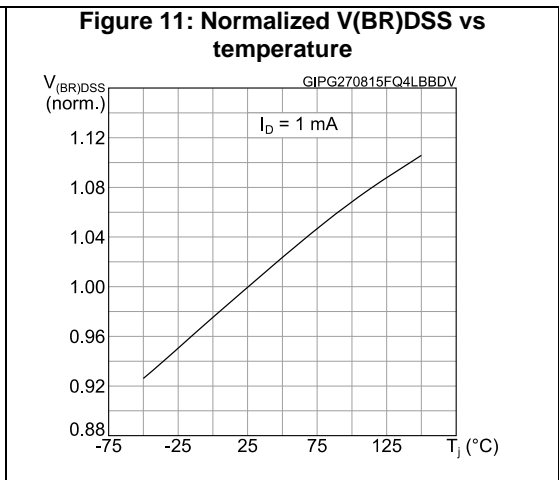
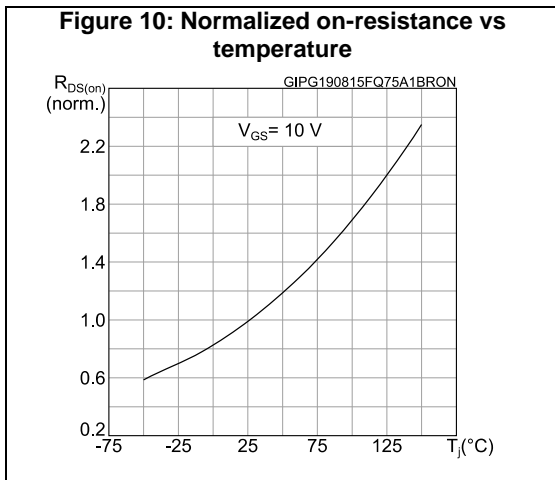
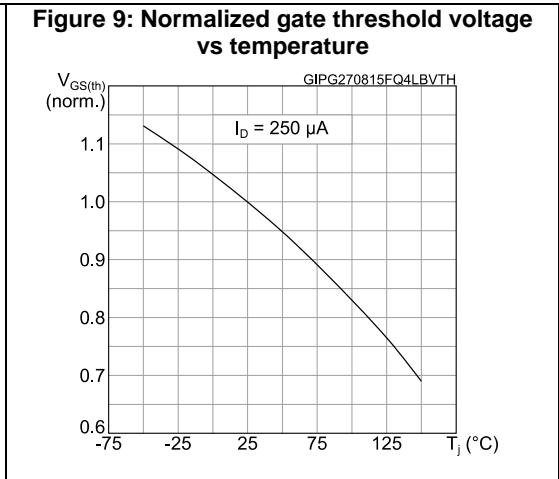
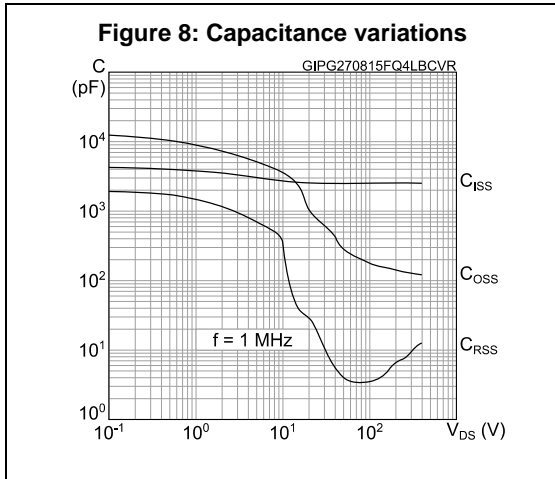
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250\text{ }\mu\text{A}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

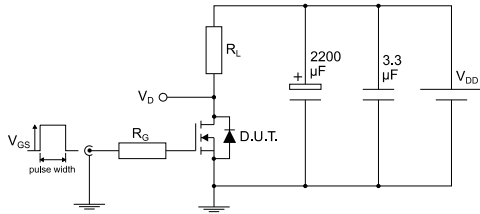
2.1 Electrical characteristics (curves)





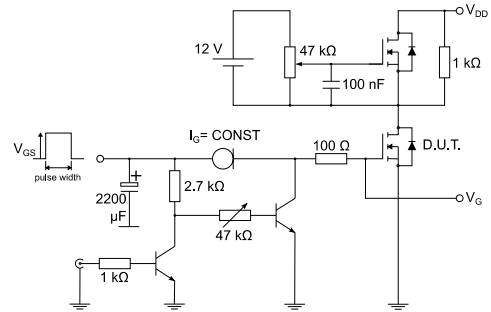
3 Test circuits

Figure 14: Test circuit for resistive load switching times



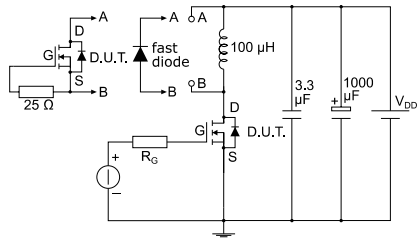
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Figure 15: Test circuit for gate charge behavior



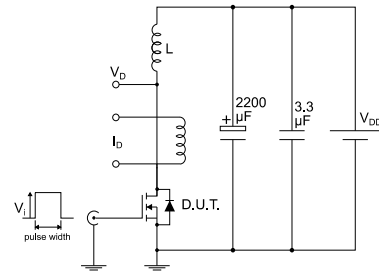
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Figure 16: Test circuit for inductive load switching and diode recovery times



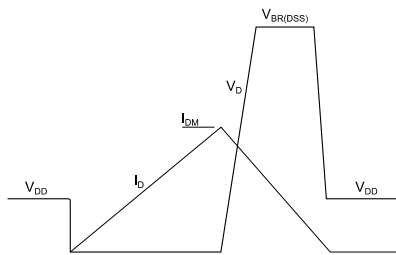
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Figure 17: Unclamped inductive load test circuit



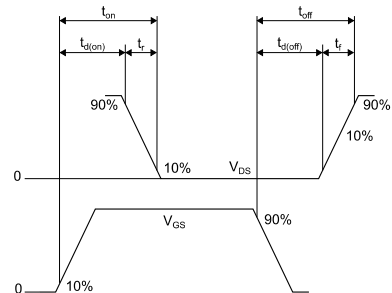
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 20: D²PAK (TO-263) type A package outline

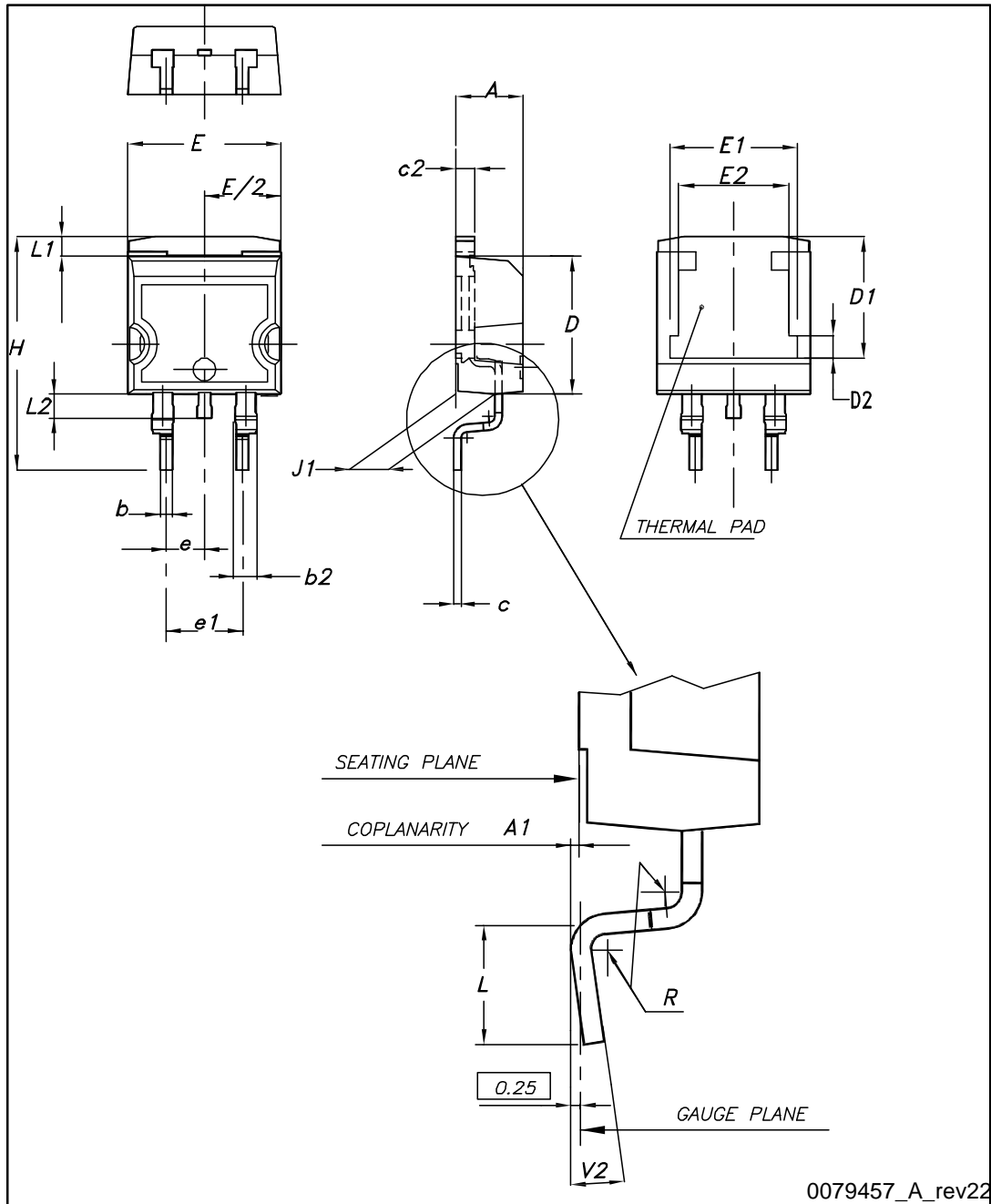
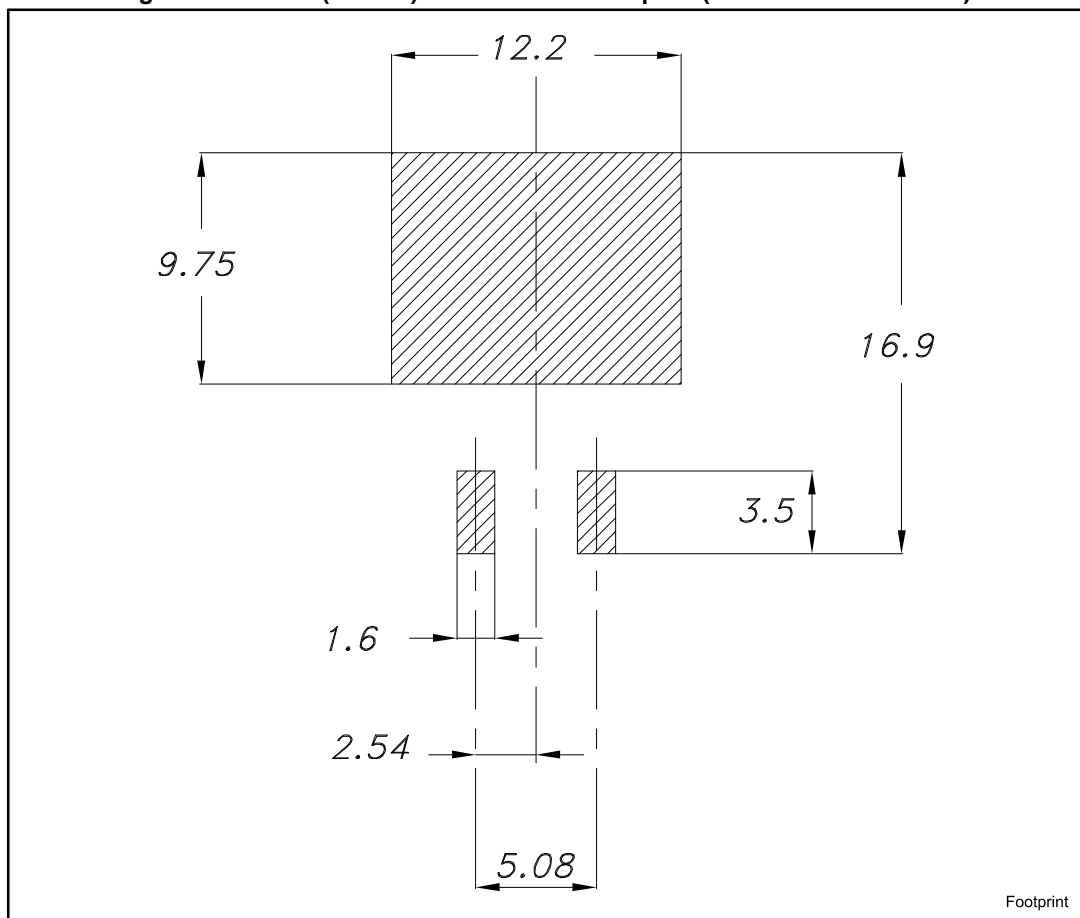


Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D²PAK packing information

Figure 22: Tape

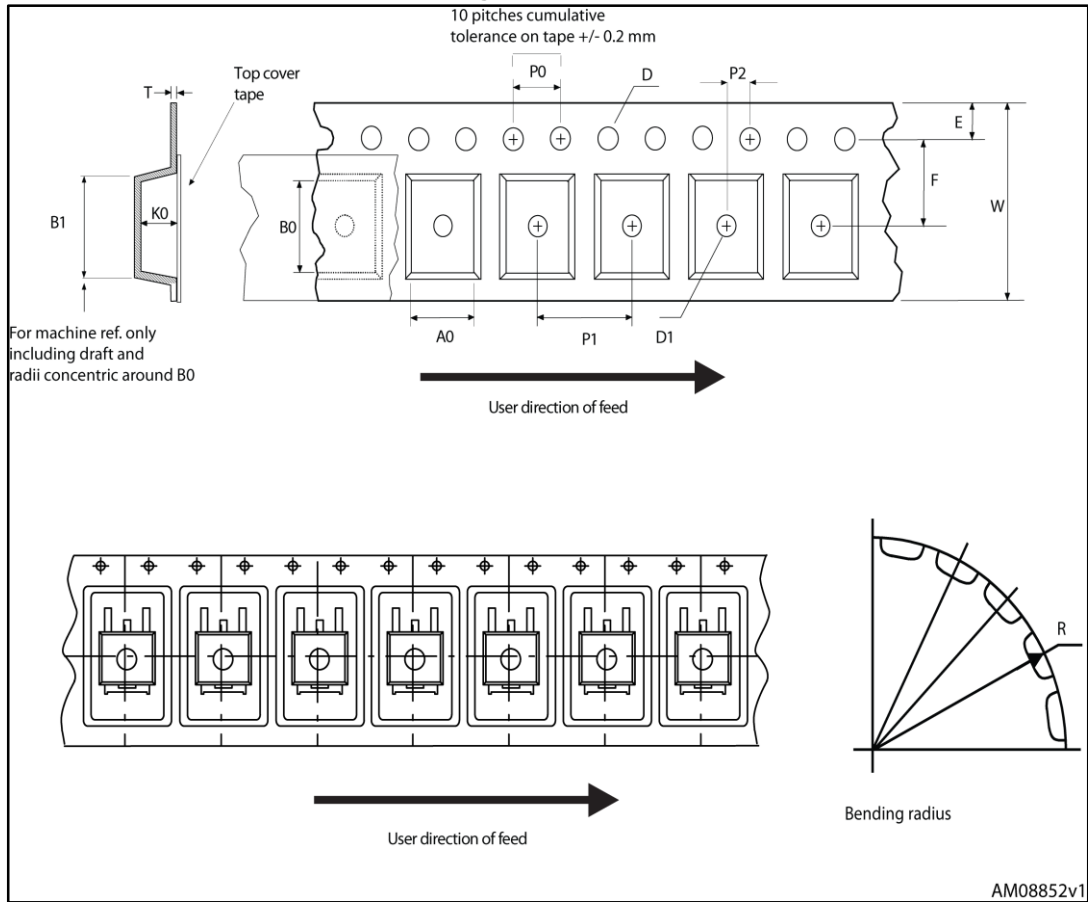


Figure 23: Reel

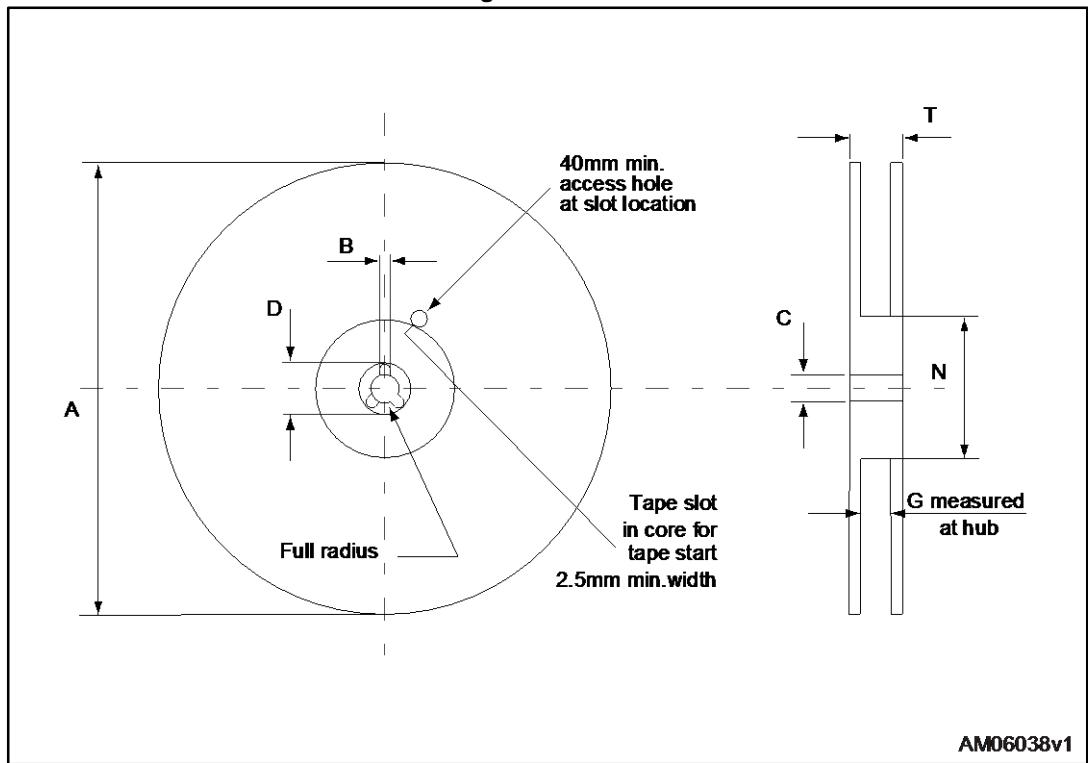


Table 11: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
27-Aug-2015	1	Initial version

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