

Single-Channel: 6N138, 6N139 Dual-Channel: HCPL2730, HCPL2731 Low Input Current High Gain Split Darlington Optocouplers

Features

- Low current – 0.5mA
- Superior CTR-2000%
- Superior CMR-10kV/μs
- CTR guaranteed 0–70°C
- U.L. recognized (File # E90700)
- VDE recognized (File # 120915) Ordering option V, e.g., 6N138V
- Dual Channel – HCPL2730, HCPL2731

Applications

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver

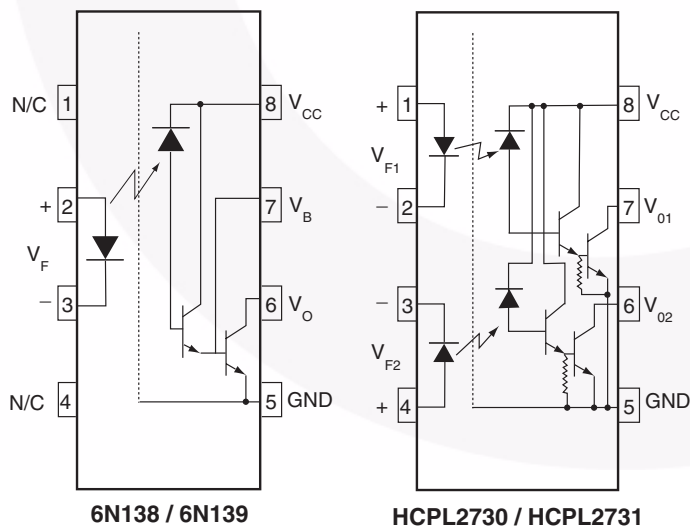
Description

The 6N138/9 and HCPL2730/HCPL2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

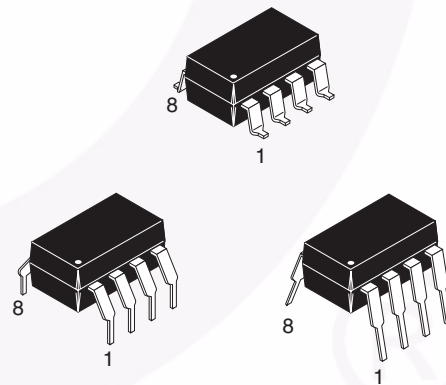
The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730/HCPL2731, an integrated emitter-base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/μs.

Schematic



Package Outlines



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Value | Units |
|-----------------|---|-----------------|----------------|------------------|
| T_{STG} | Storage Temperature | | -55 to +125 | $^\circ\text{C}$ |
| T_{OPR} | Operating Temperature | | -40 to +85 | $^\circ\text{C}$ |
| T_{SOL} | Lead Solder Temperature (Wave solder only. See recommended reflow profile graph for SMD mounting) | | 260 for 10 sec | $^\circ\text{C}$ |
| EMITTER | | | | |
| I_F (avg) | DC/Average Forward Input Current | Each Channel | 20 | mA |
| I_F (pk) | Peak Forward Input Current (50% duty cycle, 1 ms P.W.) | Each Channel | 40 | mA |
| I_F (trans) | Peak Transient Input Current - ($\leq 1\mu\text{s}$ P.W., 300 pps) | | 1.0 | A |
| V_R | Reverse Input Voltage | Each Channel | 5 | V |
| P_D | Input Power Dissipation | Each Channel | 35 | mW |
| DETECTOR | | | | |
| I_O (avg) | Average Output Current | Each Channel | 60 | mA |
| V_{ER} | Emitter-Base Reverse Voltage | 6N138 and 6N139 | 0.5 | V |
| V_{CC}, V_O | Supply Voltage, Output Voltage | 6N138, HCPL2730 | -0.5 to 7 | V |
| | | 6N139, HCPL2731 | -0.5 to 18 | |
| P_O | Output Power Dissipation | Each Channel | 100 | mW |

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)**Individual Component Characteristics**

| Symbol | Parameter | Test Conditions | Device | Min. | Typ.* | Max. | Unit |
|---------------------------|--|--|--------------|------|-------|------|----------------------|
| EMITTER | | | | | | | |
| V_F | Input Forward Voltage | $T_A = 25^\circ\text{C}$ | All | | 1.30 | 1.7 | V |
| | | Each channel ($I_F = 1.6\text{mA}$) | | | | 1.75 | |
| BV_R | Input Reverse Breakdown Voltage | $T_A = 25^\circ\text{C}$, $I_R = 10\mu\text{A}$ | All | 5.0 | 20 | | V |
| $\Delta V_F / \Delta T_A$ | Temperature Coefficient of Forward Voltage | $I_F = 1.6\text{mA}$ | All | | -1.8 | | mV/ $^\circ\text{C}$ |
| DETECTOR | | | | | | | |
| I_{OH} | Logic HIGH Output Current | $I_F = 0\text{mA}$, $V_O = V_{CC} = 18\text{V}$ | 6N139 | | 0.01 | 100 | μA |
| | | Each Channel | HCPL2731 | | | | |
| | | $I_F = 0\text{mA}$, $V_O = V_{CC} = 7\text{V}$ | 6N138 | | 0.01 | 250 | |
| | | Each Channel | HCPL2730 | | | | |
| I_{CCL} | Logic LOW supply | $I_F = 1.6\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 18\text{V}$ | 6N138, 6N139 | | 0.4 | 1.5 | mA |
| | | $I_{F1} = I_{F2} = 1.6\text{mA}$, $V_{CC} = 18\text{V}$ | HCPL2731 | | 1.3 | 3 | |
| | | $V_{O1} - V_{O2} = \text{Open}$, $V_{CC} = 7\text{V}$ | HCPL2730 | | | | |
| I_{CCH} | Logic HIGH Supply | $I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 18\text{V}$ | 6N138, 6N139 | | 0.05 | 10 | μA |
| | | $I_{F1} = I_{F2} = 0\text{mA}$, $V_{CC} = 18\text{V}$ | HCPL2731 | | 0.10 | 20 | |
| | | $V_{O1} - V_{O2} = \text{Open}$, $V_{CC} = 7\text{V}$ | HCPL2730 | | | | |

Transfer Characteristics

| Symbol | Parameter | Test Conditions | Device | Min. | Typ.* | Max. | Unit |
|--|--|---|----------|------|-------|------|------|
| COUPLED | | | | | | | |
| CTR | Current Transfer Ratio ⁽¹⁾⁽²⁾ | $I_F = 0.5\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC} = 4.5\text{V}$ | 6N139 | 400 | 1100 | | % |
| | | Each Channel | HCPL2731 | | 3500 | | |
| | | $I_F = 1.6\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC} = 4.5\text{V}$ | 6N139 | 500 | 1300 | | |
| | | Each Channel | HCPL2731 | | 2500 | | |
| | | $I_F = 1.6\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC} = 4.5\text{V}$ | 6N138 | 300 | 1300 | | |
| | | Each Channel | HCPL2730 | | 2500 | | |
| V_{OL} | Logic LOW Output Voltage ⁽²⁾ | $I_F = 0.5\text{mA}$, $I_O = 2\text{mA}$, $V_{CC} = 4.5\text{V}$ | 6N139 | | 0.08 | 0.4 | V |
| | | $I_F = 1.6\text{mA}$, $I_O = 8\text{mA}$, $V_{CC} = 4.5\text{V}$ | 6N139 | | 0.01 | 0.4 | |
| | | Each Channel | HCPL2731 | | | | |
| | | $I_F = 0.5\text{mA}$, $I_O = 15\text{mA}$, $V_{CC} = 4.5\text{V}$ | 6N139 | | 0.13 | 0.4 | |
| | | Each Channel | HCPL2731 | | | | |
| | | $I_F = 12\text{mA}$, $I_O = 24\text{mA}$, $V_{CC} = 4.5\text{V}$ | 6N139 | | 0.20 | 0.4 | |
| | | Each Channel | HCPL2731 | | | | |
| $I_F = 1.6\text{mA}$, $I_O = 4.8\text{mA}$, $V_{CC} = 4.5\text{V}$ | 6N138 | | 0.10 | 0.4 | | | |
| Each Channel | HCPL2730 | | | | | | |

*All Typical at $T_A = 25^\circ\text{C}$

Electrical Characteristics (Continued) ($T_A = 0$ to 70°C unless otherwise specified)

Switching Characteristics ($V_{CC} = 5\text{V}$)

| Symbol | Parameter | Test Conditions | Device | Min. | Typ.* | Max. | Unit |
|-----------|---|---|----------------------|-------|--------|------|------------------------|
| T_{PHL} | Propagation Delay Time to Logic LOW ⁽²⁾ (Fig. 24) | $R_L = 4.7\Omega, I_F = 0.5\text{mA}$ | 6N139 | | | 30 | μs |
| | | $T_A = 25^\circ\text{C}$ | | | 4 | 25 | |
| | | $R_L = 4.7\Omega, I_F = 0.5\text{mA}$ | HCPL2731 | | | 120 | |
| | | Each Channel $T_A = 25^\circ\text{C}$ | | | 3 | 100 | |
| | | $R_L = 270\Omega, I_F = 12\text{mA}$ | 6N139 | | | 2 | |
| | | $T_A = 25^\circ\text{C}$ | | | 0.2 | 1 | |
| | | $R_L = 270\Omega, I_F = 12\text{mA}$, Each Channel $T_A = 25^\circ\text{C}$ | HCPL2730 HCPL2731 | | 0.3 | 2 | |
| T_{PLH} | Propagation Delay Time to Logic HIGH ⁽²⁾ (Fig. 24) | $R_L = 4.7\Omega, I_F = 0.5\text{mA}$ | 6N139 | | | 90 | μs |
| | | Each Channel | HCPL2731 | | | | |
| | | $R_L = 4.7\Omega, I_F = 0.5\text{mA}, T_A = 25^\circ\text{C}$ | 6N139 | | 12 | 60 | |
| | | Each Channel | HCPL2731 | | 22 | | |
| | | $R_L = 270\Omega, I_F = 12\text{mA}$ | 6N139 | | | 10 | |
| | | $T_A = 25^\circ\text{C}$ | | | 1.3 | 7 | |
| | | $R_L = 270\Omega, I_F = 12\text{mA}$, Each Channel $T_A = 25^\circ\text{C}$ | HCPL2730 HCPL2731 | | 5 | 10 | |
| ICM_H | Common Mode Transient Immunity at Logic HIGH ⁽³⁾ (Fig. 25) | $I_F = 0\text{mA}, V_{CM} = 10V_{P-P}, T_A = 25^\circ\text{C}, R_L = 2.2\Omega$ | 6N138 6N139 | 1,000 | 10,000 | | $\text{V}/\mu\text{s}$ |
| | | Each Channel | HCPL2730 HCPL2731 | | | | |
| | | $R_L = 2.2\Omega, I_F = 1.6\text{mA}$ | 6N138 | | | 50 | |
| | | Each Channel | HCPL2730/1 | | | | |
| ICM_L | Common Mode Transient Immunity at Logic LOW ⁽³⁾ (Fig. 25) | $(I_F = 1.6\text{mA}, V_{CM} = 10V_{P-P}, R_L = 2.2\Omega)$ | 6N138 6N139 | 1,000 | 10,000 | | $\text{V}/\mu\text{s}$ |
| | | $T_A = 25^\circ\text{C}$ | | | 7 | 35 | |
| | | Each Channel | HCPL2730 HCPL2731 | | 16 | | |

** All Typical at $T_A = 25^\circ\text{C}$

Electrical Characteristics (Continued) ($T_A = 0$ to 70°C unless otherwise specified)**Isolation Characteristics**

| Symbol | Characteristics | Test Conditions | Min. | Typ.* | Max. | Unit |
|-----------|--|---|------|-----------|------|------------------|
| I_{I-O} | Input-Output Insulation Leakage Current ⁽⁴⁾ | Relative humidity = 45%, $T_A = 25^\circ\text{C}$, $t = 5\text{s}$, $V_{I-O} = 3000\text{VDC}$ | | | 1.0 | μA |
| V_{ISO} | Withstand Insulation Test Voltage ⁽⁴⁾ | $\text{RH} \leq 50\%$, $T_A = 25^\circ\text{C}$, $I_{I-O} \leq 2\mu\text{A}$, $t = 1\text{ min.}$ | 2500 | | | V_{RMS} |
| R_{I-O} | Resistance (Input to Output) ⁽⁴⁾ | $V_{I-O} = 500\text{VDC}$ | | 10^{12} | | Ω |
| C_{I-O} | Capacitance (Input to Output) ⁽⁴⁾⁽⁵⁾ | $f = 1\text{MHz}$ | | 0.6 | | pF |
| I_{I-I} | Input-Input Insulation Leakage Current ⁽⁶⁾ | $\text{RH} \leq 45\%$, $V_{I-I} = 500\text{VDC}$, $t = 5\text{s}$, HCPL2730/2731 only | | 0.005 | | μA |
| R_{I-I} | Input-Input Resistance ⁽⁶⁾ | $V_{I-I} = 500\text{VDC}$, HCPL2730/2731 only | | 10^{11} | | Ω |
| C_{I-I} | Input-Input Capacitance ⁽⁶⁾ | $f = 1\text{MHz}$, HCPL2730/2731 only | | 0.03 | | pF |

*All Typicals at $T_A = 25^\circ\text{C}$ **Notes:**

- Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
- Pin 7 open. (6N138 and 6N139 only)
- Common mode transient immunity in logic HIGH level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic HIGH state (i.e., $V_O > 2.0\text{V}$). Common mode transient immunity in logic LOW level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic LOW state (i.e., $V_O < 0.8\text{V}$).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- For dual channel devices, C_{I-O} is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Electrical Characteristics (Continued) $T_A = 25^\circ\text{C}$ unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} - V_{OLX} (@ I_L - I_2)}{I_L}$$

Where:

V_{DD1} = Input Supply Voltage

V_{DD2} = Output Supply Voltage

V_{DF} = Diode Forward Voltage

V_{OL1} = Logic "0" Voltage of Driver

V_{OH1} = Logic "1" Voltage of Driver

I_F = Diode Forward Current

V_{OLX} = Saturation Voltage of Output Transistor

I_L = Load Current Through Resistor R2

I_2 = Input Current of Output Gate

| INPUT | | R1 (V) | OUTPUT | | | | | | |
|------------|----------|--------|-----------|------------|--------|--------|--------|--------|--------|
| | | | CMOS @ 5V | CMOS @ 10V | 74XX | 74LXX | 74SXX | 74LSXX | 74HXX |
| | | | R2 (V) | R2 (V) | R2 (V) | R2 (V) | R2 (V) | R2 (V) | R2 (V) |
| CMOS @ 5V | NON-INV. | 2000 | 1000 | 2200 | 750 | 1000 | 1000 | 1000 | 560 |
| | INV. | 510 | | | | | | | |
| CMOS @ 10V | NON-INV. | 5100 | | | | | | | |
| | INV. | 4700 | | | | | | | |
| 74XX | NON-INV. | 2200 | | | | | | | |
| | INV. | 180 | | | | | | | |
| 74LXX | NON-INV. | 1800 | | | | | | | |
| | INV. | 100 | | | | | | | |
| 74SXX | NON-INV. | 2000 | | | | | | | |
| | INV. | 360 | | | | | | | |
| 74LSXX | NON-INV. | 2000 | | | | | | | |
| | INV. | 180 | | | | | | | |
| 74HXX | NON-INV. | 2000 | | | | | | | |
| | INV. | 180 | | | | | | | |

Fig. 1 Resistor Values for Logic Interface

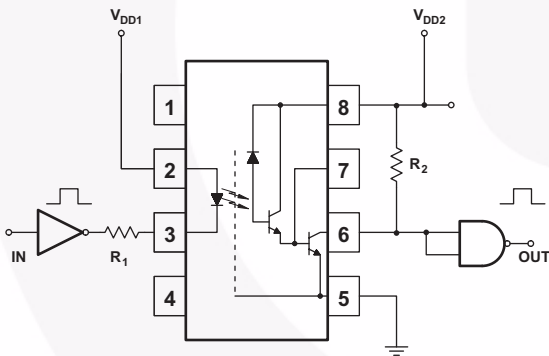


Fig. 2 Non-Inverting Logic Interface

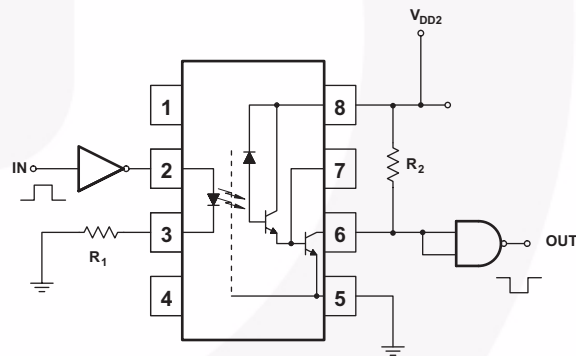


Fig. 3 Inverting Logic Interface

Typical Performance Curves

Fig. 4 LED Forward Current vs. Forward Voltage

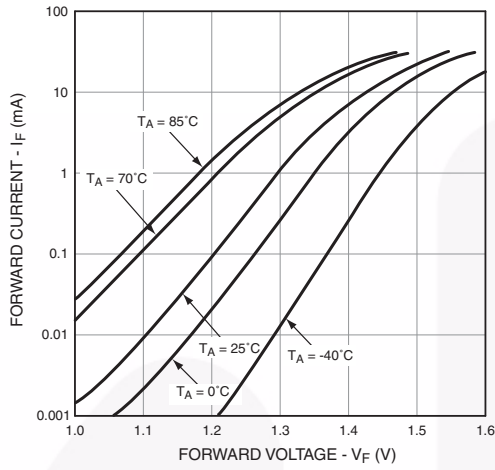


Fig. 5 LED Forward Voltage vs. Temperature

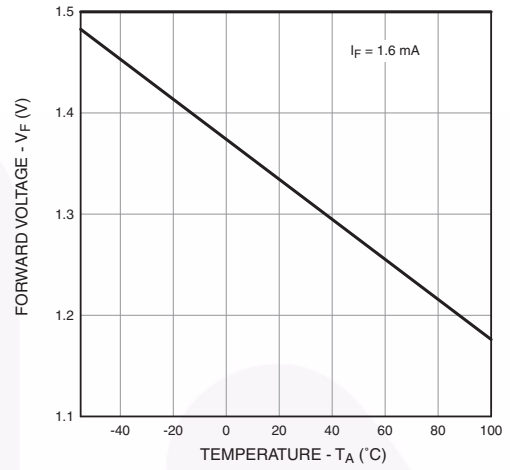


Fig. 6 Non-saturated Rise and Fall Times vs. Load Resistance (6N138 / 6N139 Only)

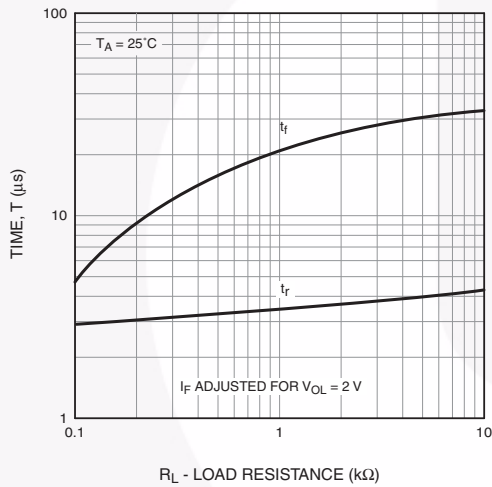


Fig. 7 Non-saturated Rise and Fall Times vs. Load Resistance (HCPL2730 / HCPL2731 Only)

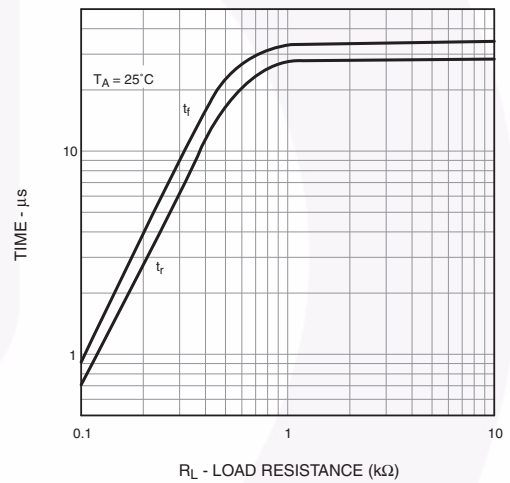


Fig. 8 Propagation Delay To Logic Low vs. Base-Emitter Resistance (HCPL2730 / HCPL2731 Only)

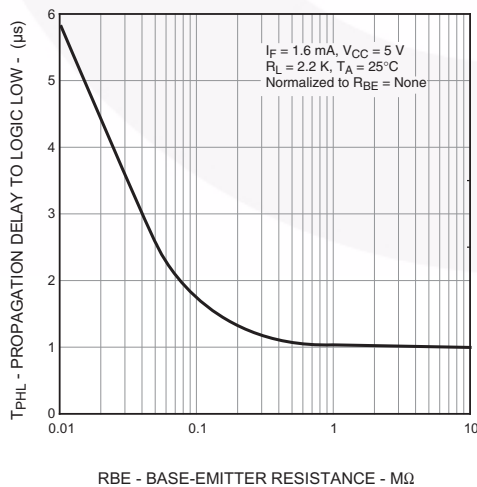
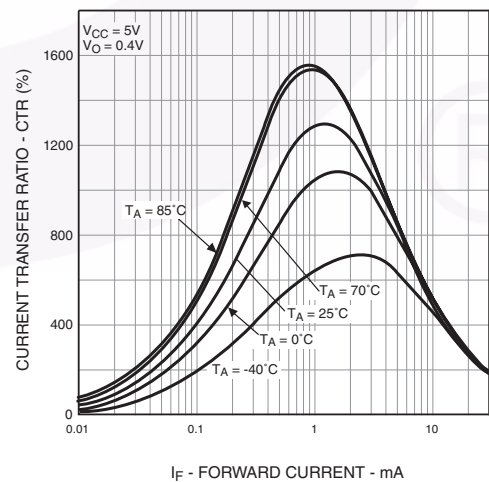


Fig. 9 Current Transfer Ratio vs. Forward Current (6N138 / 6N139 Only)



Typical Performance Curves (Continued)

Fig. 10 Current Transfer Ratio vs. Base-Emitter Resistance (6N138 / 6N139 Only)

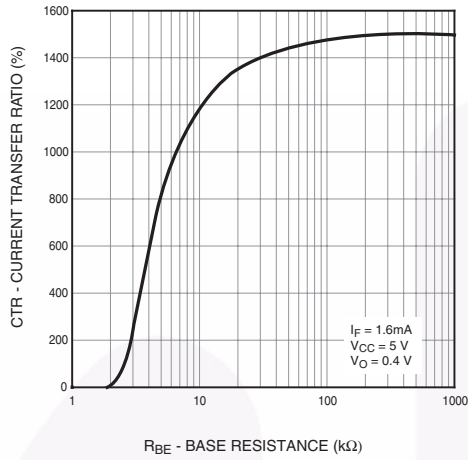


Fig. 11 Current Transfer Ratio vs. Forward Current (HCPL2730 / HCPL2731 Only)

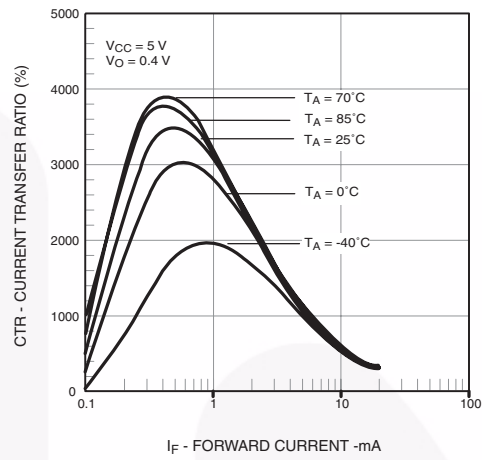


Fig. 12 Output Current vs. Output Voltage (6N138 / 6N139 Only)

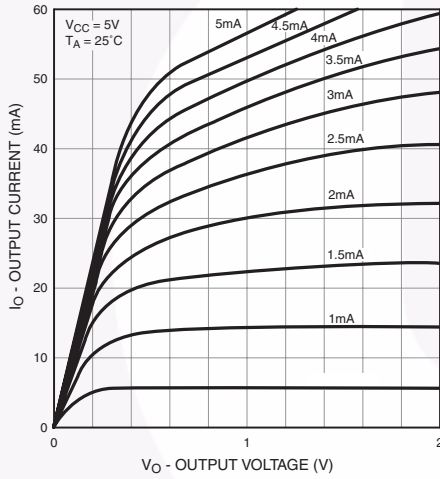


Fig. 13 Output Current vs. Output Voltage (HCPL2730 / HCPL2731 Only)

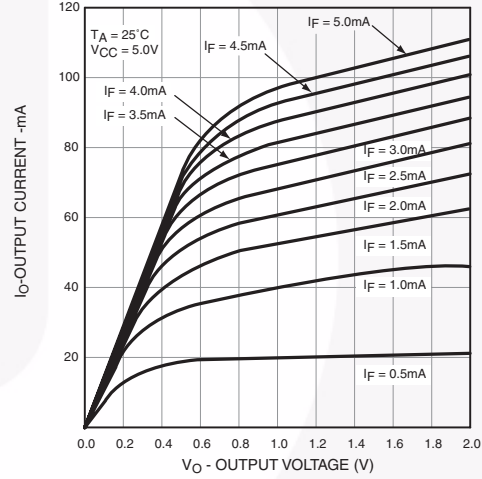


Fig. 14 Output Current vs. Input Diode Forward Current (6N138 / 6N139 Only)

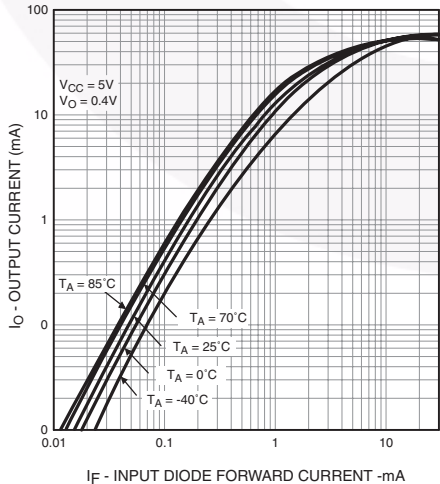
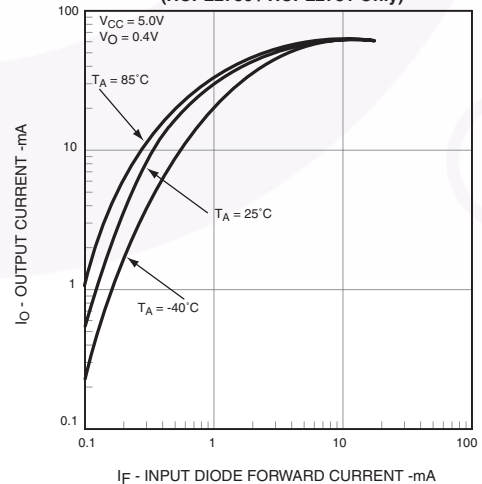


Fig. 15 Output Current vs. Input Diode Forward Current (HCPL2730 / HCPL2731 Only)



Typical Performance Curves (Continued)

Fig. 16 Logic Low Supply Current vs. Input Diode Forward Current (6N138 / 6N139 Only)

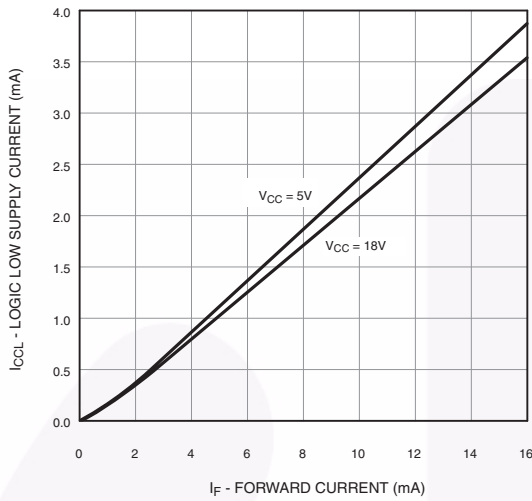


Fig. 17 Logic Low Supply Current vs. Input Diode Forward Current (HCPL2730 / HCPL2731 Only)

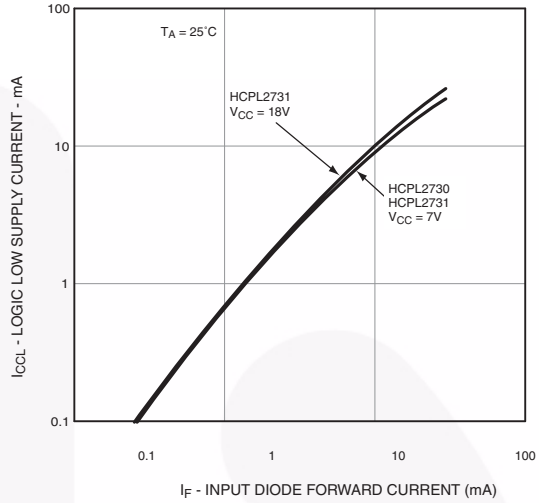


Fig. 18 Propagation Delay vs. Input Diode Forward Current (6N138 / 6N139 Only)

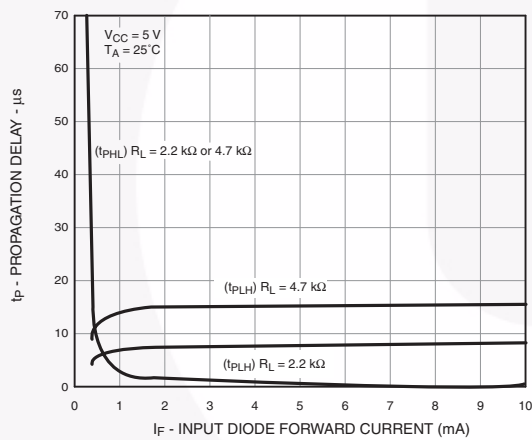


Fig. 19 Propagation Delay vs. Input Diode Forward Current (HCPL2730 / HCPL2731 Only)

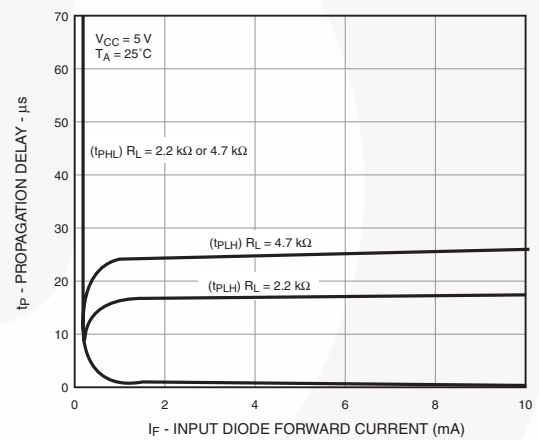


Fig. 20 Propagation Delay to Logic Low vs. Pulse Period (6N138 / 6N139 Only)

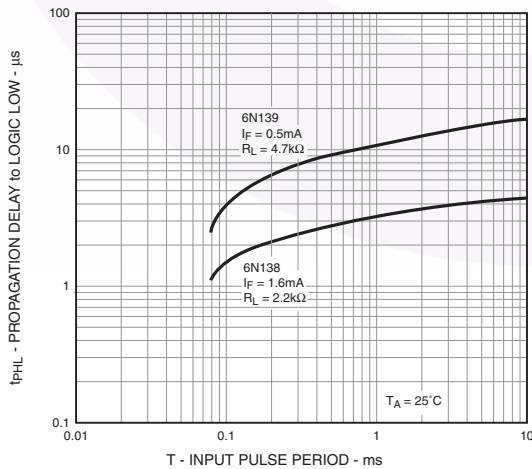
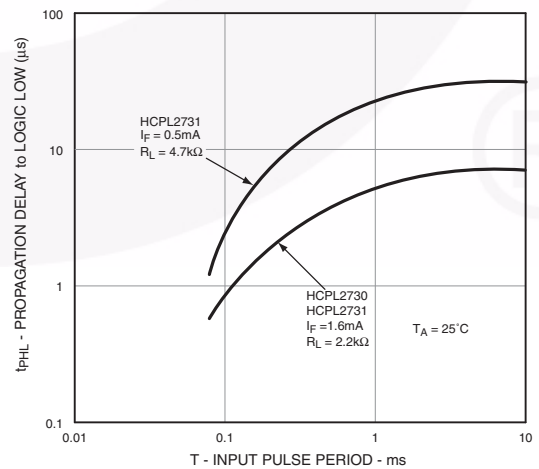


Fig. 21 Propagation Delay to Logic Low vs. Pulse Period (HCPL2730 / HCPL2731 Only)



Typical Performance Curves (Continued)

Fig. 22 Propagation Delay vs. Temperature (6N138 / 6N139 Only)

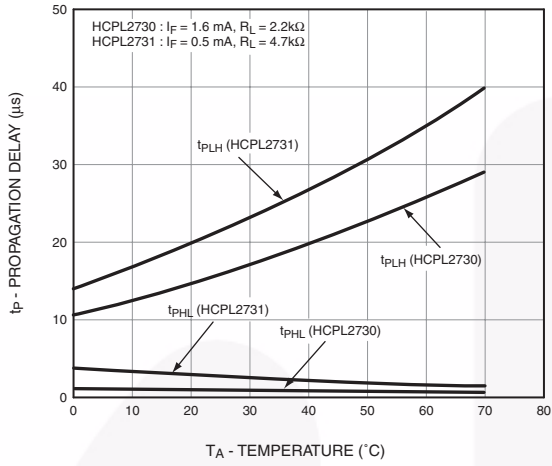
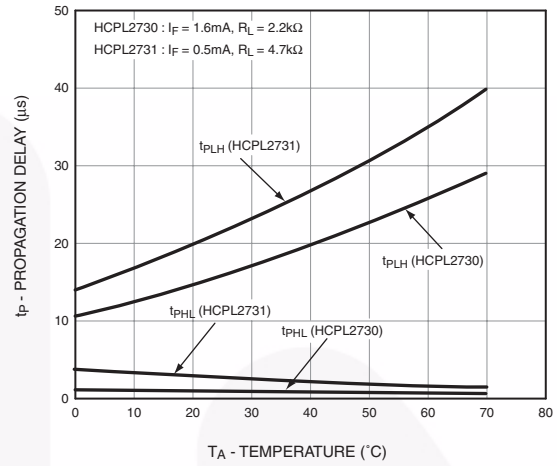


Fig. 23 Propagation Delay vs. Temperature (HCPL2730 / HCPL2731 Only)



Test Circuits

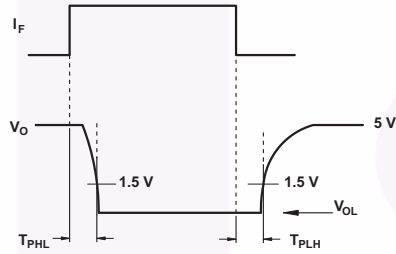
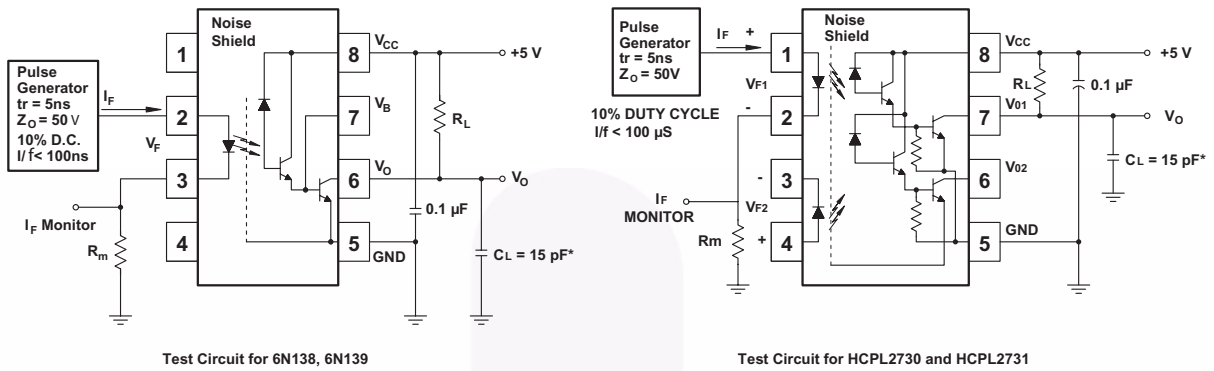


Fig. 24 Switching Time Test Circuit

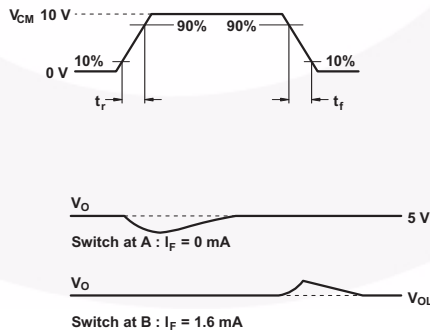
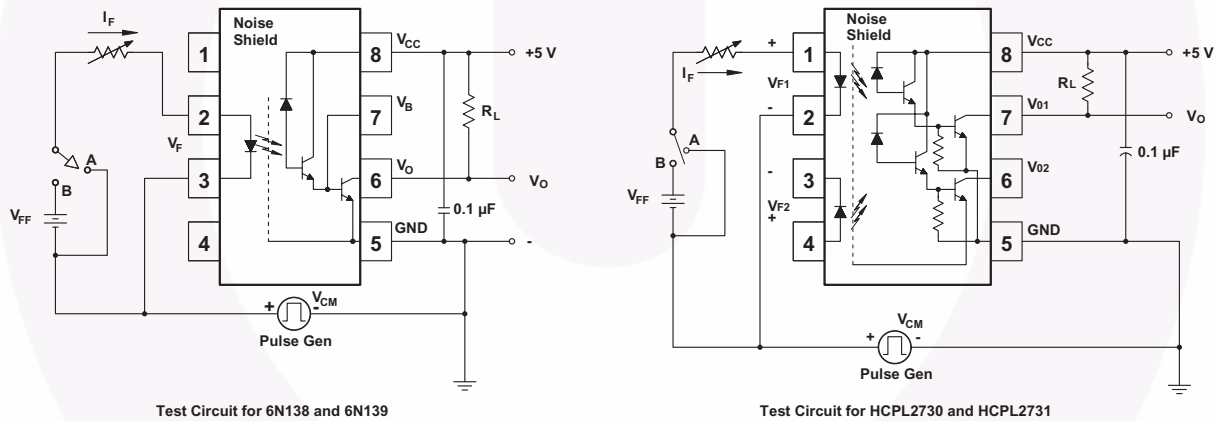
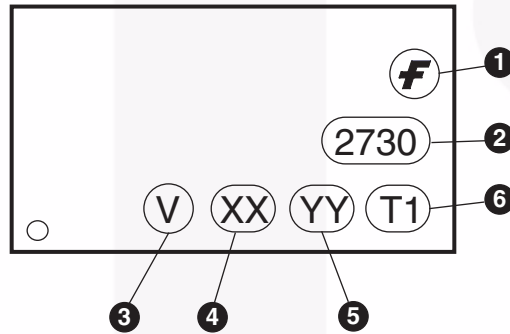


Fig. 25 Common Mode Immunity Test Circuit

Ordering Information

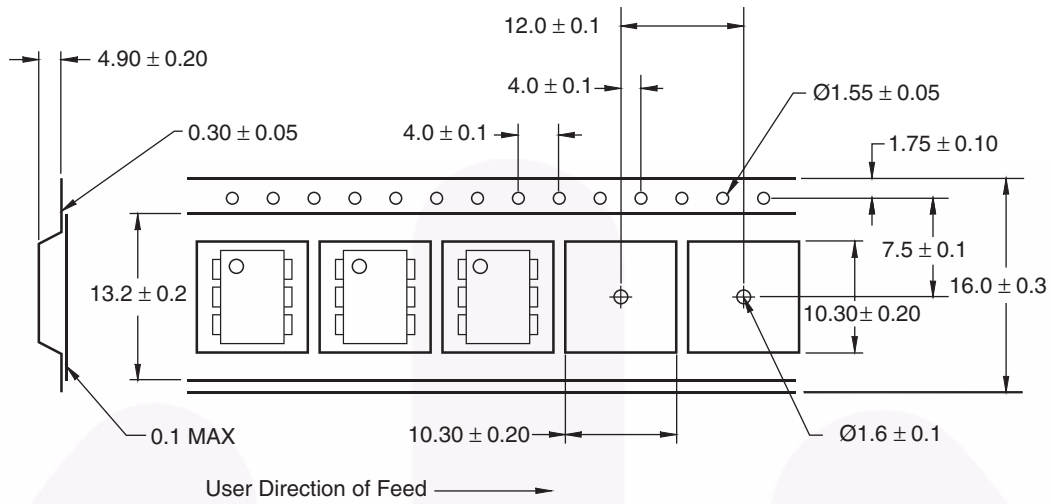
| Option | Example Part Number | Description |
|-----------|---------------------|---|
| No Suffix | 6N138 | Standard Through Hole Device, 50 pcs per tube |
| S | 6N138S | Surface Mount Lead Bend |
| SD | 6N138SD | Surface Mount; Tape and reel |
| W | 6N138W | 0.4" Lead Spacing |
| V | 6N138V | VDE0884 |
| WV | 6N138WV | VDE0884; 0.4" lead spacing |
| SV | 6N138SV | VDE0884; surface mount |
| SDV | 6N138SDV | VDE0884; surface mount; tape and reel |

Marking Information

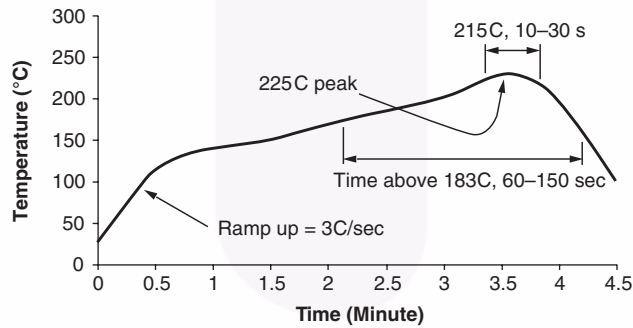


| Definitions | |
|-------------|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | Two digit year code, e.g., '07' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

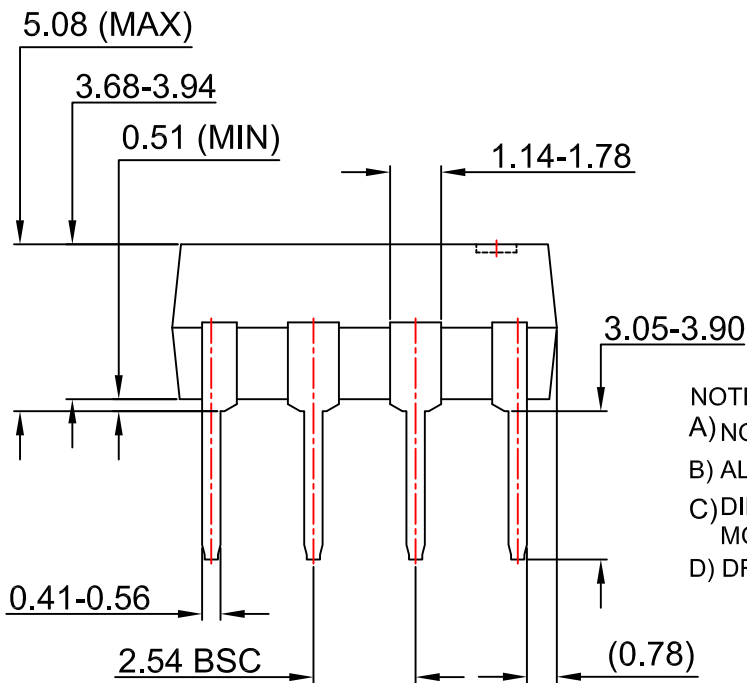
Tape Specifications



Reflow Profile



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended

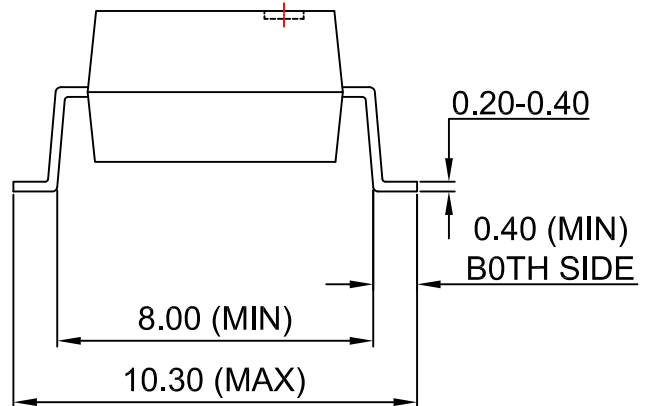


- NOTES:
 A) NO STANDARD APPLIES TO THIS PACKAGE
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
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LAND PATTERN RECOMMENDATION



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|--------------------------|-----------------------|---|
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