14-Bit, 170 MSPS/250 MSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9250**

FEATURES

- JESD204B Subclass 0 or Subclass 1 coded serial digital outputs
- Signal-to-noise ratio (SNR) = 70.6 dBFS at 185 MHz AIN and 250 MSPS
- Spurious-free dynamic range (SFDR) = 88 dBc at 185 MHz AIN and 250 MSPS
- Total power consumption: 711 mW at 250 MSPS
- 1.8 V supply voltages
- Integer 1-to-8 input clock divider
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer (DCS)
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes

FUNCTIONAL BLOCK DIAGRAM

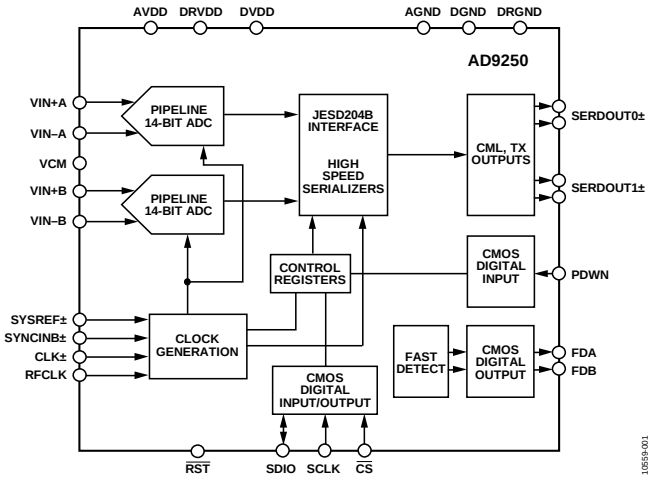

Figure 1.

APPLICATIONS

- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMAX, W-CDMA, CDMA2000, GSM, EDGE, LTE
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers
- I/Q demodulation systems
- Smart antenna systems
- Electronic test and measurement equipment
- Radar receivers
- COMSEC radio architectures
- IED detection/jamming systems
- General-purpose software radios
- Broadband data applications

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 170 MSPS/250 MSPS ADC.
2. The configurable JESD204B output block supports up to 5 Gbps per lane.
3. An on-chip, phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.
4. Support for an optional RF clock input to ease system board design.
5. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
6. Operation from a single 1.8 V power supply.
7. Standard serial port interface (SPI) that supports various product features and functions such as controlling the clock DCS, power-down, test modes, voltage reference mode, over range fast detection, and serial output configuration.

Rev. C Document Feedback

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GENERAL DESCRIPTION

The AD9250 is a dual, 14-bit ADC with sampling speeds of up to 250 MSPS. The AD9250 is designed to support communications applications where low cost, small size, wide bandwidth, and versatility are desired.

The ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. The ADC cores feature wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance. The JESD204B high speed serial interface reduces board routing requirements and lowers pin count requirements for the receiving device.

By default, the ADC output data is routed directly to the two JESD204B serial output lanes. These outputs are at CML voltage levels. Four modes support any combination of M = 1 or 2 (single or dual converters) and L = 1 or 2 (one or two lanes). For dual ADC mode, data can be sent through two lanes at the maximum sampling rate of 250 MSPS. However, if data is sent through one lane, a sampling rate of up to 125 MSPS is supported. Synchronization inputs (SYNCINB± and SYSREF±) are provided.

Flexible power-down options allow significant power savings, when desired. Programmable overrange level detection is supported for each channel via the dedicated fast detect pins.

Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface.

The AD9250 is available in a 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 1.

		AD9250-170			AD9250-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−16		+16	−16		+16	mV
Gain Error	Full	−6		+2	−6		+2.5	%FSR
Differential Nonlinearity (DNL)	Full			±0.75			±0.75	LSB
	25°C		±0.25			±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±2.1			±3.5	LSB
	25°C		±1.5			±1.5		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full	−15		+15	−15		+15	mV
Gain Error	Full	−2		+3.5	−2		+3	%FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±16			±44		ppm/°C
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		1.49			1.49		LSB rms
ANALOG INPUT								
Input Span	Full		1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5		pF
Input Resistance[3]	Full		20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9		V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}	Full		233	260		255	280	mA
$I_{DRVDD} + I_{DVDD}$	Full		104	113		140	160	mA
POWER CONSUMPTION								
Sine Wave Input	Full		607			711		mW
Standby Power[4]	Full		280			339		mW
Power-Down Power	Full		9			9		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured with a dc input and the CLK± pin active.

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 2.

		AD9250-170			AD9250-250			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 30 MHz	25°C		72.5			72.1		dBFS
f_{IN} = 90 MHz	25°C		72.0			71.7		dBFS
	Full	70.7						dBFS
f_{IN} = 140 MHz	25°C		71.4			71.2		dBFS
f_{IN} = 185 MHz	25°C		70.7			70.6		dBFS
	Full				69.3			dBFS
f_{IN} = 220 MHz	25°C		70.1			70.0		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 30 MHz	25°C		71.3			70.7		dBFS
f_{IN} = 90 MHz	25°C		70.9			70.5		dBFS
	Full	69.6						dBFS
f_{IN} = 140 MHz	25°C		70.3			70.0		dBFS
f_{IN} = 185 MHz	25°C		69.6			69.5		dBFS
	Full				68.0			dBFS
f_{IN} = 220 MHz	25°C		68.9			68.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 30 MHz	25°C		11.5			11.5		Bits
f_{IN} = 90 MHz	25°C		11.4			11.4		Bits
f_{IN} = 140 MHz	25°C		11.3			11.3		Bits
f_{IN} = 185 MHz	25°C		11.1			11.2		Bits
f_{IN} = 220 MHz	25°C		10.9			11.0		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 30 MHz	25°C		92			89		dBc
f_{IN} = 90 MHz	25°C		95			86		dBc
	Full	78						dBc
f_{IN} = 140 MHz	25°C		91			86		dBc
f_{IN} = 185 MHz	25°C		86			88		dBc
	Full				80			dBc
f_{IN} = 220 MHz	25°C		85			88		dBc
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 30 MHz	25°C		−92			−89		dBc
f_{IN} = 90 MHz	25°C		−95			−87		dBc
	Full			−78				dBc
f_{IN} = 140 MHz	25°C		−91			−86		dBc
f_{IN} = 185 MHz	25°C		−86			−88		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−85			−88		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 30 MHz	25°C		−95			−94		dBc
f_{IN} = 90 MHz	25°C		−94			−96		dBc
	Full			−78				dBc
f_{IN} = 140 MHz	25°C		−97			−96		dBc
f_{IN} = 185 MHz	25°C		−96			−88		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−93			−91		dBc

Parameter[1]	Temperature	AD9250-170 Min	AD9250-170 Typ	AD9250-170 Max	AD9250-250 Min	AD9250-250 Typ	AD9250-250 Max	Unit
TWO-TONE SFDR								
f_{IN} = 184.12 MHz (−7 dBFS), 187.12 MHz (−7 dBFS)	25°C		87			84		dBc
CROSSTALK[2]	Full		95			95		dB
FULL POWER BANDWIDTH[3]	25°C		1000			1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation* for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Full power bandwidth is the bandwidth of operation determined by where the spectral power of the fundamental frequency is reduced by 3 dB.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Input CLK± Clock Rate	Full	40		625	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	0		+60	µA
Low Level Input Current	Full	−60		0	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
RF CLOCK INPUT (RFCLK)					
Input CLK± Clock Rate	Full	650		1500	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
Input Voltage Level					
High	Full	1.2		AVDD	V
Low	Full	AGND		0.6	V
High Level Input Current	Full	0		+150	µA
Low Level Input Current	Full	−150		0	µA
Input Capacitance	Full		1		pF
Input Resistance (AC-Coupled)	Full	8	10	12	kΩ
SYNCIN INPUT (SYNCINB+/SYNCINB−)					
Logic Compliance			CMOS/LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	DGND		DVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
SYSREF INPUT (SYSREF±)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT ($\overline{RST}$, $\overline{CS}$)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−100		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (SERDOUT0±/SERDOUT1±)					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	400	600	750	mV
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V
DIGITAL OUTPUTS (SDIO/FDA/FDB)					
High Level Output Voltage (V_{OH})	Full				
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage (V_{OL})	Full				
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Symbol	Temperature	AD9250-170 Min	AD9250-170 Typ	AD9250-170 Max	AD9250-250 Min	AD9250-250 Typ	AD9250-250 Max	Unit
CLOCK INPUT PARAMETERS									
Conversion Rate[1]	f_S	Full	40		170	40		250	MSPS
SYSREF± Setup Time to Rising Edge CLK±[2]	t_{REFS}	Full		0.31			0.31		ns
SYSREF± Hold Time from Rising Edge CLK±[2]	t_{REFH}	Full		0			0		ns
SYSREF± Setup Time to Rising Edge RFCLK[2]	t_{REFSRF}	Full		0.50			0.50		ns
SYSREF± Hold Time from Rising Edge RFCLK[2]	t_{REFHRF}	Full		0			0		ns
CLK± Pulse Width High	t_{CH}								
Divide-by-1 Mode, DCS Enabled		Full	2.61	2.9	3.19	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled		Full	2.76	2.9	3.05	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode		Full	0.8			0.8			ns
Aperture Delay	t_A	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter)	t_J	Full		0.16			0.16		ps rms
DATA OUTPUT PARAMETERS									
Data Output Period or Unit Interval (UI)		Full	$L/(20 \times M \times f_S)$			$L/(20 \times M \times f_S)$			Seconds
Data Output Duty Cycle		25°C		50			50		%
Data Valid Time		25°C		0.84			0.78		UI
PLL Lock Time (t_{LOCK})		25°C		25			25		µs
Wake-Up Time									
Standby		25°C		10			10		µs
ADC (Power-Down)[3]		25°C		250			250		µs
Output (Power-Down)[4]		25°C		50			50		µs
Subclass 0: SYNCINB± Falling Edge to First Valid K.28 Characters (Delay Required for Rx CGS Start)		Full	5			5			Multiframes
Subclass 1: SYSREF± Rising Edge to First Valid K.28 Characters (Delay Required for SYNCB± Rising Edge/Rx CGS Start)		Full	6			6			Multiframes
CGS Phase K.28 Characters Duration		Full	1			1			Multiframes
Pipeline Delay									
JESD204B M1, L1 Mode (Latency)		Full		36			36		Cycles[5]
JESD204B M1, L2 Mode (Latency)		Full		59			59		Cycles
JESD204B M2, L1 Mode (Latency)		Full		25			25		Cycles
JESD204B M2, L2 Mode (Latency)		Full		36			36		Cycles
Fast Detect (Latency)		Full		7			7		Cycles
Data Rate per Lane		Full		3.4	5.0			5.0	Gbps
Uncorrelated Bounded High Probability (UBHP) Jitter		25°C		6			8		ps
Random Jitter									
At 3.4 Gbps		Full		2.3					ps rms
At 5.0 Gbps		Full					1.7		ps rms
Output Rise/Fall Time		Full		60			60		ps
Differential Termination Resistance		25°C		100			100		Ω
Out-of-Range Recovery Time		Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Refer to Figure 3 for timing diagram.
[3] Wake-up time ADC is defined as the time required for the ADC to return to normal operation from power-down mode.
[4] Wake-up time output is defined as the time required for JESD204B output to return to normal operation from power-down mode.
[5] Cycles refers to ADC conversion rate cycles.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS (See Figure 62)					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between $\overline{CS}$ and SCLK	2			ns
t_H	Hold time between $\overline{CS}$ and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in figures)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in figures)	10			ns
t_{SPI_RST}	Time required after hard or soft reset until SPI access is available (not shown in figures)	500			µs

Timing Diagrams

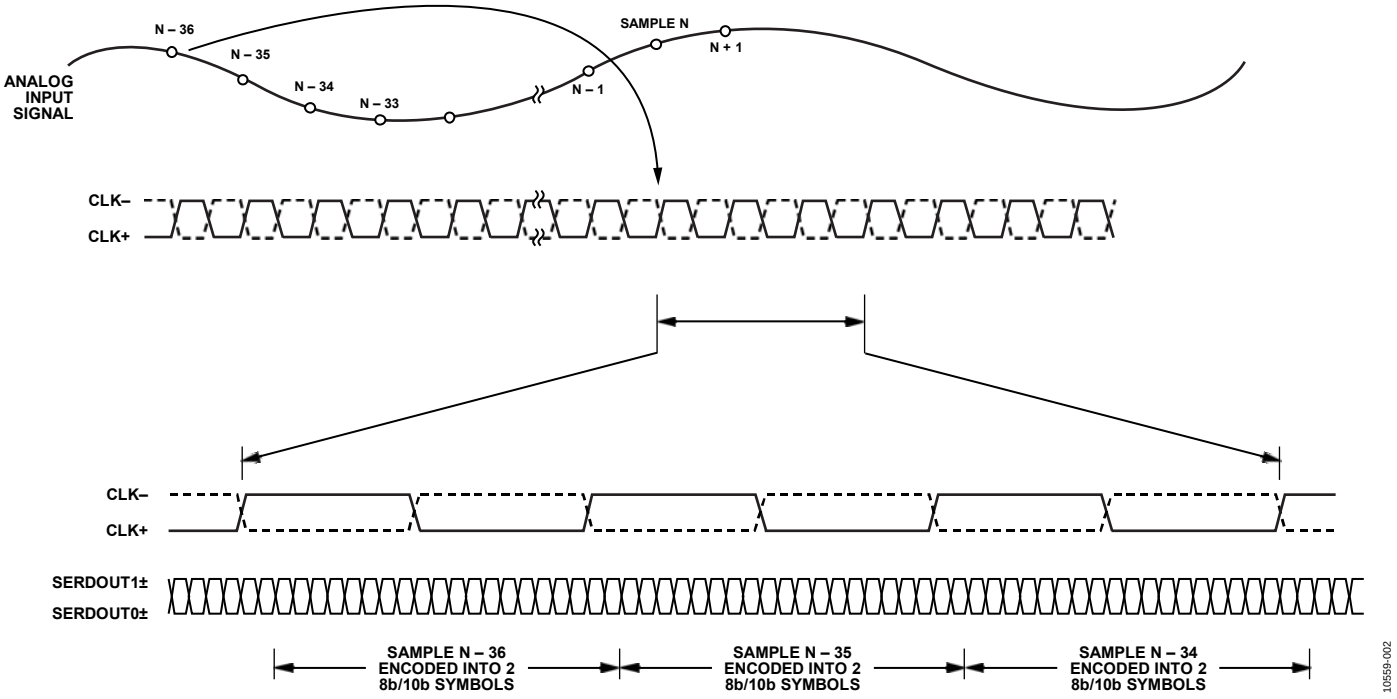


Figure 2. Data Output Timing

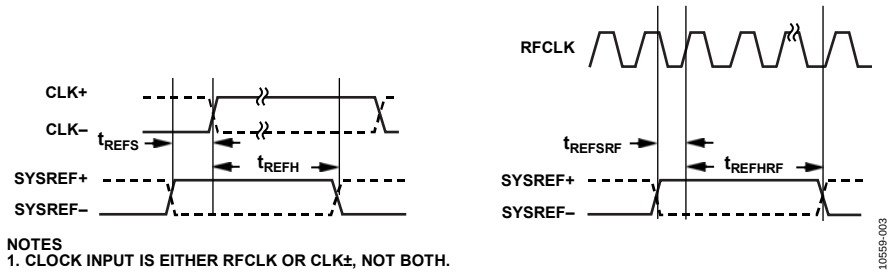


Figure 3. SYSREF± Setup and Hold Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
RFCLK to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
$\overline{CS}$, PDWN to AGND	−0.3 V to AVDD + 0.3 V
SCLK to AGND	−0.3 V to AVDD + 0.3 V
SDIO to AGND	−0.3 V to AVDD + 0.3 V
$\overline{RST}$ to DGND	−0.3 V to DVDD + 0.3 V
FDA, FDB to DGND	−0.3 V to DVDD + 0.3 V
SERDOUT0+, SERDOUT0−, SERDOUT1+, SERDOUT1− to AGND	−0.3 V to DRVDD + 0.3 V
SYNCINB+, SYNCINB− to DGND	−0.3 V to DVDD + 0.3 V
SYSREF+, SYSREF− to AGND	−0.3 V to AVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. This increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
48-Lead LFCSP 7 mm × 7 mm (CP-48-13)	0	25	2	14	°C/W
	1.0	22			°C/W
	2.5	20			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

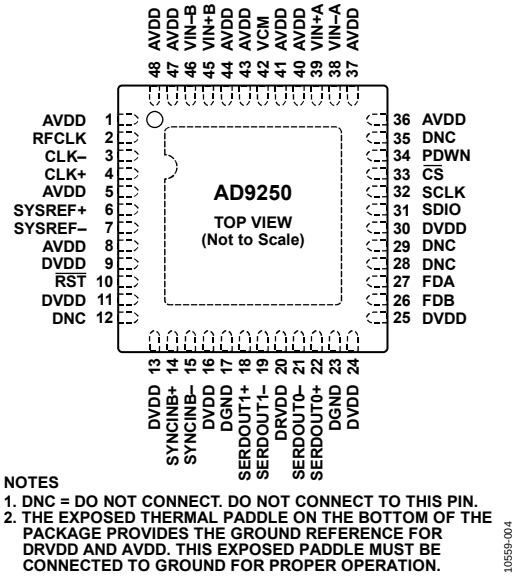


Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
1, 5, 8, 36, 37, 40, 41, 43, 44, 47, 48	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
9, 11, 13, 16, 24, 25, 30	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
12, 28, 29, 35	DNC		Do Not Connect.
17, 23	DGND		Ground Reference for DVDD.
20	DRVDD	Supply	JESD204B PHY Serial Output Driver Supply (1.8 V Nominal). Note that the DRVDD power is referenced to the AGND Plane.
Exposed Paddle	AGND/DRGND	Ground	The exposed thermal paddle on the bottom of the package provides the ground reference for DRVDD and AVDD. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
2	RFCLK	Input	ADC RF Clock Input.
3	CLK–	Input	ADC Nyquist Clock Input—Complement.
4	CLK+	Input	ADC Nyquist Clock Input—True.
38	VIN–A	Input	Differential Analog Input Pin (–) for Channel A.
39	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
42	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. Decouple this pin to ground using a 0.1 µF capacitor.
45	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
46	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
ADC Fast Detect Outputs			
26	FDB	Output	Channel B Fast Detect Indicator (CMOS Levels).
27	FDA	Output	Channel A Fast Detect Indicator (CMOS Levels).
Digital Inputs			
6	SYSREF+	Input	JESD204B LVDS SYSREF Input—True.
7	SYSREF–	Input	JESD204B LVDS SYSREF Input—Complement.
14	SYNCINB+	Input	JESD204B LVDS SYNC Input—True.
15	SYNCINB–	Input	JESD204B LVDS SYNC Input—Complement.

Pin No.	Mnemonic	Type	Description
Data Outputs			
18	SERDOUT1+	Output	Lane B CML Output Data—True.
19	SERDOUT1−	Output	Lane B CML Output Data—Complement.
21	SERDOUT0−	Output	Lane A CML Output Data—Complement.
22	SERDOUT0+	Output	Lane A CML Output Data—True.
DUT Controls			
10	$\overline{\text{RST}}$	Input	Digital Reset (Active Low).
31	SDIO	Input/Output	SPI Serial Data I/O.
32	SCLK	Input	SPI Serial Clock.
33	$\overline{\text{CS}}$	Input	SPI Chip Select (Active Low).
34	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 18).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, sample rate is maximum for speed grade, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, link parameters used were M = 2 and L = 2, unless otherwise noted.

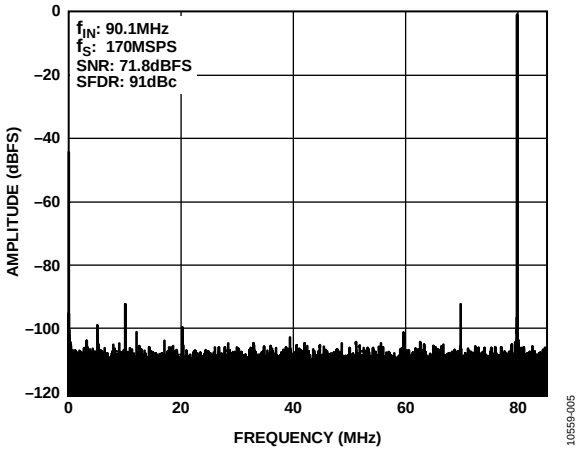


Figure 5. AD9250-170 Single-Tone FFT with f_{IN} = 90.1 MHz

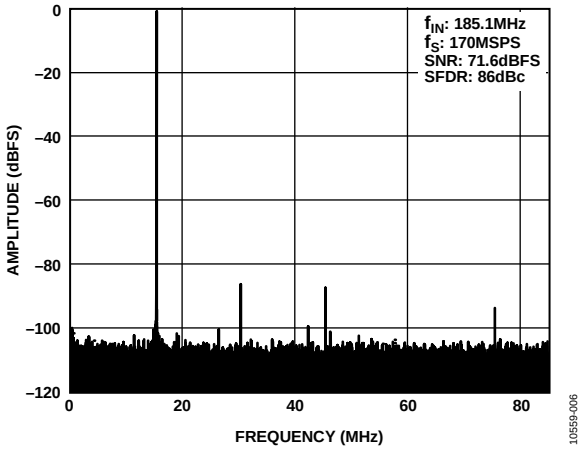


Figure 6. AD9250-170 Single-Tone FFT with f_{IN} = 185.1 MHz

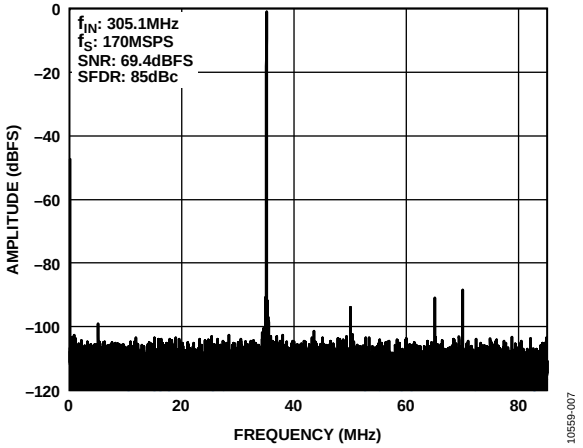


Figure 7. AD9250-170 Single-Tone FFT with f_{IN} = 305.1 MHz

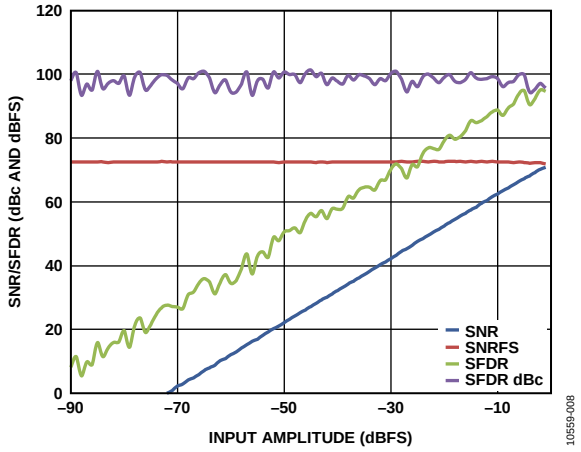


Figure 8. AD9250-170 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

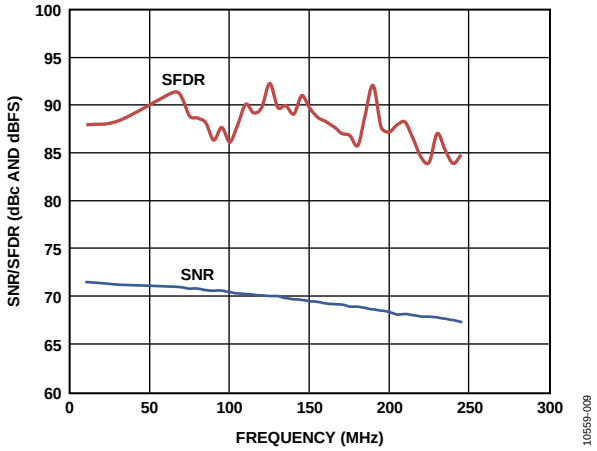


Figure 9. AD9250-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

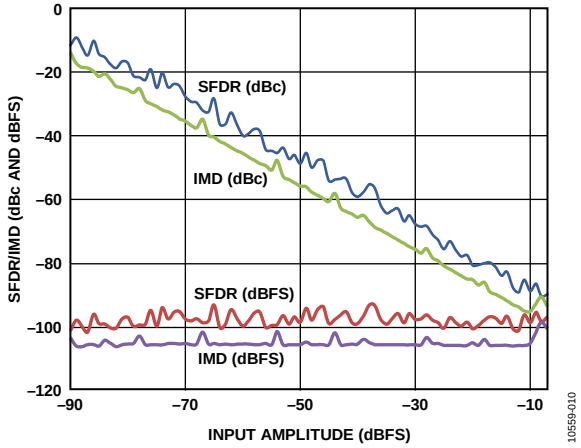


Figure 10. AD9250-170 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

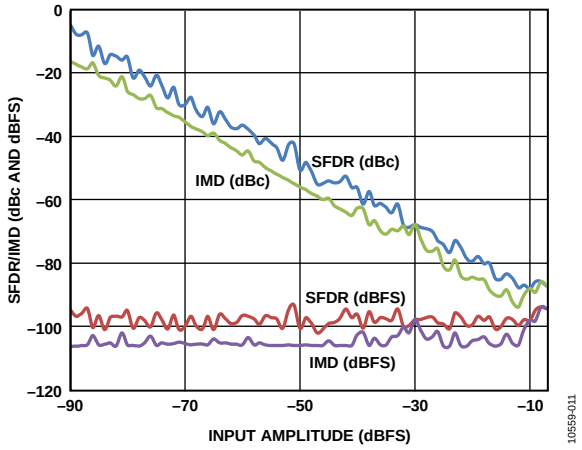


Figure 11. AD9250-170 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

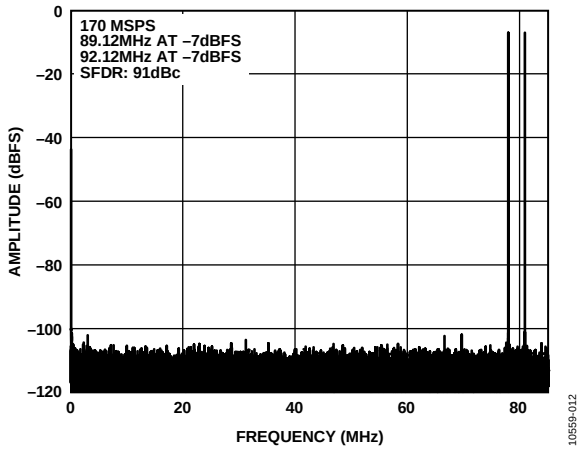


Figure 12. AD9250-170 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

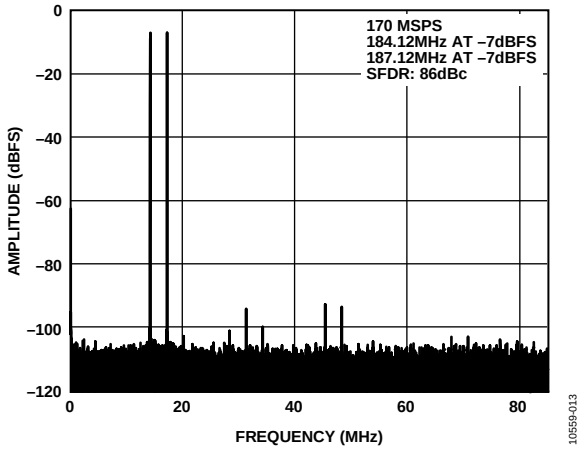


Figure 13. AD9250-170 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

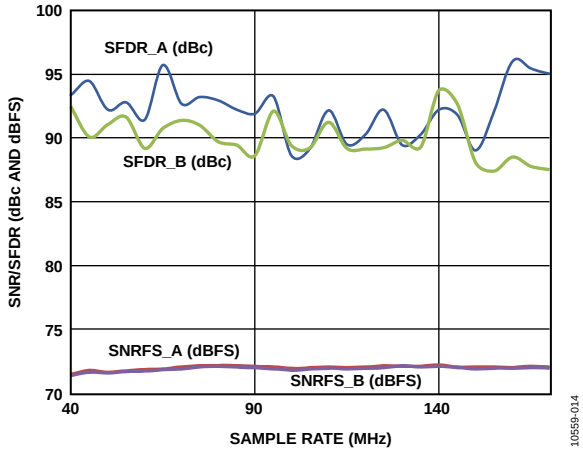


Figure 14. AD9250-170 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

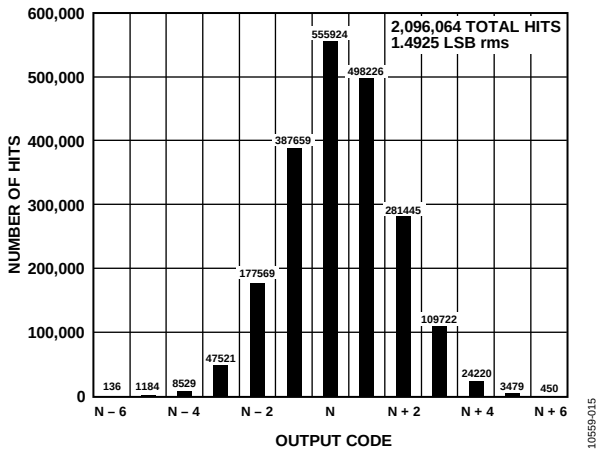


Figure 15. AD9250-170 Grounded Input Histogram

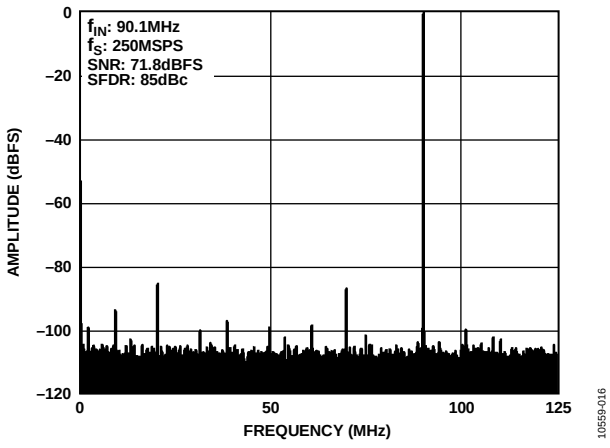


Figure 16. AD9250-250 Single-Tone FFT with f_{IN} = 90.1 MHz

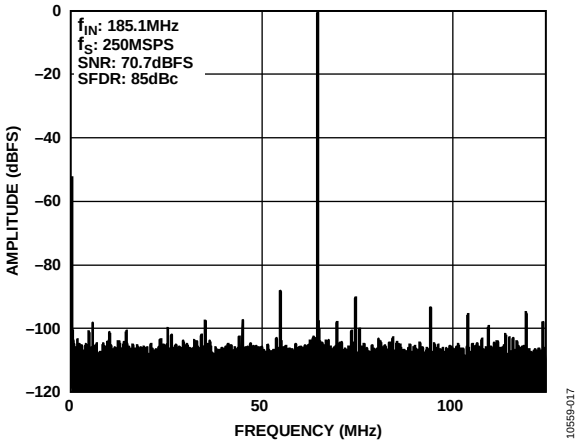


Figure 17. AD9250-250 Single-Tone FFT with f_{IN} = 185.1 MHz

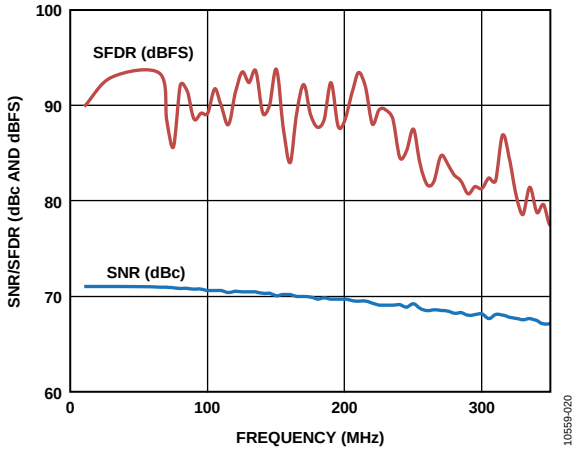


Figure 20. AD9250-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

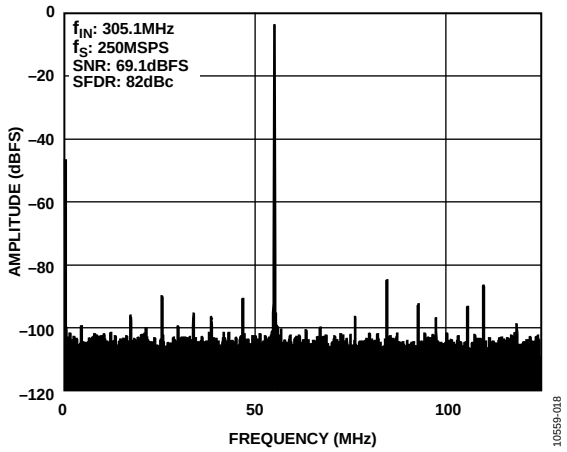


Figure 18. AD9250-250 Single-Tone FFT with f_{IN} = 305.1 MHz

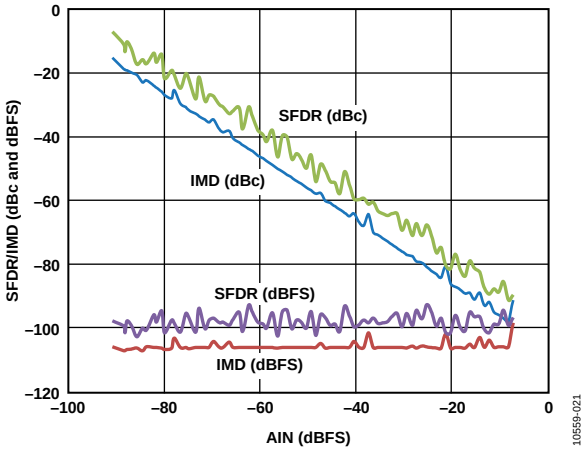


Figure 21. AD9250-250 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

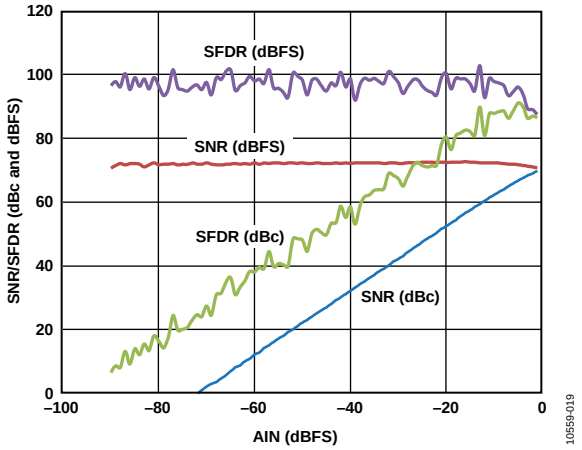


Figure 19. AD9250-250 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

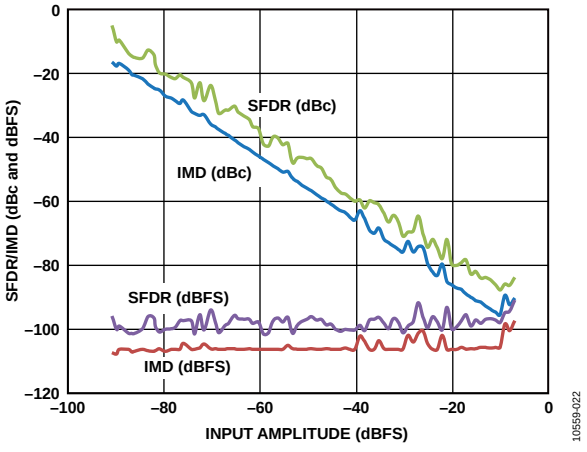


Figure 22. AD9250-250 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

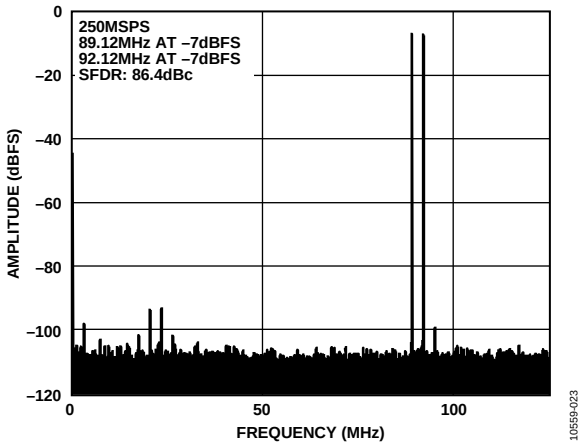


Figure 23. AD9250-250 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

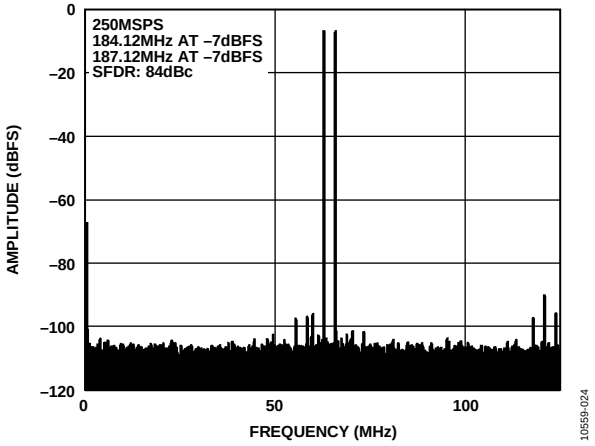


Figure 24. AD9250-250 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

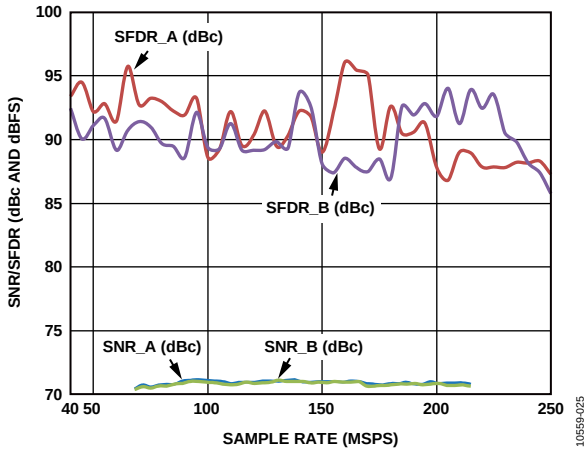


Figure 25. AD9250-250 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

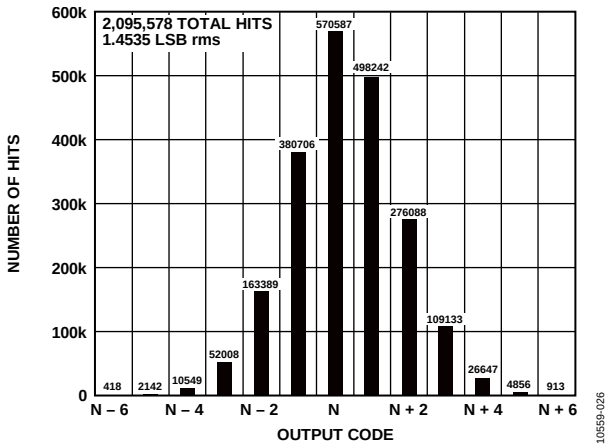


Figure 26. AD9250-250 Grounded Input Histogram

EQUIVALENT CIRCUITS

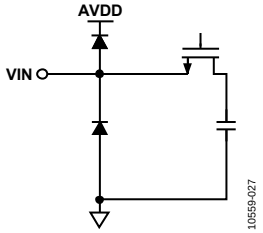


Figure 27. Equivalent Analog Input Circuit

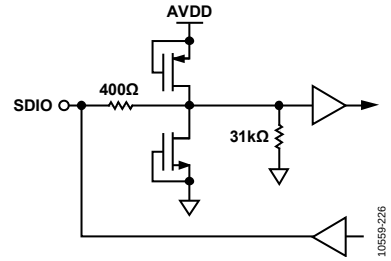


Figure 31. Equivalent SDIO Circuit

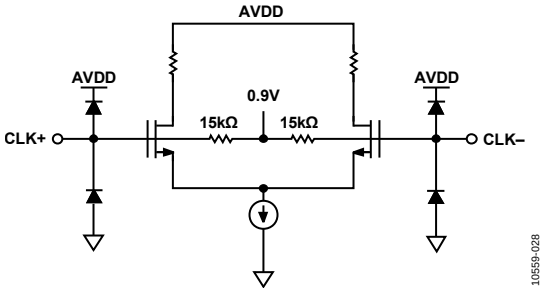


Figure 28. Equivalent Clock Input Circuit

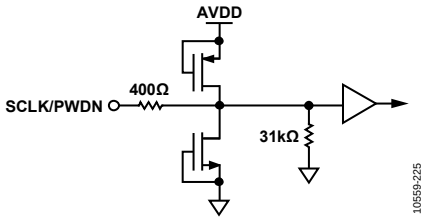


Figure 32. Equivalent SCLK or PDWN Input Circuit

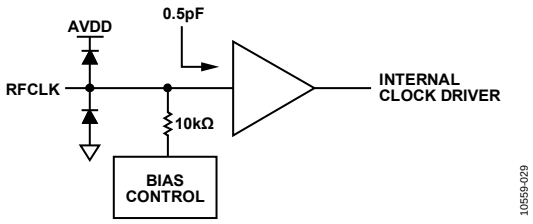


Figure 29. Equivalent RF Clock Input Circuit

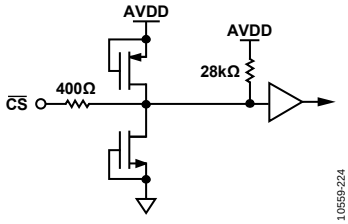


Figure 33. Equivalent $\overline{CS}$ Input Circuit

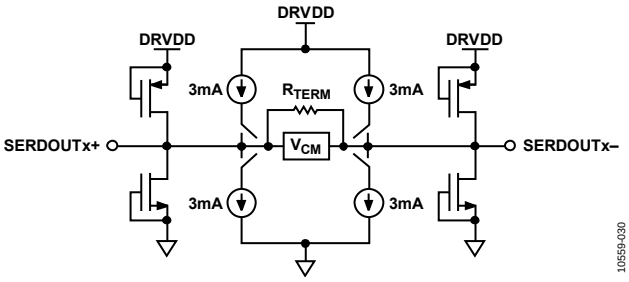


Figure 30. Digital CML Output Circuit

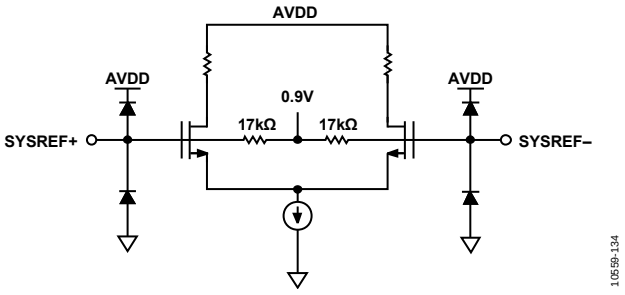


Figure 34. Equivalent SYSREF± Input Circuit

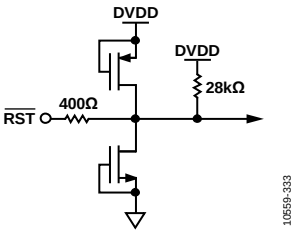


Figure 35. Equivalent $\overline{RST}$ Input Circuit

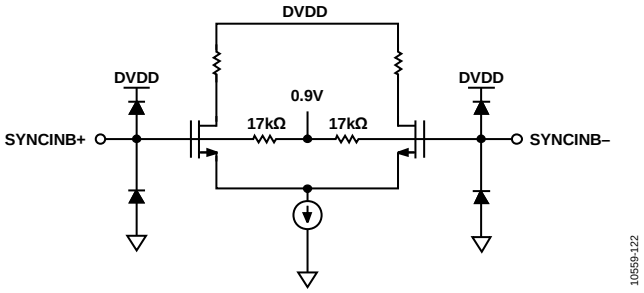


Figure 37. SYNCINB± Circuit

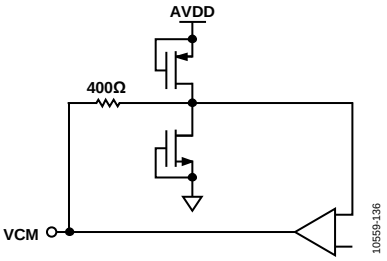


Figure 36. Equivalent VCM Circuit

THEORY OF OPERATION

The AD9250 has two analog input channels and two JESD204B output lanes. The signal passes through several stages before appearing at the output port(s).

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

A synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9250 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9250 architecture consists of a dual, front-end, sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9250 is a differential, switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 38). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, reduce the shunt capacitors. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

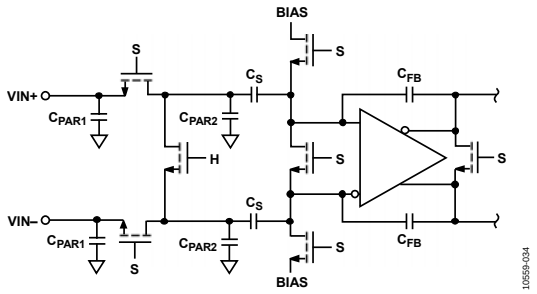


Figure 38. Switched-Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN– and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD9250 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). Decouple the VCM pin to ground by using a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD9250 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD9250 (see Figure 39), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

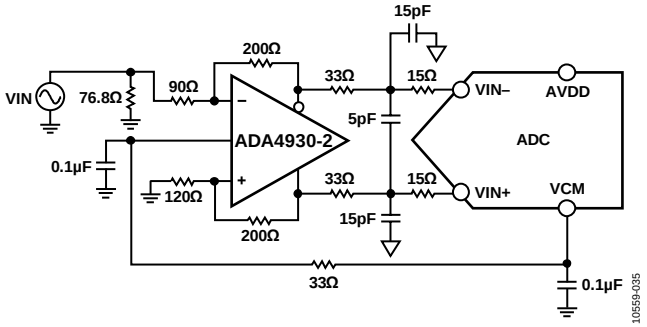


Figure 39. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 40. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

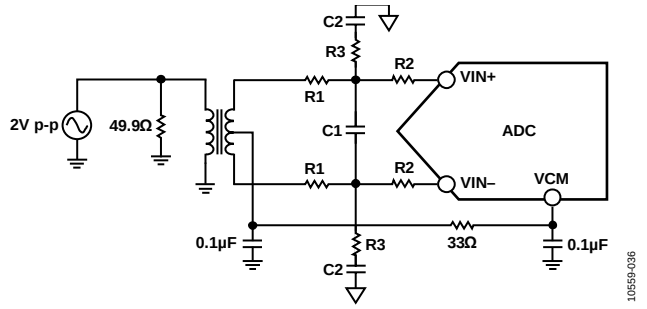


Figure 40. Differential Transformer-Coupled Configuration

Consider the signal characteristics when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9250. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 41). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

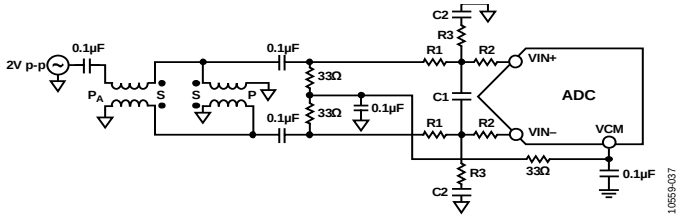


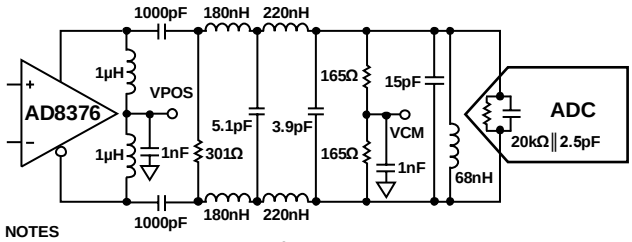
Figure 41. Differential Double Balun Input Configuration

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C1, C2, and R3 components shown in Figure 40 and Figure 41.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	24.9
100 to 400	15	8.2	0	8.2	24.9
>400	15	≤3.9	0	≤3.9	24.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGAs) provides good performance for driving the AD9250. Figure 42 shows an example of the AD8376 driving the AD9250 through a band-pass antialiasing filter.



NOTES
1. ALL INDUCTORS ARE COILCRAFT® 0603CS COMPONENTS WITH THE EXCEPTION OF THE 1µH CHOKE INDUCTORS (COILCRAFT 0603LS).
2. FILTER VALUES SHOWN ARE FOR A 20MHz BANDWIDTH FILTER CENTERED AT 140MHz.

Figure 42. Differential Input Configuration Using the AD8376

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9250. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC tracks the reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

The AD9250 has two options for deriving the input sampling clock, a differential Nyquist sampling clock input or an RF clock input (which is internally divided by 4). The clock input is selected in Register 0x09 and by default is configured for the Nyquist clock input. For optimum performance, clock the AD9250 Nyquist sample clock input, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or via capacitors. These pins are biased internally (see Figure 43) and require no external bias. If the clock inputs are floated, CLK– is pulled slightly lower than CLK+ to prevent spurious clocking.

Nyquist Clock Input Options

The AD9250 Nyquist clock input supports a differential clock between 40 MHz to 625 MHz. The clock input structure supports differential input voltages from 0.3 V to 3.6 V and is therefore compatible with various logic family inputs, such as CMOS, LVDS, and LVPECL. A sine wave input is also accepted, but higher slew rates typically provide optimal performance. Clock source jitter is a critical parameter that can affect performance, as described in the Jitter Considerations section. If the inputs are floated, pull the CLK– pin low to prevent spurious clocking.

The Nyquist clock input pins, CLK+ and CLK–, are internally biased to 0.9 V and have a typical input impedance of 4 pF in parallel with 10 kΩ (see Figure 43). The input clock is typically ac-coupled to CLK+ and CLK–. Some typical clock drive circuits are presented in Figure 44 through Figure 47 for reference.

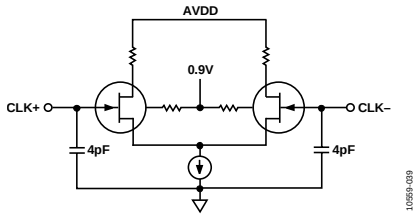


Figure 43. Equivalent Nyquist Clock Input Circuit

For applications where a single-ended low jitter clock between 40 MHz to 200 MHz is available, an RF transformer is recommended. An example using an RF transformer in the clock network is shown in Figure 44. At frequencies above 200 MHz, an RF balun is recommended, as seen in Figure 45. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9250 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9250, yet preserves the fast rise and fall times of the clock, which are critical to low jitter performance.

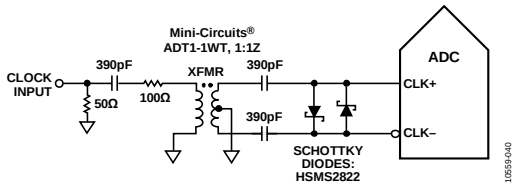


Figure 44. Transformer-Coupled Differential Clock (Up to 200 MHz)

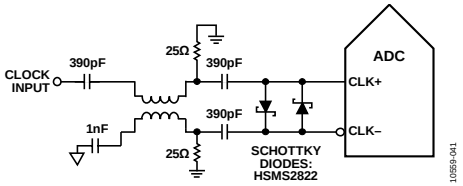


Figure 45. Balun-Coupled Differential Clock (Up to 625 MHz)

In some cases, it is desirable to buffer or generate multiple clocks from a single source. In those cases, Analog Devices, Inc., offers clock drivers with excellent jitter performance. Figure 46 shows a typical PECL driver circuit that uses PECL drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516-0 through AD9516-5 device family, AD9517-0 through AD9517-4 device family, AD9518-0 through AD9518-4 device family, AD9520-0 through AD9520-5 device family, AD9522-0 through AD9522-5 device family, AD9523, AD9524, and ADCLK905/ADCLK907/ADCLK925

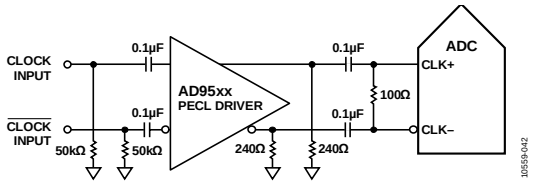


Figure 46. Differential PECL Sample Clock (Up to 625 MHz)

Analog Devices also offers LVDS clock drivers with excellent jitter performance. A typical circuit is shown in Figure 47 and uses LVDS drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516-0 through AD9516-5 device family, AD9517-0 through AD9517-4 device family, AD9518-0 through AD9518-4 device family, AD9520-0 through AD9520-5 device family, AD9522-0 through AD9522-5 device family, AD9523, and AD9524.

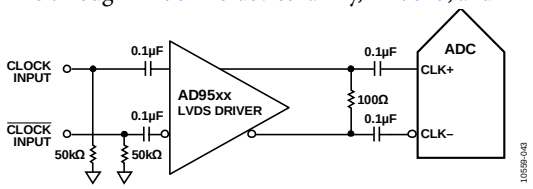


Figure 47. Differential LVDS Sample Clock (Up to 625 MHz)

RF Clock Input Options

The AD9250 RF clock input supports a single-ended clock between 625 GHz to 1.5 GHz. The equivalent RF clock input circuit is shown in Figure 48. The input is self biased to 0.9 V and is typically ac-coupled. The input has a typical input impedance of 10 kΩ in parallel with 1 pF at the RFCLK pin.

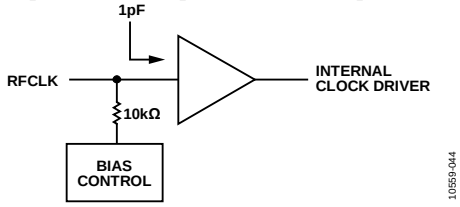


Figure 48. Equivalent RF Clock Input Circuit

It is recommended to drive the RF clock input of the AD9250 with a PECL or sine wave signal with a minimum signal amplitude of 600 mV peak to peak. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section. Figure 49 shows the preferred method of clocking when using the RF clock input on the AD9250. It is recommended to use a 50 Ω transmission line to route the clock signal to the RF clock input of the AD9250 due to the high frequency nature of the signal and terminate the transmission line close to the RF clock input.

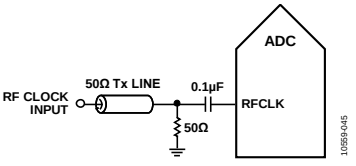


Figure 49. Typical RF Clock Input Circuit

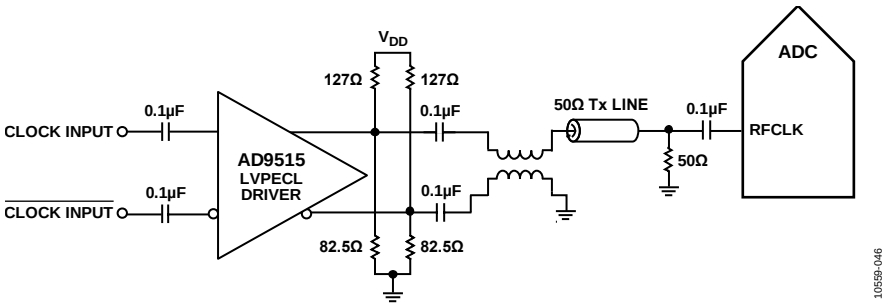


Figure 50. Differential PECL RF Clock Input Circuit

Figure 50 shows the RF clock input of the AD9250 being driven from the LVPECL outputs of the AD9515. The differential LVPECL output signal from the AD9515 is converted to a single-ended signal using an RF balun or RF transformer. The RF balun configuration is recommended for clock frequencies associated with the RF clock input.

Input Clock Divider

The AD9250 contains an input clock divider with the ability to divide the Nyquist input clock by integer values between 1 and 8. The RF clock input uses an on-chip predivider to divide the clock input by four before it reaches the 1 to 8 divider. This allows higher input frequencies to be achieved on the RF clock input. The divide ratios can be selected using Register 0x09 and Register 0x0B. Register 0x09 is used to set the RF clock input, and Register 0x0B can be used to set the divide ratio of the 1-to-8 divider for both the RF clock input and the Nyquist clock input. For divide ratios other than 1, the duty-cycle stabilizer is automatically enabled.

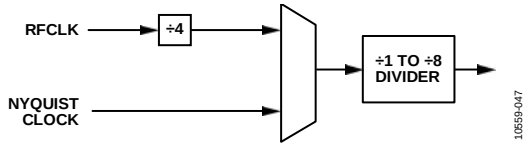


Figure 51. AD9250 Clock Divider Circuit

The AD9250 clock divider can be synchronized using the external SYSREF input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYSREF signal or only on the first signal after the register is written. A valid SYSREF causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9250 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9250.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 52.

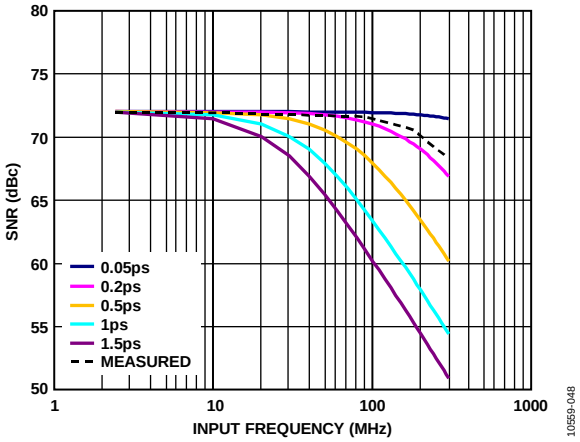


Figure 52. AD9250-250 SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9250. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), retime it by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance* and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter* for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 53, the power dissipated by the AD9250 is proportional to its sample rate. The data in Figure 53 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

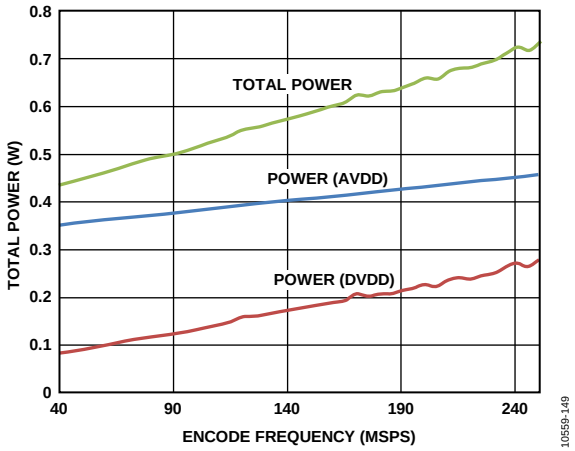


Figure 53. AD9250-250 Power vs. Encode Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9250 is placed in power-down mode. In this state, the ADC typically dissipates about 9 mW. Asserting the PDWN pin low returns the AD9250 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI,* for additional details.

DIGITAL OUTPUTS

JESD204B TRANSMIT TOP LEVEL DESCRIPTION

The AD9250 digital output uses the JEDEC Standard No. JESD204B, *Serial Interface for Data Converters*. JESD204B is a protocol to link the AD9250 to a digital processing device over a serial interface of up to 5 Gbps link speeds (3.5 Gbps, 14-bit ADC data rate). The benefits of the JESD204B interface include a reduction in required board area for data interface routing and the enabling of smaller packages for converter and logic devices. The AD9250 supports single or dual lane interfaces.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8b/10b encoding as well as optional scrambling to form serial output data. Lane synchronization is supported using special characters during the initial establishment of the link, and additional synchronization is embedded in the data stream thereafter. A matching external receiver is required to lock onto the serial data stream and recover the data and clock. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9250 JESD204B transmit block maps the output of the two ADCs over a link. A link can be configured to use either single or dual serial differential outputs that are called lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (AD9250 output) and receiver.

The JESD204B link is described according to the following parameters:

- S = samples transmitted/single converter/frame cycle (AD9250 value = 1)
- M = number of converters/converter device (AD9250 value = 2 by default, or can be set to 1)
- L = number of lanes/converter device (AD9250 value = 1 or 2)
- N = converter resolution (AD9250 value = 14)
- N' = total number of bits per sample (AD9250 value = 16)
- CF = number of control words/frame clock cycle/converter device (AD9250 value = 0)
- CS = number of control bits/conversion sample (configurable on the AD9250 up to 2 bits)
- K = number of frames per multiframe (configurable on the AD9250)
- HD = high density mode (AD9250 value = 0)
- F = octets/frame (AD9250 value = 2 or 4, dependent upon L = 2 or 1)
- C = control bit (overrange, overflow, underflow; available on the AD9250)
- T = tail bit (available on the AD9250)
- SCR = scrambler enable/disable (configurable on the AD9250)
- FCHK = checksum for the JESD204B parameters (automatically calculated and stored in register map)

Figure 54 shows a simplified block diagram of the AD9250 JESD204B link. By default, the AD9250 is configured to use two converters and two lanes. Converter A data is output to SERDOUT0+/SERDOUT0−, and Converter B is output to SERDOUT1+/SERDOUT1−. The AD9250 allows for other configurations such as combining the outputs of both converters onto a single lane or changing the mapping of the A and B digital output paths. These modes are setup through a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9250, the 14-bit converter word from each converter is broken into two octets (8 bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB), and two tail bits are added to fill the second octet. The tail bits can be configured as zeros, pseudo-random number sequence or control bits indicating overrange, underrange, or valid data conditions.

The two resulting octets can be scrambled. Scrambling is optional; however, it is available to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver should be a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8b/10b encoder. The 8b/10b encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 55 shows how the 14-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 55 illustrates the default data format.

At the data link layer, in addition to the 8b/10b encoding, the character replacement is used to allow the receiver to monitor frame alignment. The character replacement process occurs on the frame and multiframe boundaries, and implementation depends on which boundary is occurring, and if scrambling is enabled.

If scrambling is disabled, the following applies. If the last scrambled octet of the last frame of the multiframe equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet in the frame equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /F/= /K28.7/.

If scrambling is enabled, the following applies. If the last octet of the last frame of the multiframe equals 0x7C, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet equals 0xFC, the transmitter replaces the last octet with the control character /F/ = /K28.7/.

Refer to JEDEC Standard No. 204B-July 2011 for additional information about the JESD204B interface. Section 5.1 covers the transport layer and data format details and Section 5.2 covers scrambling and descrambling.

SYNCHRONIZATION

The AD9250 requires internal synchronization to process the ADC data and produce a JESD204B output. To accommodate extreme temperature changes and inconsistent power-up conditions that can occur, the timing of these circuits requires additional margin. To increase the timing margin, the procedures described in this section is required to maintain internal timing synchronization and maintain JESD204B link quality.

There are four specific cases to consider to accommodate, JESD204B Subclass 0 or 1 operation and if using Nyquist or harmonic clocking. Harmonic clocking uses an input clock at a multiple of between 2 through 8 of the ADC sample rate where the AD9250 internal clock divider is set (using Register 0x0B).

See Table 14 for a description of configuring JESD204B link modes of operation using Register 0x3A.

For Subclass 0 and a Nyquist input clock (when deterministic latency is not required and an external SYSREF is not used),

1. Apply power to the AD9250, and allow voltages and clocks to stabilize
2. Apply a soft reset by writing 0x3C to Register 0x00.
3. Wait at least 500 µs.
4. Set Register 0xEE and Register 0xEF to a value of 0x80.
5. Configure the AD9250 as desired, including the JESD204B parameters. Configure the link setup parameters (see the Link Setup Parameters section).
6. Establish an internal LMFC within the AD9250 by writing 0xFF to Register 0xF3.
7. Wait at least 6 LMFCs.
8. Perform the clock adjustment register writes as shown in the Clock Adjustment Register Writes section.
9. Wait at least 6 LMFCs.
10. Enable the JESD204B receiver and initiate a link.

For Subclass 1 and a Nyquist Input clock (when deterministic latency is required and an external SYSREF is used),

1. Apply power to the AD9250, and allow voltages and clocks to stabilize.
2. Apply a soft reset by writing 0x3C to Register 0x00.
3. Wait at least 500 µs.
4. Set Register 0xEE and Register 0xEF to a value of 0x80.
5. Configure the AD9250 as desired, including the JESD204B parameters. Configure the link setup parameters (see the Link Setup Parameters section).
6. Force an internal alignment within the AD9250 by writing 0xFF to Register 0xF3.
7. Wait at least 6 LMFCs.
8. Establish a LMFC within the AD9250 by providing a SYSREF signal.
9. Perform the clock adjustment register writes as shown in the Clock Adjustment Register Writes section.
10. Wait at least 6 LMFCs.
11. Enable the JESD204B receiver and initiate a link.

For Subclass 0 and harmonic input clock,

1. Apply power to the AD9250, and allow voltages and clocks to stabilize.
2. Assert a power-down either by using the PDWN input or by setting Register 0x08 with a value of 0x05.
3. Configure the proper clock divider setting in Register 0x0B. Commit the clock divider setting by writing 0x01 to Register 0xFF.
4. Set Register 0xEE and Register 0xEF to a value of 0x80.
5. Configure the AD9250 as desired, including the JESD204B parameters. Configure the link setup parameters (see the Link Setup Parameters section).
6. Deassert power down and wait at least 250 ms.
7. Force an internal alignment within the AD9250 by writing 0xFF to Register 0xF3.
8. Wait at least 6 LMFCs.
9. Perform the clock adjustment register writes as shown in the Clock Adjustment Register Writes section.
10. Wait at least 6 LMFCs.
11. Enable the JESD204B Receiver and initiate a link.

For Subclass 1 and harmonic input clock,

1. Apply power to the AD9250, and allow voltages and clocks to stabilize.
2. Assert a power-down either by using the PDWN input or by setting Register 0x08 a value of 0x05.
3. Configure the proper clock divider setting in Register 0x0B. Commit the clock dividet setting by writing 0x01 to Register 0xFF.
4. Set Register 0xEE and Register 0xEF to a value of 0x80.
5. Configure the AD9250 as desired, including the JESD204B parameters. Configure the link setup parameters (see the Link Setup Parameters section).
6. Deassert power down and wait at least 250 ms.
7. Force an internal alignment within the AD9250 by writing 0xFF to Register 0xF3.
8. Wait at least 6 LMFCs.
9. Set the LMFC using SYSREF for JESD204B Subclass 1 operation.
10. Perform the clock adjustment register writes as shown in the Clock Adjustment Register Writes section.
11. Enable the JESD204B receiver and initiate a link.
12. Wait at least 6 LMFCs.
13. Bring the JESD204B receiver out of reset.

If the AD9250 has been configured for the continuous SYSREF mode of operation using Register 0x3A, Bit 2 = 1, it is important to disable the internal SYSREF buffer by setting Register 0x3A, Bit 2 = 0, to remove the impact of external false triggers that affect the digital path.

Clock Adjustment Register Writes

Perform the clock adjustment writes in the following order:

1. Write 0x81 to Register 0xEE.
2. Write 0x81 to Register 0xEF.
3. Write 0x82 to Register 0xEE.
4. Write 0x82 to Register 0xEF.
5. Write 0x83 to Register 0xEE.
6. Write 0x83 to Register 0xEF.
7. Write 0x84 to Register 0xEE.
8. Write 0x84 to Register 0xEF.
9. Write 0x85 to Register 0xEE.
10. Write 0x85 to Register 0xEF.
11. Write 0x86 to Register 0xEE.
12. Write 0x86 to Register 0xEF.
13. Write 0x87 to Register 0xEE.
14. Write 0x87 to Register 0xEF.

JESD204B SYNCHRONIZATION DETAILS

The AD9250 supports JESD204B Subclass 0 and Subclass 1 and establishes synchronization of the link through one or two control signals, SYNC and Subclass 1 also use SYSREF, and a common device clock. SYSREF and SYNC are common to all converter devices for alignment purposes at the system level.

The synchronization process is accomplished over three phases: code group synchronization (CGS), initial lane alignment sequence (ILAS), and data transmission. If scrambling is enabled, scrambling begins with the first data byte following the last alignment character of the ILAS. CGS and ILAS phases are not scrambled.

CGS Phase

In the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver (external logic device) must locate K28.5 characters in its input data stream using clock and data recovery (CDR) techniques.

When in Subclass 1 mode, the receiver locks onto the K28.5 characters. Once detected, the receiver initiates a SYSREF edge so that the AD9250 transmit data establishes a local multiframe clock (LMFC) internally.

The SYSREF edge also resets any sampling edges within the ADC to align sampling instances to the LMFC. This is important to maintain synchronization across multiple devices.

If Subclass 0: at the next receiver's internal clock; if Subclass 1: at the next receiver's LMFC boundary, the receiver or logic device de-asserts the SYNC~ signal (SYNCINB± goes high), and the transmitter block begins the ILAS phase.

ILAS Phase

In the ILAS phase, the transmitter sends out a known pattern, and the receiver aligns all lanes of the link and verifies the parameters of the link.

The ILAS phase begins after SYNC~ has been de-asserted (goes high). If Subclass 0: the transmitter begins ILAS at the next transmitter's internal clock; if Subclass 1: at the next transmitter's internal LMFC boundary, the transmit block begins to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted. The four multiframes include the following:

- Multiframe 1: Begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2: Begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (see Table 10), and ends with an /A/ character. Many of the parameters values are of the notation of the value − 1.
- Multiframe 3: Is the same as Multiframe 1.
- Multiframe 4: Is the same as Multiframe 1.

Data Transmission Phase

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame.
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC.

Table 10. Fourteen Configuration Octets of the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD			CF[4:0]				
11	Reserved, Don't Care							
12	Reserved, Don't Care							
13	FCHK[7:0]							

LINK SETUP PARAMETERS

The following demonstrates how to configure the AD9250 JESD204B interface paremeters. These details are a subset of the setup details provided in the Synchronization section. The steps to configure the output include the following:

1. Disable lanes before changing the configuration.
2. Select the quick configuration option.
3. Configure the detailed options.
4. Check FCHK, checksum of JESD204B interface parameters.
5. Set the additional digital output configuration options.
6. Re-enable lane(s).

Disable Lanes Before Changing Configuration

Before modifying the JESD204B link parameters, disable the link and hold it in reset. This is accomplished by writing Logic 1 to Register 0x5F, Bit 0.

Select Quick Configuration Option

Write to Register 0x5E, the 204B quick configuration register to select the configuration options. See Table 13 for configuration options and resulting JESD204B parameter values.

- 0x11 = one converter, one lane
- 0x12 = one converter, two lanes
- 0x21 = two converters, one lane
- 0x22 = two converters, two lanes

Configure Detailed Options

Configure the tail bits and control bits.

- With N' = 16 and N = 14, there are two bits available per sample for transmitting additional information over the JESD204B link. The options are tail bits or control bits. By default, tail bits of 0b00 value are used.
- Tail bits are dummy bits sent over the link to complete the two octets and do not convey any information about the input signal. Tail bits can be fixed zeros (default) or psuedo random numbers (Register 0x5F, Bit 6).
- One or two control bits can be used instead of the tail bits through Register 0x72, Bits[7:6]. The tail bits can be set using Register 0x14, Bits[7:5], and can be enabled using Address 0x5F, Bit 6.

Set lane identification values.

- JESD204B allows parameters to identify the device and lane. These parameters are transmitted during the ILAS phase, and they are accessible in the internal registers.
- There are three identification values: device identification (DID), bank identification (BID), and lane identification (LID). DID and BID are device specific; therefore, they can be used for link identification.

Set number of frames per multiframe, K

- Per the JESD204B specification, a multiframe is defined as a group of K successive frames, where K is between 1 and 32, and it requires that the number of octets be between 17 and 1024. The K value is set to 32 by default in Register 0x70, Bits[7:0]. Note that Register 0x70 represents a value of K − 1.
- The K value can be changed; however, it must comply with a few conditions. The AD9250 uses a fixed value for octets per frame [F] based on the JESD204B quick configuration setting. K must also be a multiple of 4 and conform to the following equation.

$$32 \geq K \geq Ceil\ (17/F)$$

- The JESD204B specification also calls for the number of octets per multiframe (K × F) to be between 17 and 1024. The F value is fixed through the quick configuration setting to ensure this relationship is true.

Table 11. JESD204B Configurable Identification Values

DID Value	Register, Bits	Value Range
LID (Lane 0)	0x66, [4:0]	0…31
LID (Lane 1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255
BID	0x65, [3:0]	0…15

Scramble, SCR.

- Scrambling can be enabled or disabled by setting Register 0x6E, Bit 7. By default, scrambling is enabled. Per the JESD204B protocol, scrambling is only functional after the lane synchronization has completed.

Select lane synchronization options.

Most of the synchronization features of the JESD204B interface are enabled by default for typical applications. In some cases, these features can be disabled or modified as follows:

- ILAS enabling is controlled in Register 0x5F, Bits[3:2] and by default is enabled. Optionally, to support some unique instances of the interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to either disable the ILAS sequence or continually repeat the ILAS sequence.

The AD9250 has fixed values of some of the JESD204B interface parameters, and they are as follows:

- [N] = 14: number of bits per converter is 14, in Register 0x72, Bits[4:0]; Register 0x72 represents a value of N − 1.
- [N'] = 16: number of bits per sample is 16, in Register 0x73, Bits[4:0]; Register 0x73 represents a value of N' − 1.
- [CF] = 0: number of control words/ frame clock cycle/converter is 0, in Register 0x75, Bits[4:0].

Verify read only values: lanes per link (L), octets per frame (F), number of converters (M), and samples per converter per frame (S). The AD9250 calculates values for some JESD204B parameters based on other settings, particularly the quick configuration register selection. The read only values here are available in the register map for verification.

- [L] = lanes per link can be 1 or 2, read the values from Register 0x6E, Bit 0
- [F] = octets per frame can be 1, 2, or 4, read the value from Register 0x6F, Bits[7:0]
- [HD] = high density mode can be 0 or 1, read the value from Register 0x75, Bit 7
- [M] = number of converters per link can be 1 or 2, read the value from Register 0x71, Bits[7:0]
- [S] = samples per converter per frame can be 1 or 2, read the value from Register 0x74, Bits[4:0]

Check FCHK, Checksum of JESD204B Interface Parameters

The JESD204B parameters can be verified through the checksum value [FCHK] of the JESD204B interface parameters. Each lane has a FCHK value associated with it. The FCHK value is transmitted during the ILAS second multiframe and can be read from the internal registers.

The checksum value is the modulo 256 sum of the parameters listed in the No. column of Table 12. The checksum is calculated by adding the parameter fields before they are packed into the octets shown in Table 12.

The FCHK for the lane configuration for data coming out of Lane 0 can be read from Register 0x78. Similarly, the FCHK for the lane configuration for data coming out of Lane 1 can be read from Register 0x79.

Table 12. JESD204B Configuration Table Used in ILAS and CHKSUM Calculation

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N′[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				

Additional Digital Output Configuration Options

Other data format controls include the following:

- Invert polarity of serial output data: Register 0x60, Bit 1.
- ADC data format (offset binary or twos complement): Register 0x14, Bits[1:0].
- Options for interpreting single on SYSREF± and SYNCINB±: Register 0x3A. See Table 14 for additional descriptions of Register 0x3A controls.
- Option to remap converter and lane assignments, Register 0x82 and Register 0x83. See Figure 54 for simplified block diagram.

Re-Enable Lanes After Configuration

After modifying the JESD204B link parameters, enable the link so that the synchronization process can begin. This is accomplished by writing Logic 0 to Register 0x5F, Bit 0.

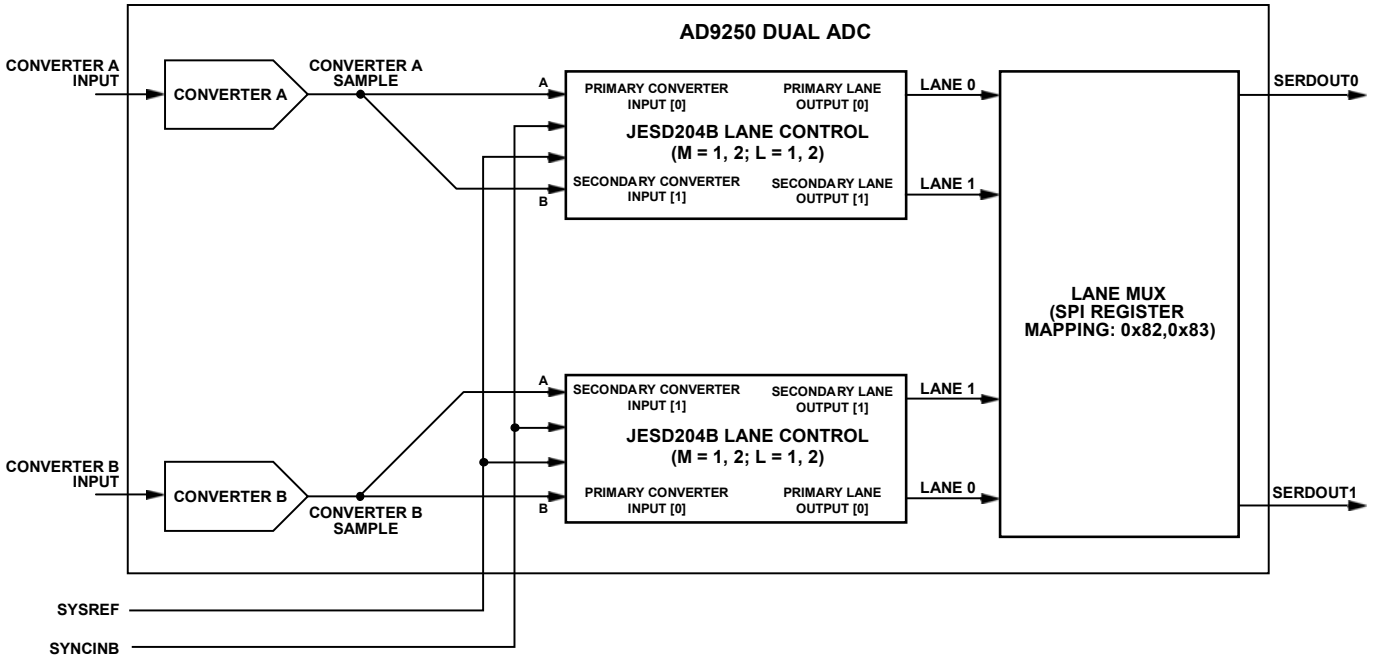


Figure 54. AD9250 Transmit Link Simplified Block Diagram

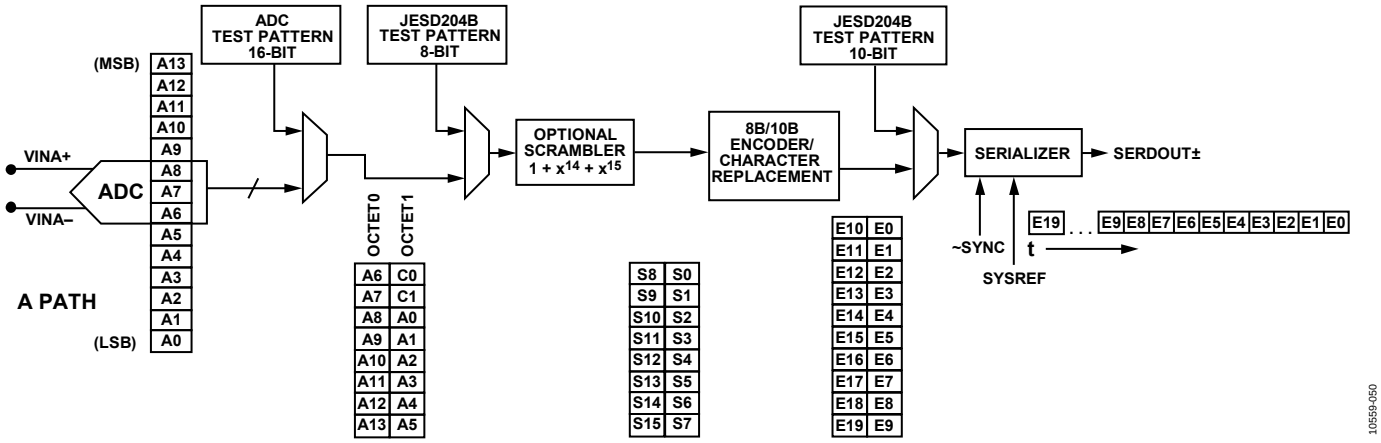


Figure 55. AD9250 Digital Processing of JESD204B Lanes

Table 13. AD9250 JESD204B Typical Configurations

JESD204B Configure Setting	M (No. of Converters), Register 0x71, Bits[7:0]	L (No. of Lanes), Register 0x6E, Bit 0	F (Octets/Frame), Register 0x6F, Bits[7:0], Read Only	S (Samples/ADC/Frame), Register 0x74, Bits[4:0], Read Only	HD (High Density Mode), Register 0x75, Bit 7, Read Only
0x11	1	1	2	1	0
0x12	1	2	1	1	1
0x21	2	1	4	1	0
0x22 (Default)	2	2	2	1	0

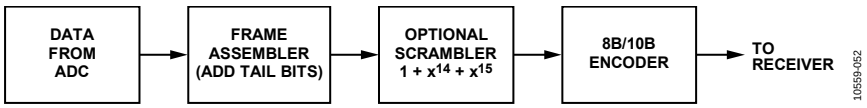


Figure 56. AD9250 ADC Output Data Path

Table 14. AD9250 JESD204B Configuration, Register 0x3A

Bit No.	Register Description	Functional Description
0	Enable internal SYSREF buffer	This bit controls the on-chip buffer for the SYSREF singal. By default, this bit is 0, which disables the buffer. If the AD9250 is configured for JESD204B Subclass 1 operation, SYSREF is required to align the JESD204B link and this bit must be set to 1. To avoid a false trigger as a result of transients caused when enabling the buffer (particularly for one-shot SYSREF configuration), set this bit first and then in a consecutive SPI register write, configure all remaining bits in Register 0x3A to the desired JESD204B link configuration, including keeping this bit at 1. A setting of 0 (default) gates the SYSREF signal such that the internal logic is not affected by an external SYSREF. Set this bit to 0 when in Subclass 0, that is, when SYSREF is not used. If using Subclass 1 with one-shot SYSREF mode, enable the buffer while the SYSREF is established, but then disable it during normal operation. If using Subclass 1 with continuous SYSREF mode, the buffer must remain enabled for normal operation.
1	SYSREF± enable	This bit enables the circuitry that uses the SYSREF input signal and must be on to enable Subclass 1 operation. Set this bit to 1 when using JESD204B Subclass 1 operation. This bit is self clearing after a valid SYSREF occurs when SYSREF± mode (Register 0x3A, Bit 2) is set to 1 (configured for one-shot SYSREF operation). Note that SYSREF is still used in some digital circuitry even if this bit is 0; to disable the SYSREF signal internally, Register 0x3A Bit 0 must be set to 0.
2	SYSREF± mode	This bit is used in Subclass 1 operation to define one shot or continuous SYSREF mode. To configure continuous (or gapped periodic) SYSREF, this bit is set to 0. For one-shot operation, this bit is set to 1. In one-shot mode, it is recommended that the SYSREF buffer be disabled after SYSREF has occurred by setting Register 0x3A, Bit 0 to 0.
3	Realign on SYSREF; forSubclass 1 only	When this bit is set to 1, the internal clock alignment for the JESD204B timing is forced when an active SYSREF occurs. This is recommended only for one-shot mode and must only be done prior to initially establishing a link. This resets the JESD204B link on active SYSREF and requires additional clock alignment register writes after realignment to set up timing margin over temperature properly. See the Synchronization section for the clock alignment procedure. For continuous SYSREF mode, this bit must be set to 0 during normal operation.
4	Realign on SYNCB; for Subclass 1 only	When this bit is set to 1, the internal clock alignment for the JESD204B timing is forced when an active SYNC occurs. An active SYNC requires the SYNCINB input to be logic low for at least four consecutive LMFCs.

Table 15. AD9250 JESD204B Frame Alignment Monitoring and Correction Replacement Characters

Scrambling	Lane Synchronization	Character to be Replaced	Last Octet in Multiframe	Replacement Character
Off	On	Last octet in frame repeated from previous frame	No	K28.7
Off	On	Last octet in frame repeated from previous frame	Yes	K28.3
Off	Off	Last octet in frame repeated from previous frame	Not applicable	K28.7
On	On	Last octet in frame equals D28.7	No	K28.7
On	On	Last octet in frame equals D28.3	Yes	K28.3
On	Off	Last octet in frame equals D28.7	Not applicable	K28.7

FRAME AND LANE ALIGNMENT MONITORING AND CORRECTION

Frame alignment monitoring and correction is part of the JESD204B specification. The 14-bit word requires two octets to transmit all the data. The two octets (MSB and LSB), where F = 2, make up a frame. During normal operating conditions, frame alignment is monitored via alignment characters, which are inserted under certain conditions at the end of a frame. Table 15 summarizes the conditions for character insertion along with the expected characters under the various operation modes. If lane synchronization is enabled, the replacement character value depends on whether the octet is at the end of a frame or at the end of a multiframe.

Based on the operating mode, the receiver can ensure that it is still synchronized to the frame boundary by correctly receiving the replacement characters.

DIGITAL OUTPUTS AND TIMING

The AD9250 has differential digital outputs that power up by default. The driver current is derived on-chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV peak-to-peak swing at the receiver (see Figure 57). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

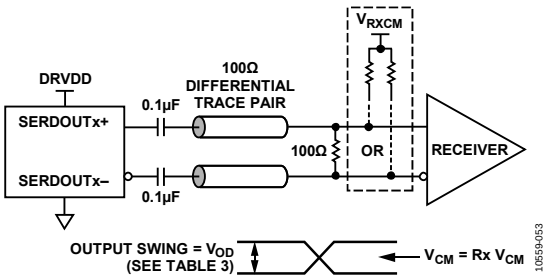


Figure 57. AC-Coupled Digital Output Termination Example

The AD9250 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of the receiver (that is, the common-mode voltage is 0.9 V for a receiver supply of 1.8 V) if dc-coupled connecting is used (see Figure 58). For receiver logic that is not within the bounds of the DRVDD supply, use an ac-coupled connection. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

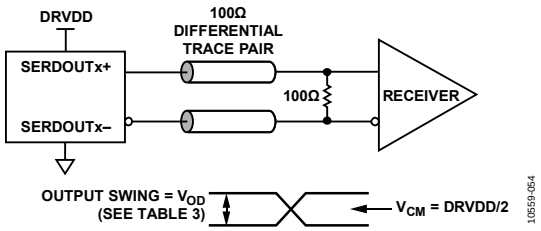


Figure 58. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 59 shows an example of the digital output (default) data eye and time interval error (TIE) jitter histogram and bathtub curve for the AD9250 lane running at 5 Gbps.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer trace lengths (see Register 0x15 in Table 17). The power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is twos complement by default. To change the output data format to offset binary, see the Memory Map section (Register 0x14 in Table 17).

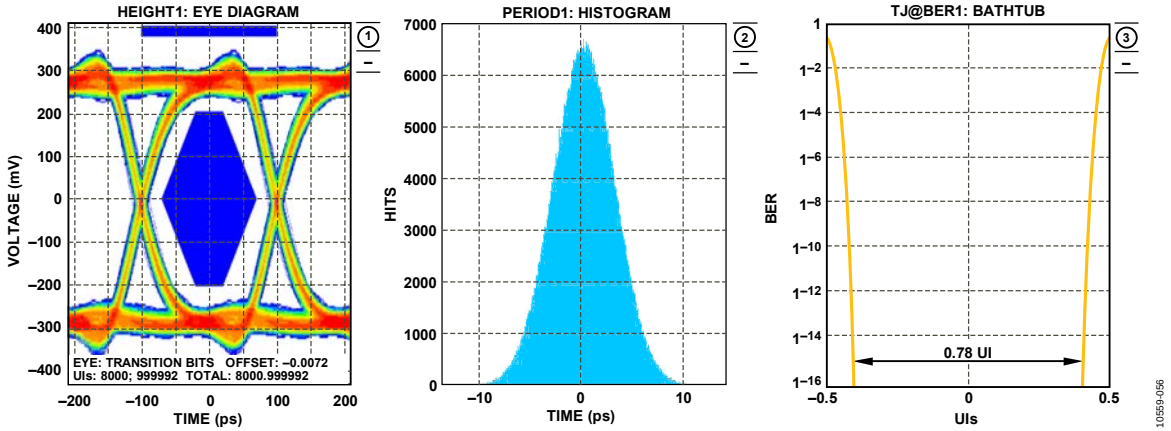


Figure 59. AD9250 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations at 5 Gbps

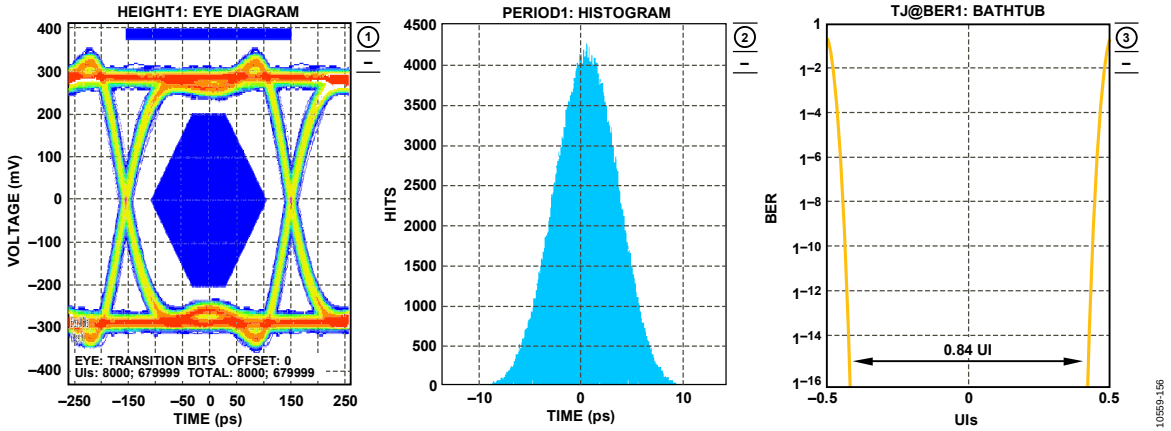


Figure 60. AD9250 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations at 3.4 Gbps

ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides delayed information on the state of the analog input that is of limited value in preventing clipping. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip occurs. In addition, because input signals can have significant slew rates, latency of this function is of concern.

Using the SPI port, the user can provide a threshold above which the FD output is active. Bit 0 of Register 0x45 enables the fast detect feature. Register 0x47 to Register 0x4A allow the user to set the threshold levels. As long as the signal is below the selected threshold, the FD output remains low. In this mode, the magnitude of the data is considered in the calculation of the condition, but the sign of the data is not considered. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 36 ADC clock cycles. An overrange at the input is indicated by this bit 36 clock cycles after it occurs.

GAIN SWITCHING

The AD9250 includes circuitry that is useful in applications either where large dynamic ranges exist, or where gain ranging amplifiers are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

Fast Threshold Detection (FDA and FDB)

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located in Register 0x47 and Register 0x48. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 7 clock cycles. The approximate upper threshold magnitude is defined by

$$Upper\ Threshold\ Magnitude\ (\text{dBFS}) = 20 \log (Threshold\ Magnitude/2^{13})$$

Or, alternatively, the register value can be calculated by the target threshold using the following equation:

$$Value = 10^{(Threshold\ Magnitude\ [\text{dBFS}]/20)} \times 2^{13}$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x49 and Register 0x4A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$Lower\ Threshold\ Magnitude\ (\text{dBFS}) = 20 \log (Threshold\ Magnitude/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0x0FFF to those registers; and to set a lower threshold of −10 dBFS, write 0x0A1D to those registers.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located in Register 0x4B and Register 0x4C.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 61.

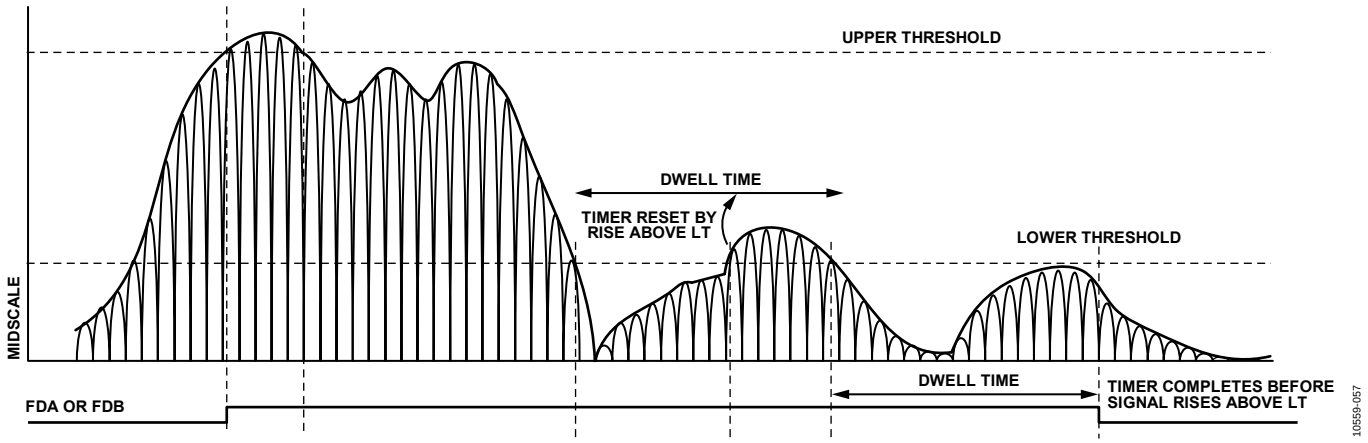


Figure 61. Threshold Settings for FDA and FDB Signals

DC CORRECTION

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path; however, this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

DC CORRECTION BANDWIDTH

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.29 Hz and 2.387 kHz at 245.76 MSPS). The bandwidth is controlled by writing to the 4-bit dc correction bandwidth select register, located at Register 0x40, Bits[5:2]. The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC\_Corr\_BW = 2^{-k-14} \times f_{CLK}/(2 \times \pi)$$

where:
k is the 4-bit value programmed in Bits[5:2] of Register 0x40 (values between 0 and 13 are valid for k).
f_{CLK} is the AD9250 ADC sample rate in hertz.

DC CORRECTION READBACK

The current dc correction value can be read back in Register 0x41 and Register 0x42 for each channel. The dc correction value is a 16-bit value that can span the entire input range of the ADC.

DC CORRECTION FREEZE

Setting Bit 6 of Register 0x40 freezes the dc correction at its current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

DC CORRECTION (DCC) ENABLE BITS

Setting Bit 1 of Register 0x40 enables dc correction for use in the output data signal path.

SERIAL PORT INTERFACE (SPI)

The AD9250 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the $\overline{CS}$ pin (see Table 16). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The $\overline{CS}$ (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 16. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface, reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
$\overline{CS}$	Chip Select Bar. An active low control that gates the read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 62 and Table 5.

Other modes involving the $\overline{CS}$ are available. The $\overline{CS}$ can be held low indefinitely, which permanently enables the device; this is called streaming. The $\overline{CS}$ can stall high between bytes to allow for additional external timing. When $\overline{CS}$ is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and the W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 16 comprise the physical interface between the user programming device and the serial port of the AD9250. The SCLK pin and the $\overline{CS}$ pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the $\overline{CS}$ signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9250 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 17 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9250 part-specific features are described in the Memory Map Register Description section.

Table 17. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage

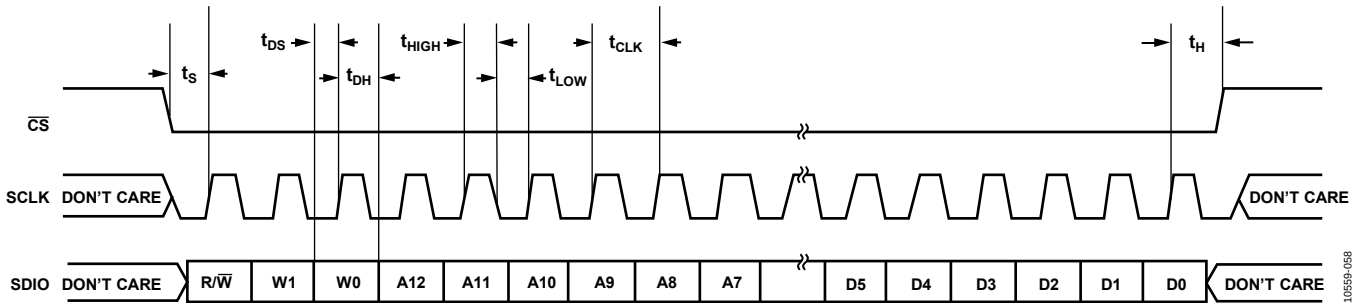


Figure 62. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0xA8).

The memory map register table (see Table 18) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x25. The remaining registers, Register 0x3A and Register 0x59, are documented in the Memory Map Register Description section.

Open and Reserved Locations

All address and bit locations that are not included in Table 18 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), do not write to this address location.

Default Values

After the AD9250 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 18.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x09, Address 0x0B to Address 0x14, Address 18, Address 3A, Address 0x40 to Address 0x4C are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 18 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 18 affect the entire part and the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 18 are not currently supported for this device.

Table 18. Memory Map Registers

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x00	Global SPI config	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	
0x01	CHIP ID	AD9250 8-bit chip ID is 0xB9								0xB9	Read only
0x02	Chip info			Speed grade 00 = 250 MSPS 11 = 170 MSPS			Reserved for chip die revision currently 0x0			0x00 or 0x30	
0x05	Channel index							SPI write to ADC B path	SPI write to ADC A path	0x03	
0x08	PDWN modes			External PDWN mode; 0 = PDWN is full power down; 1 = PDWN puts device in standby	JTX in standby; 0 = JESD204B core is unaffected in standby; 1 = JESD204B core is powered down except for PLL during standby	JESD204B power modes; 00 = normal mode (power up); 01 = power-down mode: PLL off, serializer off, clocks stopped, digital held in reset; 10 = standby mode: PLL on, serializer off, clocks stopped, digital held in reset		Chip power modes; 00 = normal mode (power up); 01 = power-down mode, digital datapath clocks disabled, digital datapath held in reset; most analog paths powered off; 10 = standby mode; digital datapath clocks disabled, digital datapath held in reset, some analog paths powered off (Local)		0x00	
0x09	Global clock	Reserved		Clock selection: 00 = Nyquist clock 10 = RF clock divide by 4 11 = clock off					Clock duty cycle stabilizer enable	0x01	DCS enabled if clock divider enabled
0x0A	PLL status	PLL locked status							JESD204B link is ready		Read only
0x0B	Global clock divider			Clock divider phase output of the internal divide by 1 to divide by 8 divider circuit, clock cycles are relative to the input clock to this block; 0x0 = 0 input clock cycles delayed; 0x1 = 1 input clock cycles delayed; 0x2 = 2 input clock cycles delayed; … 0x7 = 7 input clock cycles delayed Note that the RF clock divider phase is not selectable			Clock divider ratio of the divide by 1 to divide by 8 divider circuit to generate the encode clock; 0x00 = divide by 1; 0x01 = divide by 2; 0x02 = divide by 3; … 0x7 = divide by 8; using a CLKDIV_DIVIDE_RATIO > 0 (Divide Ratio > 1) causes the DCS to be automatically enabled		0x00	
0x0D	Test control reg	User test mode cycle; 00 = repeat pattern (user pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, …); 10 = single pattern (user pattern 1, 2, 3, 4, then all zeros) (Local)		Long psuedo random number generator reset; 0 = long PRN enabled; 1 = long PRN held in reset (Local)	Short psuedo random number generator reset; 0 = short PRN enabled; 1 = short PRN held in reset (Local)	Data output test generation mode; 0000 = off (normal mode); 0001 = midscale short; 0010 = positive full scale; 0011 = negative full scale; 0100 = alternating checkerboard; 0101 = PN23 sequence long; 0110 = PN9 sequence short; 0111 = one-/zero-word toggle; 1000 = user test mode (use with Register 0x0D, Bit 7 and user pattern 1, 2, 3, 4); 1001 to 1110 = unused; 1111 = ramp output (Local)				0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x10	Customer offset	Offset adjust in LSBs from +31 to −32 (twos complement format); 01 1111 = adjust output by +31; 01 1110 = adjust output by +30; … 00 0001 = adjust output by +1; 00 0000 = adjust output by 0 (default); … 10 0001 = adjust output by −31; 10 0000 = adjust output by −32 (Local)								0x00	
0x14	Output mode	JTX CS bits assignment (in conjunction with Register 0x72) 000 = (overrange||underrange, valid) 001 = (overrange||underrange) 010 = (overrange||underrange, blank) 011 = (blank, valid) 100 = (blank, blank) All others = (overrange||underrange, valid)			Disable output from ADC		Invert ADC data; 0 = normal (default); 1 = inverted (Local)	Digital datapath output data format select (DFS) (local); 00 = offset binary; 01 = twos complement (Local)		0x01	
0x15	CML output adjust						JESD204B CML differential output drive level adjustment; 000 = 81% of nominal (that is, 478 mV); 001 = 89% of nominal (that is, 526 mV); 010 = 98% of nominal (that is, 574 mV); 011 = nominal (default) (that is, 588 mV); 110 = 126% of nominal (that is, 738 mV)			0x03	
0x18	ADC VREF				Main reference full-scale VREF adjustment; 0 1111 = internal 2.087 V p-p; … 0 0001 = internal 1.772 V p-p; 0 0000 = internal 1.75 V p-p (default); 1 1111 = internal 1.727 V p-p; … 1 0000 = internal 1.383 V p-p					0x00	
0x19	User Test Pattern 1 L	User Test Pattern 1 LSB; use in conjunction with Register 0x0D and Register 0x61								0x00	
0x1A	User Test Pattern 1 M	User Test Pattern 1 MSB								0x00	
0x1B	User Test Pattern 2 L	User Test Pattern 2 LSB								0x00	
0x1C	User Test Pattern 2 M	User Test Pattern 2 MSB								0x00	
0x1D	User Test Pattern 3 L	User Test Pattern 3 LSB								0x00	
0x1E	User Test Pattern 3 M	User Test Pattern 3 MSB								0x00	
0x1F	User Test Pattern 4 L	User Test Pattern 4 LSB								0x00	
0x20	User Test Pattern 4 M	User Test Pattern 4 MSB								0x00	
0x21	PLL low encode				00 = for lane speeds > 2 Gbps; 01 = for lane speeds < 2 Gbps					0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x3A	SYNCINB±/ SYSREF± CTRL				SYNCINB± OPERATION 0 = normal mode; 1 = realign lanes on every active SYNCINB±	For Subclass 1 Only: 0 = normal mode; 1 = realign lanes on every active SYSREF±; use with single shot SYSREF in Subclass 1 mode	SYSREF± mode; 0 = continuous reset clock dividers; 1 = sync on next SYSREF± rising edge only	SYSREF± enable; 0 = disabled; 1 = enabled. NOTE: This bit self-clears after SYSREF if SYSREF± mode = 1	Enable internal SYSREF± buffer; 0 = buffer disabled, external SYSREF± pin ignored; 1 = buffer enabled, use external SYSREF± pin	0x00	See Table 14 for more details
0x40	DCC CTRL		Freeze dc correction; 0 = calculate; 1 = freezeval	DC correction bandwidth select; correction bandwidth is 2387.32 Hz/reg val; there are 14 possible values; 0000 = 2387.32 Hz; 0001 = 1193.66 Hz; 1101 = 0.29 Hz				Enable DCC		0x00	
0x41	DCC value LSB	DC Correction Value[7:0]								0x00	
0x42	DCC value MSB	DC Correction Value[15:8]								0x00	
0x45	Fast detect control				Pin function; 0 = fast detect; 1 = overrange	Force FDA/FDB pins; 0 = normal function; 1 = force to value	Force value of FDA/FDB pins if force pins is true, this value is output on FD pins		Enable fast detect output	0x00	
0x47	FD upper threshold	Fast Detect Upper Threshold[7:0]								0x00	
0x48	FD upper threshold		Fast Detect Upper Threshold[14:8]							0x00	
0x49	FD lower threshold	Fast Detect Lower Threshold[7:0]								0x00	
0x4A	FD lower threshold		Fast Detect Lower Threshold[14:8]							0x00	
0x4B	FD dwell time	Fast Detect Dwell Time[7:0]								0x00	
0x4C	FD dwell time	Fast Detect Dwell Time[15:8]								0x00	
0x5E	204B quick config	Quick configuration register, always reads back 0x00; 0x11 = M = 1, L = 1; one converter, one lane; second converter is not automatically powered down; 0x12 = M = 1, L = 2; one converter, two lanes; second converter is not automatically powered down; 0x21 = M = 2, L = 1; two converters, one lane; 0x22 = M = 2, L = 2; two converters, two lanes								0x00	Always reads back 0x00
0x5F	204B Link CTRL 1		Tail bits: If CS bits are not enabled; 0 = extra bits are 0; 1 = extra bits are 9-bit PN	JESD204B test sample enabled	Reserved; set to 1	ILAS mode; 01 = ILAS normal mode enabled; 11 = ILAS always on, test mode		Reserved; set to 0	Power-down JESD204B link; set high while configuring link parameters	0x14	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x60	204B Link CTRL 2	Reserved; set to 0	Reserved; set to 0	Reserved; set to 0				Invert logic of JESD204B bits		0x00	
0x61	204B Link CTRL 3	Reserved; set to 0	Reserved; set to 0	Test data injection point; 01 = 10-bit data at 8B/10B output; 10 = 8-bit data at scrambler input		JESD204B test mode patterns; 0000 = normal operation (test mode disabled); 0001 = alternating checker board; 0010 = 1/0 word toggle; 0011 = PN sequence PN23; 0100 = PN sequence PN9; 0101= continuous/repeat user test mode; 0110 = single user test mode; 0111 = reserved; 1000 = modified RPAT test sequence, must be used with JTX_TEST_GEN_SEL = 01 (output of 8b/10b); 1100 = PN sequence PN7; 1101 = PN sequence PN15; other setting are unused				0x00	
0x62	204B Link CTRL 4	Reserved								0x00	
0x63	204B Link CTRL 5	Reserved								0x00	
0x64	204B DID config	JESD204B DID value								0x00	
0x65	204B BID config					JESD204B BID value				0x00	
0x66	204B LID Config 0				Lane 0 LID value					0x00	
0x67	204B LID Config 1				Lane 1 LID value					0x01	
0x6E	204B parameters SCR/L	JESD204B scrambling (SCR); 0 = disabled; 1 = enabled							JESD204B lanes (L); 0 = 1 lane; 1 = 2 lanes	0x81	
0x6F	204B parameters F	JESD204B number of octets per frame (F); calculated value (Note that this value is in x – 1 format)								0x01	Read Only
0x70	204B parameters K	JESD204B number of frames per multiframe (K); set value of K per JESD204B specifications, but also must be a multiple of 4 octets (Note that this value is in x – 1 format)								0x1F	
0x71	204B parameters M	JESD204B number of converters (M); 0 = 1 converter; 1 = 2 converters								0x01	
0x72	204B parameters CS/N	Number of control bits (CS); 00 = no control bits (CS = 0); 01 = 1 control bit (CS = 1); 10 = 2 control bits (CS = 2)				ADC converter resolution (N), 0xD = 14-bit converter (N = 14) (Note that this value is in x – 1 format)				0x0D	
0x73	204B parameters subclass/Np		JESD204B subclass; 0x0 = Subclass 0; 0x1 = Subclass 1 (default)			JESD204B N′ value; 0xF = N′ = 16 (Note that this value is in x – 1 format)				0x2F	
0x74	204B parameters S			Reserved; set to 1	JESD204B samples per converter frame cycle (S); read only (Note that this value is in x – 1 format)					0x20	
0x75	204B parameters HD and CF	JESD204B HD value; read only			JESD204B control words per frame clock cycle per link (CF); read only					0x00	Read Only
0x76	204B RESV1	Reserved Field Number 1								0x00	
0x77	204B RESV2	Reserved Field Number 2								0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x78	204B CHKSUM0	JESD204B serial checksumvalue for Lane 0								0x42	
0x79	204B CHKSUM1	JESD204B serial checksumvalue for Lane 1								0x43	
0x82	204B Lane Assign 1			00 = assign Logical Lane 0 to Physical Lane A (default); 01 = assign Logical Lane 0 to Physical Lane B				Reserved; set to 1	Reserved; set to 0	0x02	
0x83	204B Lane Assign 2			Reserved; set to 1	Reserved; set to 1			00 = assign Logical Lane 1 to Physical Lane A; 01 = assign Logical Lane 1 to Physical Lane B (default)		0x31	
0x8B	204B LMFC offset				Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase counter when SYSREF is asserted; used for deterministic delay applications					0x00	
0xA8	204B pre-emphasis	JESD204B pre-emphasis enable option (consult factory for more detail); set value to 0x04 for pre-emphasis off; set value to 0x14 for pre-emphasis on								0x04	Typically not required
0xEE	Internal digital clock delay	Enable internal clock delay	Set to 0	Set to 0	Set to 0	Use incrementing values from 0 to 7 to increase internal digital clock delay. For internal data latching purposes, this does not affect external timing.				0x00	See JESD Section for use
0xEF	Internal digital clock delay	Enable internal clock delay	Set to 0	Set to 0	Set to 0	Use incrementing values from 0 to 7 to increase internal digital clock delay. For internal data latching purposes, this does not affect external timing.				0x00	See JESD Section for use
0xF3	Internal digital clock alignment			Force manual re-align on Lane 1, self clearing	Lane 1 Alignment complete	Force manual realign on Lane 0, self clearing	Lane 0 alignment complete			0x14	See JESD
0xFF	Device update (global)								Transfer settings		

MEMORY MAP REGISTER DESCRIPTION

For more information on functions controlled in Register 0x00 to Register 0x25, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD9250, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9250, use two separate 1.8 V power supplies. The power supply for AVDD can be isolated and for DVDD and DRVDD it can be tied together, in which case isolation between DVDD and DRVDD is required. Isolation can be achieved using a ferrite bead or an inductor of approximately 1 µH. An unfiltered switching regulator is not recommended for the DRVDD supply as it impacts the performance of the JESD204B serial transmission lines and may result in link problems. Alternately, the JESD204B PHY power (DRVDD) and analog (AVDD) supplies can be tied together, and a separate supply can be used for the digital outputs (DVDD).

The designer can employ several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PC board level and close to the pins of the part with minimal trace length. Each power supply domain must have local high frequency decoupling capacitors. This is especially important for DRVDD and AVDD to maintain analog performance.

When using the AD9250, a single PCB ground plane should be sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. Mate a continuous, exposed (no solder mask) copper plane on the PCB to the AD9250 exposed paddle, Pin 0.

The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

Decouple the VCM pin to ground with a 0.1 µF capacitor, as shown in Figure 40. For optimal channel-to-channel isolation, include a 33 Ω resistor between the AD9250 VCM pin and the Channel A analog input network connection, as well as between the AD9250 VCM pin and the Channel B analog input network connection.

SPI Port

When the full dynamic performance of the converter is required, do not activate the SPI port during periods. Because the SCLK, $\overline{CS}$, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9250 to keep these signals from transitioning at the converter input pins during critical sampling periods.

JESD204B Configuration

This section describes an example of the setup required to configure Subclass 1 operation. This example assumes the input clock is equal to the conversion rate.

1. Provide a stable input clock and power to the AD9250.
2. Disable the JESD204B PHY by setting Register 0x5F to 0x15.
3. Set the quick configuration register, Register 0x5E to load various base configurations based on M and L.
4. Enable internal SYSREF buffer by setting Register 0x3A to Register 0x01.
5. Configure the method of SYSREF operation:
   - For one-shot SYSREF operation, set Register 0x3A to 0x0F
   - For continuous or gapped periodic SYSREF operation, set Register 0x3A to 0x03.
6. Set Register 0xEE and Register 0xEF to a value of 0x80.
7. Set other JESD204B related registers if desired, specifically Register 0x14, Register 0x15, Register 0x21, Register 0x60 to Register 0x67, Register 0x6E, Register 0x70, Register 0x82, Register 0x83, Register 0x8B, and Register 0xA8.
8. Enable the JESD204B PHY by setting Register 0x5F to 0x14.
9. Verify Register 0x0A reads back 0x81 indicating the PLL is locked and the link is ready.
10. Apply the SYSREF synchronization signal to the AD9250.
11. Wait at least 6 LMFCs.
12. If the AD9250 is configured for one-shot SYSREF, it is recommended to disable the internal SYSREF buffer at this point by setting Register 0x3A to 0x04.
13. Perform the clock adjustment writes in the following order:
    a. Write 0x81 to Register 0xEE.
    b. Write 0x81 to Register 0xEF.
    c. Write 0x82 to Register 0xEE.
    d. Write 0x82 to Register 0xEF.
    e. Write 0x83 to Register 0xEE.
    f. Write 0x83 to Register 0xEF.
    g. Write 0x84 to Register 0xEE.
    h. Write 0x84 to Register 0xEF.
    i. Write 0x85 to Register 0xEE.
    j. Write 0x85 to Register 0xEF.
    k. Write 0x86 to Register 0xEE.
    l. Write 0x86 to Register 0xEF.
    m. Write 0x87 to Register 0xEE.
    n. Write 0x87 to Register 0xEF.
14. Wait at least 6 LMFCs.
15. The receiver can now begin the CGS phase of the link.

OUTLINE DIMENSIONS

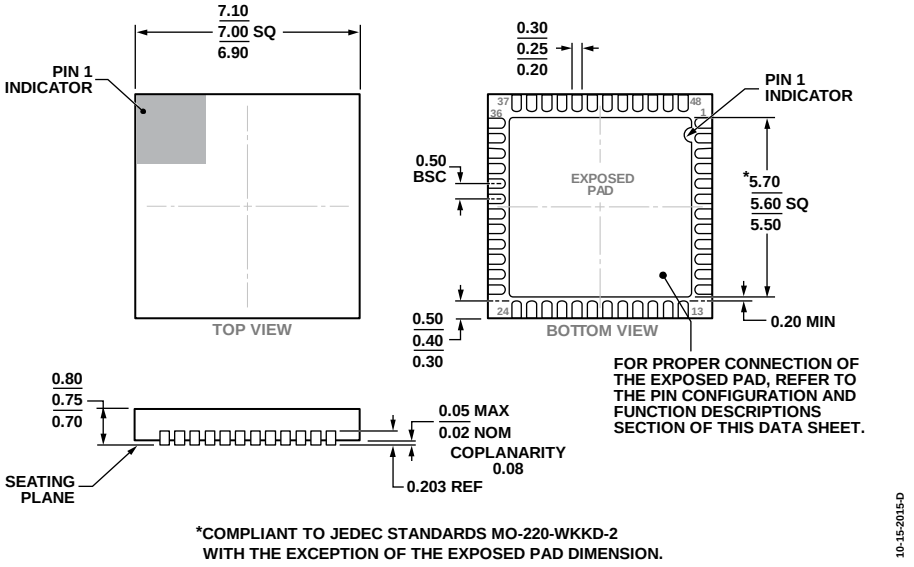


Figure 63. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9250BCPZ-170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9250BCPZRL7-170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9250-170EBZ	−40°C to +85°C	Evaluation Board with AD9250-170	
AD9250BCPZ-250	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9250BCPZRL7-250	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9250-250EBZ	−40°C to +85°C	Evaluation Board with AD9250-250	

[1] Z = RoHS Compliant Part.

NOTES

D10559-0-1/16(C)