MCP9902

Low-Temperature Remote Diode Sensor

Features

- Remote External Temperature Monitor
  - ±1°C maximum accuracy ($-40°C < T_{DIODE} < +65°C$)
  - ±2°C maximum accuracy ($85°C < T_{DIODE} < +125°C$)
  - 0.125°C resolution
- Internal Temperature Monitor
  - ±1°C accuracy
  - 0.125°C resolution
- Supports up to 2.2 nF diode filter capacitor
- Up to 400 kHz clock rate
  - Maskable with register control
- Programmable SMBus address
- Operating voltage: 3.0 to 3.6 (V)
- ESD protection: 2 kV HBM
- Temperature Range: -40°C to +125°C
- Available in a small 8-Lead 2x2 mm WDFN package

Typical Applications

- General Purpose Temperature Sensing
- Industrial Freezers and Refrigerators
- Food Processing
- Base Stations
- Remote Radio Unit

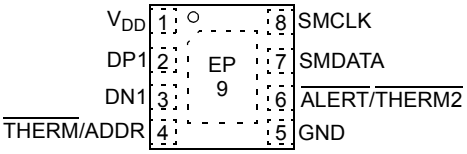
Description

The MCP9902 is a high-accuracy, low-cost, System Management Bus (SMBus) temperature sensor. The MCP9902 monitors an internal and external diode channel. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45 nm, 65 nm and 90 nm processors) and automatic diode-type detection combine to provide a robust solution for complex environmental monitoring applications.

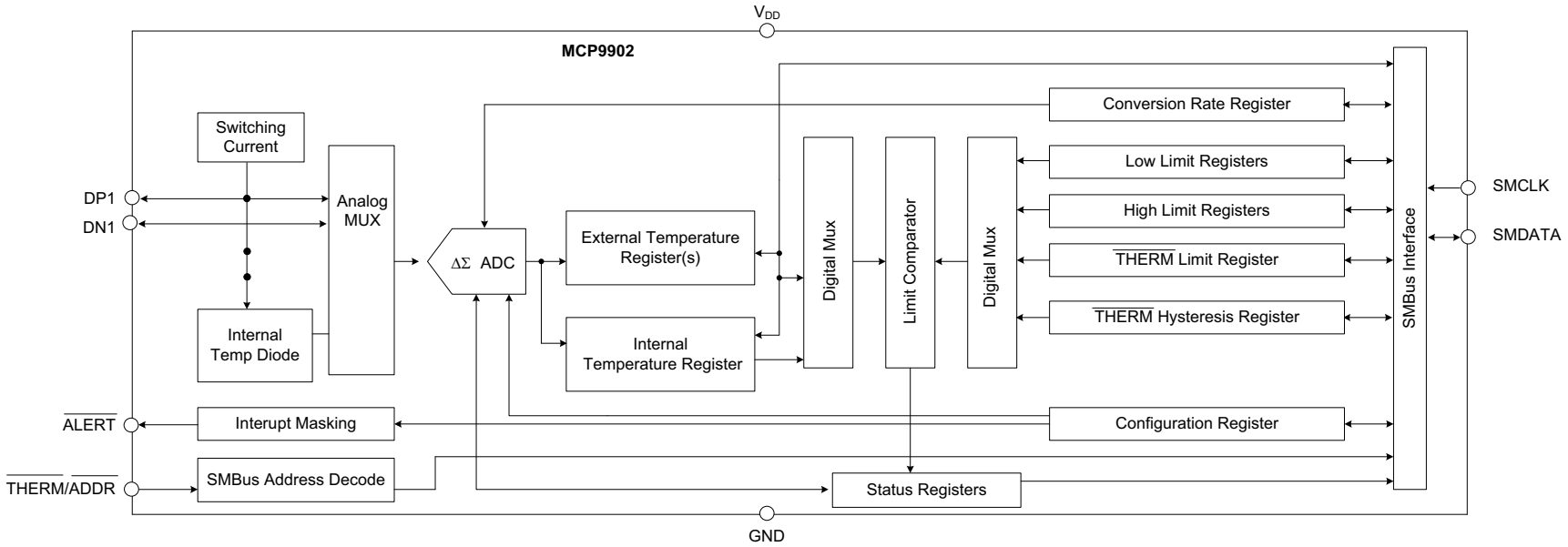
Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus ±1°C measurement accuracy for both external and internal diode temperatures provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Package Type

MCP9902
2 x 2 WDFN*



MCP9902 Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 500 mW
Maximum current out of V_{SS} pin ..... 20 mA
Maximum current into V_{DD} pin ..... 20 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ± 20 mA
ESD Rating, All pins HBM 2000V
Input Current, any pin Except V_{DD} ..... ± 10 mA

† **NOTICE**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability

Note: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$. Rating up to +85°C.

1.2 DC Characteristics

Electrical Characteristics: Unless otherwise specified, 3.0 ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	—
Supply Current	I_{DD}	—	200	450	µA	0.0625 conversion/second, dynamic averaging disabled
		—	225	600	µA	1 conversions/sec, dynamic averaging enabled
		—	450	850	µA	4 conversions/sec, dynamic averaging enabled
		—	1120	1500	µA	≥ 16 conversions/second, dynamic averaging enabled
One-Shot Supply Current	I_{DD_OS}	—	170	230	µA	Device in One-Shot state, no active SMBus communications, ALERT and THERM pins not asserted.
Standby Supply Current	I_{DD_SBY}	—	170	230	µA	Device in Standby state, no SMBus communications, ALERT and THERM pins not asserted.
Power-on Reset Voltage	POR_V	—	0.6	0.9	V	Pin states defined
Power-On Reset Release Voltage	PORR	—	1.45	—	V	Rising V_{DD}
Power-Up Timer	t_{PWRT}	—	10	—	ms	—
V_{DD} Rise Rate	V_{DD_RISE}	0.05	—	—	V/ms	0 to 3V in 60 ms
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	—
Internal Temperature Monitor						
Temperature Accuracy		-1	±0.25	+1	°C	-40°C < T_A < +65°C
		-2	±0.5	+2	°C	—
Temperature Resolution		—	0.125	—	°C	—
External Temperature Monitor						
Temperature Accuracy		-1	±0.25	+1	°C	-40°C < T_{DIODE} < +65°C -40°C < T_A < +65°C
		-2	±0.5	+2	°C	-40°C < T_{DIODE} < +125°C
Temperature Resolution	—	—	0.125	—	°C	—
Timing and Capacitive Filter						
Time to First Communications	t_{INT_T}	—	15	20	ms	Time after power up before ready to begin communications and measure-ment
Conversion Time All Channels	t_{CONV}	—	150	—	ms	Default settings
Time to First Conver-sion from Standby	t_{CONV1}	—	220	—	ms	Default settings
Capacitive Filter	C_{FILTER}	—	2.2	2.7	nF	Connected across external diode

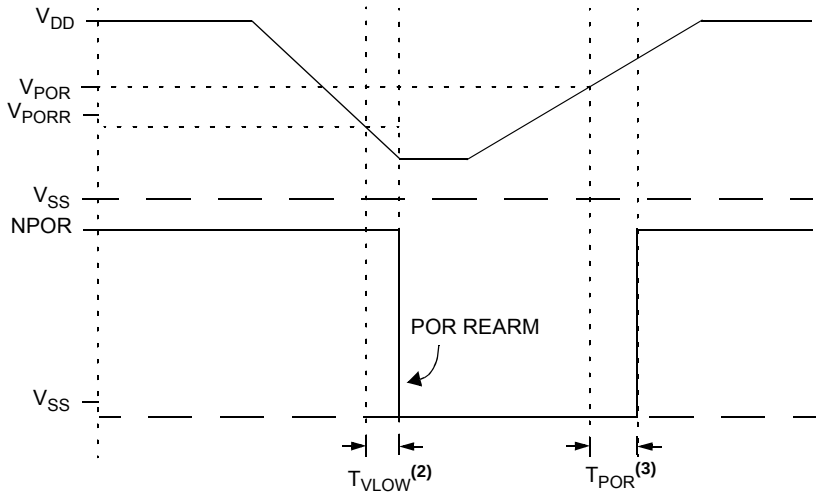
1.2 DC Characteristics (Continued)

Electrical Characteristics: Unless otherwise specified, 3.0 ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Pins						
Output Low Voltage	V_{OL}	0.4	—	—	V	I_{SINK} = 8 mA
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins Device powered or unpowered T_A < +85°C pull-up voltage ≤ 3.6V

1.3 Thermal Specifications

Electrical Characteristics: Unless otherwise specified, 3.0 ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+125	°C	
Thermal Package Resistances (Note)						
Thermal Resistance, 8L-WDFN, 2x2	θ_{JA}	—	141.3	—	°C/W	

Note: JEDEC 2s2p, board size 76.2 x 114.3 x 1.6 mm, 1 via, airflow = 0 m/s.



Note 1: When NPOR is low, the device is held in Reset.
2: T_{POR} 1 µs typical.
3: T_{VLOW} 2.7 µs typical.

FIGURE 1-1: *POR and POR Rearm With Slow Rising V_{DD}.*

1.4 SMBUS Module Specifications

Operating Conditions (unless otherwise indicated): 3.0V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +85°C						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBUS INTERFACE						
Input High Voltage	V_{IH}	2.1	—	V_{DD}	V	—
Input Low Voltage	V_{IL}	-0.3		0.8	V	—
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered T_A < +85°C
Hysteresis		—	0.1 ∗ V_{DD}	—	mV	—
Input Capacitance	C_{IN}	—	5	—	pF	—
Output Low Sink Current	I_{OL}	8.2	—	15	mA	SMDATA = 0.2V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	—
Spike Suppression	t_{SP}	—	—	50	ns	—
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	—
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	—
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	—
Setup Time: Stop	$t_{SU:STO}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When transmitting to the master
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	When receiving from the master
Clock Low Period	t_{LOW}	1.3	—	—	µs	—
Clock High Period	t_{HIGH}	0.6	—	—	µs	—
Clock/Data Fall time	t_{FALL}	—	—	300	ns	—
Clock/Data Rise time	t_{RISE}	—	—	300	ns	Min = 20+0.1 C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Min = 20+0.1 C_{LOAD} ns
Timeout	$t_{TIME-OUT}$	25	—	35	ms	Per bus line
Clock Frequency	f_{SMB}	10	—	400	kHz	Disabled by default

2.0 TYPICAL OPERATING CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated 3.0 ≤ VDD ≤ 3.6V at -40°C ≤ TA ≤ +125°C.

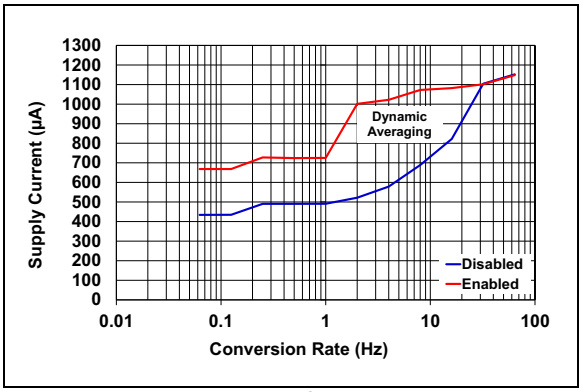


FIGURE 2-1: *Supply Current Vs. Conversion Rate (T_A = +25°C, V_{DD} = 3.3V).*

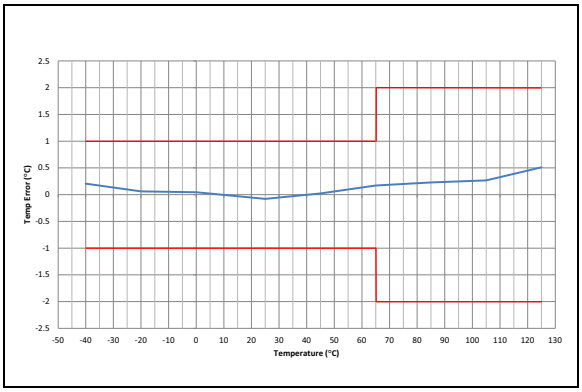


FIGURE 2-4: *Temperature Error Vs. Ambient Temperature (V_{DD} = 3.3V, T_D = 25°C, 16 Units, 2N3904).*

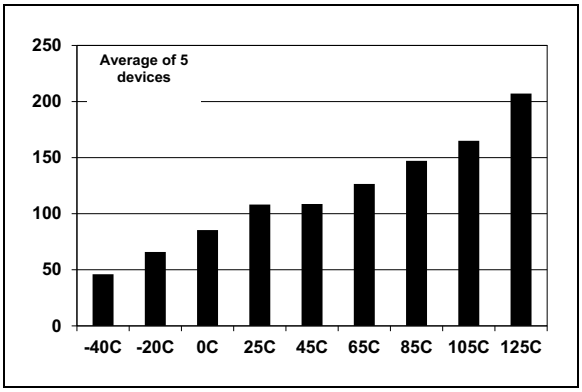


FIGURE 2-2: *I_{DD} Vs. Temperature.*

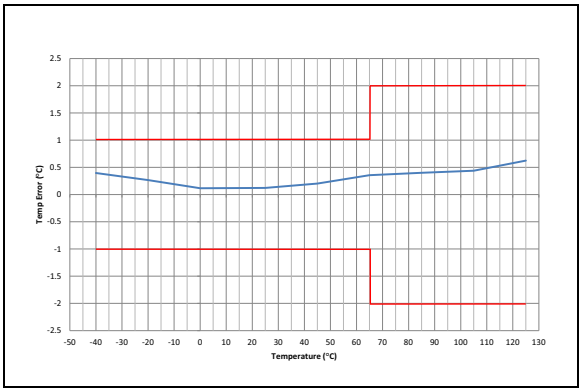


FIGURE 2-5: *Temperature Error Vs. Remote Temperature. (V_{DD} = 3.3V, T_D = 25°C, 16 Units, 2N3904).*

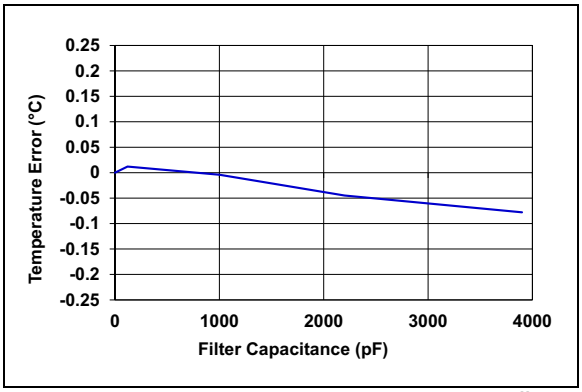


FIGURE 2-3: *Temperature Error Vs. Filter Capacitor (V_{DD} = 3.3V, T_A = T_D = +25°C, 2N3904).*

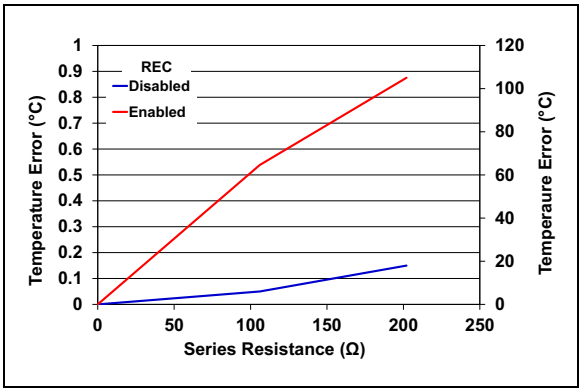


FIGURE 2-6: *Temperature Error Vs. Series Resistance (TA = +25°C, V_{DD} = 3.3V).*

2.1 Pin Descriptions

The MCP9902 has two variants that include features unique to each device. Refer to the table to determine applicability of the pin descriptions.

The description of the pins is listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

MCP9902 WDFN	Pin Name	Pin Type	Description
1	V_{DD}	P	POWER
2	DP1	ANALOG	DIODE ANODE
3	DN1	ANALOG	DIODE CATHODE
4	$\overline{\text{THERM}}$ /ADDR	OD	NON-MASKABLE THERM
5	GND	P	GROUND
6	$\overline{\text{ALERT}}/\overline{\text{THERM2}}$	OD	MASKABLE ALERT/THERM2
7	SMDATA	OD	SMBus CLOCK
8	SMCLK	OD	SMBus DATA
9	EP	—	EXPOSED THERMAL PAD

1: See **Section 2.1.8 "Exposed Thermal Pad (EP)"** for grounding recommendations.

2.1.1 POWER SUPPLY (V_{DD})

This pin is used to supply power to the device.

2.1.2 DIODE THERMAL CONNECTIONS (DN1/DP1)

Remote Diode 1 anode (DP1) and cathode (DN1) pins for the MCP9902.

2.1.3 $\overline{\text{THERM}}$ LIMIT ALERT ($\overline{\text{THERM}}$/ADDR)

This pin asserts low when the hardware-set THERM limit threshold is exceeded by one of the temperature sensors. The assertion of this signal can't be controlled or masked by register setting. If enabled, the SMBus slave address is set by the pull-up resistor on this pin.

2.1.4 GROUND (GND)

This pin is used for system ground for the device.

2.1.5 MASKABLE ALERT ($\overline{\text{ALERT}}/\overline{\text{THERM2}}$)

This pin asserts when a diode temperature exceeds the ALERT threshold. This pin may be masked by register settings.

2.1.6 SMBUS DATA (SMDATA)

This is the open drain, bidirectional data pin for SMBus communication.

2.1.7 SMBUS CLOCK (SMCLK)

This is the SMBus input clock pin for SMBus communication.

2.1.8 EXPOSED THERMAL PAD (EP)

Not internally connected, but recommend grounding for mechanical support.

3.0 FUNCTIONAL DESCRIPTION

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the MCP9902 and using that data to control the speed of one or more fans.

The MCP9902 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceeds user programmable limits. This allows the MCP9902 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. In the second level of monitoring provides a non-maskable interrupt on the $\overline{\text{THERM}}$ output if the measured temperatures meet or exceed a second programmable limit.

Figure 3-1 shows a system level block diagram of the MCP9902.

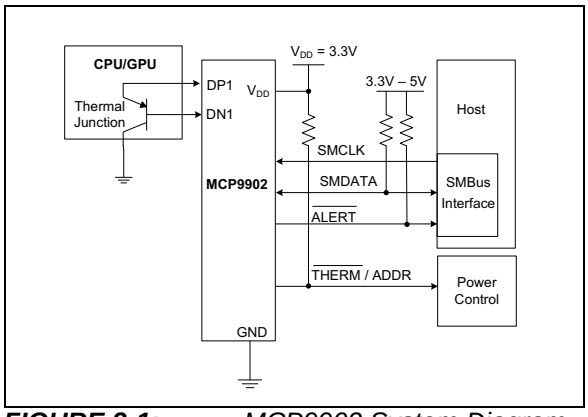


FIGURE 3-1: *MCP9902 System Diagram.*

3.1 Power States

The MCP9902 has two modes of operation:

- Active (Run) - In this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- Standby (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the one-shot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

3.2 Conversion Rates

The MCP9902 may be configured for different conversion rates based on the system requirements. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 3-1.

TABLE 3-1: CONVERSION RATE

CONV<3:0>					Conversions/ Second
HEX	3	2	1	0	
0h	0	0	0	0	1/16
1h	0	0	0	1	1/8
2h	0	0	1	0	1/4
3h	0	0	1	1	1/2
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

3.3 Dynamic Averaging

Dynamic averaging allows the MCP9902 to measure the external diode channel for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Register 4-6). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21 ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the typical supply current based on the chosen conversion rate as shown in the power supply characteristics in **Table 1.2 "DC Characteristics"**.

3.4 THERM Output

The THERM output is asserted independently of the ALERT output and cannot be masked. Whenever any of the measured temperatures exceed the user programmed Therm Limit values for the programmed number of consecutive measurements, the THERM output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the Therm Limit minus the Therm Hysteresis (also programmable).

When the THERM output is asserted, the THERM status bits will likewise be set. Reading these bits will not clear them until the THERM output is deasserted. Once the THERM output is deasserted, the THERM status bits will be automatically cleared.

3.5 THERM Pin Address Decoding

The Address decode is performed by pulling known currents from V_{DD} through the external resistor causing the pin voltage to drop based on the respective current / resistor relationship. This pin voltage is compared against a threshold that determines the value of the pull-up resistor.

The MCP9902-A SMBus slave address is determined by the pull-up resistor on the THERM/ADDR pin as shown in Table 3-2.

TABLE 3-2: SMBUS ADDRESS DECODE

Pull Up Resistor on THERM pin (±5%)	SMBus Address
4.7 kΩ	1111_100 (r/$\overline{w}$)b
6.8 kΩ	1011_100 (r/$\overline{w}$)b
10 kΩ	1001_100 (r/$\overline{w}$)b
15 kΩ	1101_100 (r/$\overline{w}$)b
22 kΩ	0011_100 (r/$\overline{w}$)b
33 kΩ	0111_100 (r/$\overline{w}$)b

The MCP9902-1 SMBus address is hard coded to 1001_100(r/$\overline{w}$).

The MCP9902-2 SMBus address is hard coded to 1001_101(r/$\overline{w}$).

3.6 ALERT/THERM2 Output

3.6.1 ALERT/THERM2 PIN INTERRUPT MODE

When configured to operate in interrupt mode, the ALERT / THERM2 pin asserts low when an out-of-limit measurement (≥ high limit or < low limit) is detected on any diode or when an external diode fault is detected. The ALERT/ THERM2 pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT/THERM2 pin will remain asserted until the appropriate status bits are cleared.

The ALERT/THERM2 pin can be masked by setting the MASK_ALL bit. Once the ALERT/THERM2 pin has been masked, it will be deasserted and remain deasserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the ALERT/THERM2 pin is masked will update the Status Register normally. There are also individual channel masks (see Register 4-20).

The ALERT/THERM2 pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT/THERM2 Outputs can be hard-wired together.

3.6.2 ALERT/THERM2 PIN IN THERM MODE

When the ALERT/THERM2 pin is configured to operate in THERM mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT/THERM2 pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the ALERT/THERM2 pin is asserted in THERM mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT/THERM2 pin is deasserted. Once the ALERT/THERM2 pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the ALERT/THERM2 pin in this mode; however, the individual channel masks (see Register 4-20) will prevent the respective channel from asserting the ALERT/THERM2 pin.

3.7 Temperature Measurement

The MCP9902 monitors the temperature of an internal diode and one external diode.

The device contains programmable High, Low, and Therm limits for all measured temperature channels. If the measured temperature goes below the Low limit or above the High limit, the ALERT/THERM2 pin can be asserted (based on user settings). If the measured temperature meets or exceeds the Therm Limit, the THERM pin is asserted unconditionally, providing two tiers of temperature detection.

3.8 Beta Compensation

The MCP9902 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. For the MCP9902, the external diode channel automatically detects the type of external diode and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately +0.25°C error at +100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately +8.25°C error at +100°C.

Care should be taken when setting the BETA<2:0> bits if the auto-detection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), the BETA<2:0> bits should be set to '111b'.

3.9 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents causes the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e., on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The MCP9902 automatically corrects up to 100 ohms of series resistance.

3.10 Programmable External Diode Ideality Factor

The MCP9902 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the MCP9902 provides a 6-bit register for the external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

These registers store the ideality factors that are applied to the external diode. Table 3-3 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting Microchip.

TABLE 3-3: IDEALITY FACTOR LOOK-UP TABLE (DIODE MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 3-4 when using a CPU substrate transistor.

TABLE 3-4: SUBSTRATE DIODE IDEALITY FACTOR LOOK-UP TABLE (BJT MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408
12h	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

3.11 Diode Faults

The MCP9902 detects several “diode fault” mechanisms, defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN. When each temperature measurement is made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT / THERM2 pin asserts (unless masked, see Register 4-20) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked).

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT / THERM2 pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode-connected transistor), temperature measurements will continue as normal with no alerts.

The External Diode Fault Register (Register 4-19) indicates which of the external diodes caused the FAULT bit in the Status Register to be set. This register is cleared when it is read.

3.12 Consecutive Alerts

The MCP9902 contains multiple consecutive alert counters. One set of counters applies to the ALERT/THERM2 pin and the second set of counters applies to the THERM pin. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT/THERM2 and THERM pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

The Consecutive Alert Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT/THERM2 or THERM pin is asserted. Additionally, the Consecutive Alert Register controls the SMBus Time-out functionality.

An out-of-limit condition (i.e., HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT/THERM2 pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e., E1HIGH) will be set to ‘1’, the ALERT/THERM2 pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the ALERT/THERM2 pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT/THERM2 pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the Therm Hysteresis value.

For example, if the CALRT<2:0> bits are set for four consecutive alerts on an MCP9902 device, the high limits are set at +70°C, and none of the channels are masked, then the ALERT/THERM2 pin will be asserted after the following five measurements:

- The Internal Diode reads +71°C and the external diode reads +69°C. Consecutive alert counter for INT is incremented to 1.
- Both the Internal Diode and the External Diode 1 read +71°C. The consecutive alert counter for INT is incremented to 2, and the counter for EXT1 is set to 1.
- The External Diode 1 reads +71°C and the Internal Diode reads +69°C. The consecutive alert counter for INT is cleared, and EXT1 is incremented to 2.
- The Internal Diode reads +71°C and the external diode reads +71°C. The consecutive alert counter for INT is set to 1 and EXT1 is incremented to 3.
- The Internal Diode reads +71°C and the external diode reads +71°C. The consecutive alert counter for INT is incremented to 2 and EXT1 is incremented to 4. The appropriate status bits are set for EXT1 and the ALERT/THERM2 pin is asserted. The EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

All temperature channels use this value to set the respective counters. The consecutive Therm counter is incremented whenever any measurement exceed the corresponding Therm Limit.

If the temperature drops below the Therm Limit, the counter is reset. If a number of consecutive measurements above the Therm Limit occurs, the THERM pin is asserted low.

Once the THERM pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the Therm Limit minus the Therm Hysteresis value.

The bits are decoded as shown in Table 3-5.The default setting is one consecutive out-of-limit conversion, and is set in Register 4-21.

TABLE 3-5: CONSECUTIVE ALERT/ THERM SETTINGS

2	1	0	Number of consecutive out of limit measurements
0	0	0	1 (default for CALRT<2:0>)
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM<2:0>)

3.13 Limit Register Interaction

The various limit registers in the device interact based on both external conditions present on the diode pins as well as changes in register bits in the SMBus interface.The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT/THERM2 pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT/THERM2 pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in Standby mode, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One Shot Register (see Register 4-15) or by clearing the RUN/STOP bit (see Register 4-6).

The THERM Limit Status Register contains the status bits that are set when a temperature channel Therm Limit is exceeded. If any of these bits are set, the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

3.13.1 HIGH LIMIT REGISTER

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits. Reading from the register will also clear the HIGH status bit in the Status Register.

The ALERT/THERM2 pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the ALERT/THERM2 pin is configured as a comparator output (see **Section 3.6.2 "ALERT/THERM2 Pin In THERM Mode"**).

3.13.2 LOW LIMIT REGISTER

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits.

The ALERT/THERM2 pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the ALERT/THERM2 pin is configured as a comparator output (see **Section 3.6.2 "ALERT/THERM2 Pin In THERM Mode"**).

3.13.3 THERM LIMIT REGISTER

The Therm Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the Therm Limit, the THERM pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the ALERT/THERM2 pin, the THERM pin cannot be masked. Additionally, the THERM pin will be released once the temperature drops below the corresponding threshold minus the Therm Hysteresis.

3.13.4 CHANNEL MASKING

The Channel Mask Register (Register 4-20) controls individual channel masking. When a channel is masked, the ALERT/THERM2 pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the THERM pin.

3.14 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled (default). The typical filter performance is shown in Figure 3-2 and Figure 3-3. The Filter Configuration Register controls the digital filter on the External Diode 1 channel.

TABLE 3-6: FILTER SETTINGS

FILTER<1:0>		Averaging
1	0	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

Note 1: Filtering Level 1 corresponds to 4x attenuation of a temperature spike.

2: Filtering Level 2 corresponds to 8x attenuation of a temperature spike.

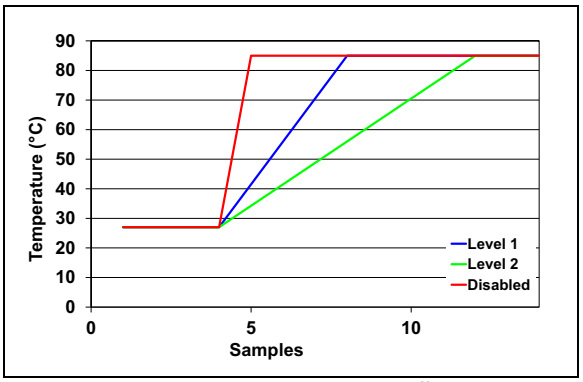


FIGURE 3-2: *Temperature Filter Step Response.*

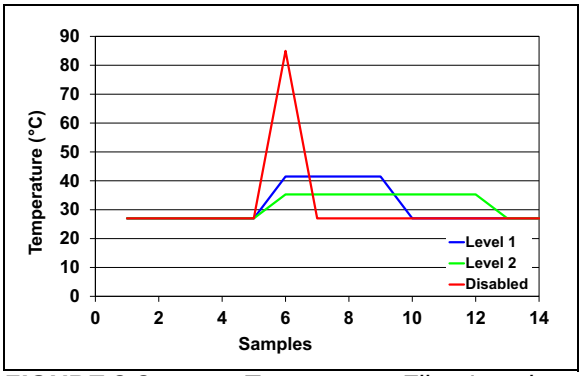


FIGURE 3-3: *Temperature Filter Impulse Response.*

EQUATION 3-1: FILTER EQUATION

$$AVG = \frac{TEMP_{N-1} + TEMP_{N-2} + \ldots + TEMP_0}{N}$$

Where: N = either 4 or 8 as determined by choosing Level1 (4) or Level 2 (8) filter

3.15 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The MCP9902 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by +64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 3-7 shows the default and extended range formats.

TABLE 3-7: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range 0°C to +127°C	Extended Range -64°C to +191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (Note 2)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (Note 1)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (Note 3)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (Note 4)

Note 1: In default mode, all temperatures < 0°C will be reported as 0°C

2: In the extended range, all temperatures less than -64°C will be reported as -64°C.

3: For the default range, all temperatures greater than +127.875°C will be reported as +127.875°C.

4: For the extended range, all temperatures greater than +191.875°C will be reported as +191.875°C.

4.0 COMMUNICATIONS PROTOCOL

The MCP9902 communicates with a host controller, such as an PIC MCU, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3-1.

For the first 15ms after power-up the device may not respond to SMBus communications.

4.1 SMBus Control Bits

The interaction between clock and data creates special function bits within the data stream.

4.1.1 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

4.1.2 SMBUS ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{WR}$ indicator bit. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus Host is reading data from the client device.

4.1.3 SMBUS DATA BYTES

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

4.1.4 SMBUS ACK AND NACK BITS

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to the Write Byte protocol.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

4.1.5 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

4.2 SMBus Timeout

The MCP9902 supports SMBus Timeout. If the clock line is held low for longer than $t_{TIMEOUT}$, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit (see Register 4-21).

4.3 SMBus and I^{2}C Compatibility

The MCP9902 is compatible with SMBus and I^{2}C. The major differences between SMBus and I^{2}C devices are highlighted here. For more information, refer to the SMBus 2.0 and I^{2}C specifications. For information on using the MCP990X in an I^{2}C system, refer to AN14.0 "Microchip Dedicated Slave Devices in I^{2}C Systems", DS00001853.

- MCP9902 supports I^{2}C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
- Minimum frequency for SMBus communications is 10kHz.
- The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the MCP990X and can be enabled by writing to the TIMEOUT bit. I^{2}C does not have a timeout.
- I^{2}C devices do not support the Alert Response Address functionality (which is optional for SMBus).

Attempting to communicate with the MCP9902 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

4.4 SMBus Protocols

The device supports Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4-1.

TABLE 4-1: PROTOCOL FORMAT

Data Sent To Device	Data Sent To The Host
# of bits sent	# of bits sent

4.4.1 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in Table 4-2.

TABLE 4-2: WRITE BYTE PROTOCOL

START	SLAVE ADDR	WR	ACK	REG ADDR	ACK	REG DATA	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

4.4.2 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4-3.

TABLE 4-3: READ BYTE PROTOCOL

START	SLAVE ADDR	WR	ACK	REG ADDR	ACK	START	SLAVE ADDR	RD	ACK	REG DATA	NACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

4.4.3 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4-4.

TABLE 4-4: SEND BYTE PROTOCOL

START	SLAVE ADDR	WR	ACK	REG ADDR	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

4.4.4 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4-5.

TABLE 4-5: RECEIVE BYTE PROTOCOL

START	SLAVE ADDR	RD	ACK	REG DATA	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

4.5 Alert Response Address

The $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 4-6.

TABLE 4-6: ALERT RESPONSE ADDRESS PROTOCOL

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 → 0	0001_100	1	0	YYYY_YYY	1	0 → 1

The MCP9902 will respond to the ARA in the following way:

- Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK_ALL bit to clear the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin.

The ARA does not clear the Status Register and if the MASK_ALL bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin will be reasserted.

4.6 Register Description

TABLE 4-7: REGISTER SET IN HEXADECIMAL ORDER

Register Name	Reg Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Por Value
INT TEMP HIGH BYTE	00h	IHB7	IHB6	IHB5	IHB4	IHB3	IHB2	IHB1	IHB0	00h
EXT1 TEMP HIGH BYTE	01h	E1HB7	E1HB6	E1HB5	E1HB4	ETHB3	E1HB2	E1HB1	E1HB0	00h
STATUS	02h	BUSY	IHIGH	ILOW	EHIGH	ELOW	FAULT	ETHRM	ITHRM	00h
CONFIG	03h	MSKAL	R/S	AT/THM	RECD1	—	RANGE	DA_DIS	—	00h
CONVERT	04h	SLEEP	—	—	—	CONV3	CONV2	CONV1	CONV0	06h (4/sec)
INT DIODE HI LIMIT TEMP	05h	IDHL7	IDHL6	IDHL5	IDHL4	IDHL3	IDHL2	IDHL1	IDHL0	55h (85°C)
INT DIODE LO LIMIT TEMP	06h	IDLL7	IDLL6	IDLL5	IDLL4	IDLL3	IDLL2	IDLL1	IDLL0	00h (0°C)
EXT1 HI LIMIT TEMP HI BYTE	07h	E1HLH7	E1HLH6	E1HLH5	E1HLH4	E1HLH3	E1HLH2	E1HLH1	E1HLH0	55h (85°C)
EXT1 LO LIMIT TEMP HI BYTE	08h	E1LLH7	E1LLH6	E1LLH5	E1LLH4	E1LLH3	E1LLH2	E1LLH1	E1LLH0	00h (0°C)
CONFIG	09h	MSKAL	R/S	AT/THM	RECD1	—	RANGE	DA_DIS	—	00h
CONVERT	0Ah	STOP	—	—	—	CONV3	CONV2	CONV1	CONV0	06h (4/sec)
INT DIODE HI LIMIT TEMP	0Bh	IDHL7	IDHL6	IDHL5	IDHL4	IDHL3	IDHL2	IDHL1	IDHL0	55h (85°C)
INT DIODE LO LIMIT TEMP	0Ch	IDLL7	IDLL6	IDLL5	IDLL4	IDLL3	IDLL2	IDLL1	IDLL0	00h (0°C)
EXT1 HI LIMIT TEMP HI BYTE	0Dh	E1HLH7	E1HLH6	E1HLH5	E1HLH4	E1HLH3	E1HLH2	E1HLH1	E1HLH0	55h (85°C)
EXT1 LO LIMIT TEMP HI BYTE	0Eh	E1LLH7	E1LLH6	E1LLH5	E1LLH4	E1LLH3	E1LLH2	E1LLH1	E1LLH0	00h (0°C)
ONE SHOT	0Fh	ONSH7	ONSH6	ONSH5	ONSH4	ONSH3	ONSH2	ONSH1	ONSH0	00h
EXT1 TEMP LO BYTE	10h	E1LB2	E1LB1	E1LB0	—	—	—	—	—	00h
SCRTCHPD1	11h	SPD17	SPD16	SPD15	SPD14	SPD13	SPD12	SPD11	SPD10	00h
SCRTCHPD2	12h	SPD27	SPD26	SPD25	SPD24	SPD23	SPD22	SPD21	SPD20	00h
EXT1 HI LIM TEMP LO BYTE	13h	E1HLL2	E1HLL1	E1HLL0	—	—	—	—	—	00h
EXT1 LO LIMIT TEMP LO BYTE	14h	E1LLL2	E1LLL1	E1LLL0	—	—	—	—	—	00h
EXT1 THERM LIMIT	19h	E1THL7	E1THL6	E1THL5	E1THL4	E1THL3	E1THL2	E1THL1	E1THL0	55h (85°C)
DIODE FAULT MASK	1Fh	—	—	—	—	—	—	E1MSK	INTMSK	00h
INT DIODE THERM LIMIT	20h	IDTHL7	IDTHL6	IDTHL5	IDTHL4	IDTHL3	IDTHL2	IDTHL1	IDTHL0	55h (85°C)
THRM HYS	21h	THMH7	THMH6	THMH5	THMH4	THMH3	THMH2	THMH1	THMH0	0Ah (10°C)
CONSEC ALRT	22h	TMOUT	CTHM2	CTHM1	CTHM0	CALRT2	CALRT1	CALRT0	—	70h
EXT1 BETA CONFIG	25h	—	—	—	—	ENBL1	BETA12	BETA11	BETA10	08h
EXT1 IDEALITY FACTOR	27h	—	—	IDEL15	IDEL14	IDEL13	IDEL12	IDEL11	IDEL10	12h (1.008)

TABLE 4-7: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Por Value
INT TEMP LO BYTE	29h	ITLB2	ITLB1	ITLB0	—	—	—	—	—	00h
FLTR SEL	40h	—	—	—	—	—	—	FLTER1	FLTER0	00h
PRODUCT ID (DECODER)	FDh	0	0	1	0	0	EXT2_APD_EN	0	EXT2_EN	20h
MANUFACTURER ID	FEh									5Dh
REVISION	FFh									00h

4.7 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

REGISTER 4-1: INT TEMP HI BYTE: INTERNAL DIODE HIGH BYTE TEMPERATURE DATA REGISTER (ADDRESS 00H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
IHB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **IHB<7:0>**: 2’s complement integer value of the internal diode temperature reading

REGISTER 4-2: INT TEMP LO BYTE: INTERNAL DIODE LOW BYTE TEMPERATURE DATA REGISTER (ADDRESS 29H)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
ILB<2:0>			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-5 **ILB<2:0>**: Fractional portion of the Internal Diode Temperature to be added to the value at register 00h
111 = 0.875°C
110 = 0.750°C
101 = 0.625°C
100 = 0.500°C
011 = 0.375°C
010 = 0.250°C
001 = 0.125°C
000 = 0.000°C

4-0 **Unimplemented**: Read as ‘0’

REGISTER 4-3: EXT(1) TEMP HI BYTE: EXTERNAL DIODE HIGH BYTE TEMPERATURE DATA REGISTER (ADDRESS 01H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
EXT(1)_HB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **EXT(1)_HB<7:0>**: 2's complement integer value of the External Diode n temperature reading, where n = 1 to 3, depending on the device

REGISTER 4-4: EXT(1) TEMP LO BYTE: EXTERNAL DIODE LOW BYTE TEMPERATURE DATA REGISTER (ADDRESS 10H)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
EXT(1)_LB<2:0>			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-5 **EXT(1)_LB<2:0>**: Fractional portion of the Internal Diode Temperature to be added to the value at register 00h
111 = 0.875°C
110 = 0.750°C
101 = 0.625°C
100 = 0.500°C
011 = 0.375°C
010 = 0.250°C
001 = 0.125°C
000 = 0.000°C

4-0 **Unimplemented**: Read as '0'

REGISTER 4-5: STATUS: STATUS REGISTER REPORTING STATE OF INTERNAL AND EXTERNAL DIODES (ADDRESS 02H)

RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0
BUSY	IHIGH	ILOW	EHIGH	ELOW	FAULT	ETHRM	ITHRM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7 **BUSY**: This bit indicates that the ADC is currently converting. This bit does not cause either the ALERT/THERM2 or THERM pin to be asserted.
1 = ADC is currently converting
0 = ADC is not converting

6 **IHIGH**: This bit indicates the Internal Diode channel exceeds its programmed high limit. When set, this bit will assert the ALERT/THERM2 pin.
1 = Reported temperature above the high limit
0 = Reported temperature is not above the high limit

5 **ILOW**: This bit indicates the Internal Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT/THERM2 pin.
1 = Reported temperature below the low limit
0 = Reported temperature is not below the low limit

4 **EHIGH**: This bit indicates the External Diode channel exceeds its programmed high limit. When set, this bit will assert the ALERT/THERM2 pin.
1 = Reported temperature above the high limit
0 = Reported temperature is not above the high limit

3 **ELOW**: This bit indicates the External Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT/THERM2 pin.
1 = Reported temperature below the low limit
0 = Reported temperature is not below the low limit

2 **FAULT**: This bit indicates when a diode fault is detected. When set, this bit will assert the ALERT/THERM2 pin.
1 = Open circuit or short of a diode
0 = No fault reported

1 **ETHRM**: This bit indicates the External Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released at which point it will be automatically cleared.
1 = Reported temperature above the high limit
0 = Reported temperature is not above the high limit

0 **ITHRM**: This bit is set when the Internal Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released at which point it will be automatically cleared.
1 = Reported temperature above the high limit
0 = Reported temperature is not above the high limit

REGISTER 4-6: CONFIG: CONFIGURATION REGISTER (ADDRESSES 03H AND 09H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
MSKAL	R/S	AT/THM	RECD1	—	RANGE	DA_DIS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7 **MSKAL**: Masks the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin from asserting when the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is in interrupt mode. This bit has no effect when the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is in comparator mode.
1 = The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is masked and will not be asserted for any interrupt condition when the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is in interrupt mode. The Status Register will be updated normally.
0 = The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin will be asserted.

6 **R/S**: Controls Active/Standby states.
1 = The device is in Standby state and not converting (unless a one-shot has been commanded).
0 = The device is in Active state and converting on all channels.

5 **AT/THM**: Controls the operation of the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin.
1 = The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin acts in comparator mode as described in **Section 3.6.2 “ALERT/THERM2 Pin In THERM Mode”**. In this mode the MASK_ALL bit is ignored.
0 = The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin acts in interrupt mode as described in **Section 3.6.1 “ALERT/THERM2 Pin Interrupt Mode”**.

4 **RECD1**: Disables the Resistance Error Correction (REC) for the External Diode 1.
1 = REC is disabled for the External Diode 1.
0 = REC is enabled for the External Diode 1.

3 Hardwired as ‘0’

2 **RANGE**: Configures the measurement range and data format of the temperature channels.
1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 3-7).
0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary.

1 **DA_DIS**: Disables the dynamic averaging feature on all temperature channels.
1 = The dynamic averaging feature is disabled.
0 = The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 3-1.

0 Hardwired as ‘0’

REGISTER 4-7: CONVERT: TEMPERATURE CONVERSION RATE REGISTER (ADDRESS 04H, 0AH)

RW-0	U-0	U-0	U-0	RW-0	RW-1	RW-1	RW-0
SLEEP	—	—	—	CONV<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7 **SLEEP**
0 = Active Mode or Standby mode, as controlled by R/S bit in Register 02h
1 = SLEEP mode is enabled. This bit overrides R/S in Register 02h

6-4 **Unimplemented**: Read as ‘0’

3-0 **CONV<3:0>**: The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address (04H, 0AH). Determines the conversion rate as shown in Table 3-1.

REGISTER 4-8: INT DIODE HI LIMIT TEMP: INTERNAL DIODE HIGH LIMIT TEMPERATURE REGISTER (ADDRESSES 05H AND 0BH)

RW-0	RW-1	RW-0	RW-1	RW-0	RW-1	RW-0	RW-1
IDHL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **IDHL<7:0>**: 2’s complement integer value of the Internal Diode n temperature reading,

REGISTER 4-9: INT DIODE LO LIM TEMP – INTERNAL DIODE LOW LIMIT TEMPERATURE REGISTER (ADDRESSES 06H AND 0CH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
IDLL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **IDLL<7:0>**: Integer value of the Internal Diode temperature reading,

REGISTER 4-10: EXT(1) HI LIM TEMP HB – EXTERNAL DIODE N HIGH TEMPERATURE LIMIT, HIGH BYTE REGISTER (ADDRESS 07H AND 0DH)

RW-0	RW-1	RW-0	RW-1	RW-0	RW-1	RW-0	RW-1
EXT(1)_HLH<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **EXT(1)_HLH<7:0>**: Integer value of the External Diode n temperature reading, where N = 1 to 3 depending on device

REGISTER 4-11: EXT(1) HI LIM LB – EXTERNAL DIODE N HIGH LIMIT TEMPERATURE, LOW BYTE REGISTER (ADDRESS 13H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
EXT(1)_HLL<2:0>			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-5 **EXT(1)_HLL<2:0>**: Fractional portion of the High Limit Temperature to be added to the value at the respective high byte registers
111 = 0.875°C
110 = 0.750°C
101 = 0.625°C
100 = 0.500°C
011 = 0.375°C
010 = 0.250°C
001 = 0.125°C
000 = 0.000°C

4-0 **Unimplemented**: Read as ‘0’

REGISTER 4-12: EXT(1) LO LIM HB – EXTERNAL DIODE N LOW LIMIT, HIGH BYTE TEMPERATURE REGISTER (ADDRESS 08H AND 0EH)

RW-0	RW-1	RW-0	RW-1	RW-0	RW-1	RW-0	RW-1
EXT(1)_LLHB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **EXT(1)_LLHB<7:0>**: Integer portion of External Diode n Low temperature Limit, where n = 1 to 3 depending on device

REGISTER 4-13: EXT(1) LO LIM LB – EXTERNAL DIODE N LOW LIMIT, LOW BYTE TEMPERATURE REGISTER (ADDRESS 14H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
EXT(1)_LLLB<2:0>			--	--	--	--	--
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-5 **EXT(1)_LLLB<2:0>**: Fractional portion of the Low Limit Temperature to be added to the value at the respective high byte registers, where n = 1 to 3.
111 = 0.875°C
110 = 0.750°C
101 = 0.625°C
100 = 0.500°C
011 = 0.375°C
010 = 0.250°C
001 = 0.125°C
000 = 0.000°C

4-0 **Unimplemented**: Read as '0'

REGISTER 4-14: SCRTCHPD(N): SCRATCHPAD REGISTER (ADDRESSES 11H AND 12H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
SPD(N)<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **SPD(N)<7:0>**: User temporary storage registers, where n = 1 to 2

REGISTER 4-15: ONE SHOT – ONE-SHOT TEMPERATURE CONVERSION INITIATION REGISTER (ADDRESS 0FH)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
ONSH<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **ONSH<7:0>**: When the device is in the Standby state, writing to the One-shot Register will initiate a conversion cycle and update the temperature measurements. Writing to the One Shot Register while the device is in the Active state or when the BUSY bit is set in the Status Register 02h will have no effect.

REGISTER 4-16: EXT(1) THRM LIM – EXTERNAL DIODE (N) $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 19H)

RW-0	RW-1	RW-0	RW-1	RW-0	RW-1	RW-0	RW-1
EXT(1)_THL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **EXT(1)_THL<7:0>**: External Diode (n) THERM Limits, where n=1 to 3

REGISTER 4-17: INTD THRM LIM – INTERNAL DIODE $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 20H)

RW-0	RW-1	RW-0	RW-1	RW-0	RW-1	RW-0	RW-1
IDTHL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **IDTHL<7:0>**: Internal Diode THERM Limits.

REGISTER 4-18: THRM HYS – $\overline{\text{THERM}}$ LIMIT HYSTERESIS REGISTER (ADDRESS 21H)

RW-0	RW-0	RW-0	RW-0	RW-1	RW-0	RW-1	RW-0
THRMH<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-0 **THRMH<7:0>**: ITHERM Limit hysteresis.

REGISTER 4-19: EXT FLT STS – EXTERNAL DIODE FAULT STATUS REGISTER (ADDRESS 1BH)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	U-0
—	—	—	—	E3FLT	E2FLT	E1FLT	—
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-4 **Unimplemented**: Read as ‘0’

3 **E3FLT**: This bit is set if the External Diode 3 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

2 **E2FLT**: This bit is set if the External Diode 2 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

1 **E1FLT**: This bit is set if the External Diode 2 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

0 **Unimplemented**: Read as ‘0’

REGISTER 4-20: DIODE FAULT MASK – DIODE FAULT MASK REGISTER (ADDRESS 1FH)

U-0	U-0	U-0	U-0	U-0	U-0	RW-0	RW-0
—	—	—	—	—	—	E1MSK	INTMSK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-2 **Unimplemented**: Read as ‘0’

1 **E1MASK**: Masks the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin from asserting when the External Diode 1 channel is out of limit or reports a diode fault.
1 = The External Diode 1 channel will not cause the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode 1 channel will cause the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin to be asserted if it is out of limit or reports a diode fault.

0 **INTMASK**: Masks the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin from asserting when the Internal Diode temperature is out of limit.
1 = The Internal Diode channel will not cause the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin to be asserted if it is out of limit.
0 = The Internal Diode channel will cause the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin to be asserted if it is out of limit.

REGISTER 4-21: CONSEC ALERT – CONSECUTIVE ALERT REGISTER (ADDRESS 22H)

RW-0	RW-1	RW-1	RW-1	RW-0	RW-0	RW-0	U-0
TMOUT	CTHM<2:0>			CALRT<2:0>			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7 **TMOUT**: Enables the time-out and idle functionality of the I^2C protocol.
1 = The I^2C time-out and idle functionality are enabled. The I^2C interface will time-out if the clock line is held low for longer than 30 ms. Likewise, it will reset if both the data and clock lines are held high for longer than 200 µs.
0 = The I^2C time-out and idle functionality are disabled. The I^2C interface will not time-out if the clock line is held low for longer than 30ms. Likewise, it will not reset if both the data and clock lines are held high for longer than 200 µs. This is used for I^2C compliance.

6-4 **CTHM<2:0>**: Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the $\overline{\text{THERM}}$ pin is asserted.
000 = 1
001 = 2
011 = 3
111 = 4

3-1 **CALRT<2:0>**: Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is asserted.
000 = 1
001 = 2
011 = 3
111 = 4

0 **Unimplemented**: Read as '0'

REGISTER 4-22: EXT(1) BETA CFG – BETA COMPENSATION CONFIGURATION REGISTER (ADDRESSES 25H)

U-0	U-0	U-0	U-0	RW-1	RW-0	RW-0	RW-0
—	—	—	—	ENABLE	BETA<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7 **Unimplemented**: Read as '0'

6 **Unimplemented**: Read as '0'

5 **Unimplemented**: Read as '0'

4 **Unimplemented**: Read as '0'

3 **ENABLE**: Enables the Beta Compensation factor auto-detection function.
1 = Auto-Beta detection for External Diode x is enabled
0 = Auto-Beta detection for External Diode x is disabled

2-0 **BETAx<2:0>**: These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect.
000 = 0.11
001 = 0.18
010 = 0.25
011 = 0.33
100 = 0.43
101 = 1.00
110 = 2.33
111 = disabled

REGISTER 4-23: EXT(1) IDEALITY FACTOR – EXTERNAL DIODE N IDEALITY FACTOR REGISTER (ADDRESS 27H)

U-0	U-0	RW-0	RW-1	RW-0	RW-0	RW-1	RW-0
—	—	IDEAL(n)<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7 **Unimplemented**: Read as '0'

6 **Unimplemented**: Read as '0'

5-0 **IDEAL(n)<5:0>**: External Diode n Ideality factor, where n = 1 to 3 depending on device

REGISTER 4-24: HI LIM STS – HIGH LIMIT STATUS REGISTER (ADDRESS 35H)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
—	—	—	—	E3HIGH	E2HIGH	E1HIGH	IHIGH
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-4 **Unimplemented**: Read as '0'

3 **E3HIGH**: This bit is set when the External Diode 3 exceeds its programmed HIGH limit. Reading this register will also clear the HIGH bit
1 = high limit exceeded
0 = High limit not exceeded

2 **E2HIGH**: This bit is set when the External Diode 2 exceeds its programmed HIGH limit. Reading this register will also clear the HIGH bit
1 = high limit exceeded
0 = High limit not exceeded

1 **E1HIGH**: This bit is set when the External Diode 1 exceeds its programmed HIGH limit. Reading this register will also clear the HIGH bit
1 = high limit exceeded
0 = High limit not exceeded

0 **IHIGH**: This bit is set when the Internal Diode exceeds its programmed high limit. Reading this register will also clear the HIGH bit.
1 = high limit exceeded
0 = High limit not exceeded

REGISTER 4-25: LO LIM STS – LOW LIMIT STATUS REGISTER (ADDRESS 36H)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
—	—	—	—	E3LOW	E2LOW	E1LOW	ILOW
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-4 **Unimplemented**: Read as ‘0’

3 **E3LOW**: This bit is set when the External Diode 3 channel drops below its programmed low limit. Reading from the register will also clear the LOW status bit in the Status Register.
1 = Low limit exceeded
0 = Low limit not exceeded

2 **E2LOW**: This bit is set when the External Diode 2 drops below its programmed low limit. Reading this register will also clear the LOW bit
1 = Low limit exceeded
0 = Low limit not exceeded

1 **E1LOW**: This bit is set when the External Diode 1 drops below its programmed low limit. Reading this register will also clear the LOW bit
1 = Low limit exceeded
0 = Low limit not exceeded

0 **ILOW**: This bit is set when the Internal Diode drops below its programmed low limit. Reading this register will also clear the LOW bit
1 = Low limit exceeded
0 = Low limit not exceeded

REGISTER 4-26: THRM LIM STS – HIGH LIMIT STATUS REGISTER (ADDRESS 37H)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
—	—	—	—	E3THERM	E2THERM	E1THERM	ITHERM
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-4 **Unimplemented**: Read as '0'

3 **E3THERM**: This bit is set when the External Diode 3 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.
1 = $\overline{\text{THERM}}$ pin asserted
0 = $\overline{\text{THERM}}$ pin not asserted

2 **E2THERM**: This bit is set when the External Diode 2 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.
1 = $\overline{\text{THERM}}$ pin asserted
0 = $\overline{\text{THERM}}$ pin not asserted

1 **E1THERM**: This bit is set when the External Diode 1 channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.
1 = $\overline{\text{THERM}}$ pin asserted
0 = $\overline{\text{THERM}}$ pin not asserted

0 **ITHERM**: This bit is set when the Internal Diode channel exceeds its programmed Therm Limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.
1 = $\overline{\text{THERM}}$ pin asserted
0 = $\overline{\text{THERM}}$ pin not asserted

REGISTER 4-27: FLTR SEL: FILTER SELECTION REGISTER (ADDRESS 40H)

U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0
—	—	—	—	—	—	FLTER<1:0>	
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit in unknown

7-2 **Unimplemented**: Read as '0'

1-0 **FILTER**: Control the level of digital filtering that is applied to the External Diode temperature measurement as shown in Table 3-6.

REGISTER 4-28: PROD_ID – PRODUCT ID REGISTER (ADDRESS FDH)

R-0	R-0	R-1	R-0	R-0	R-0	R-0	R-0
—	ADDR_SEL_CH	—	—	—	—	—	—
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-6 Hardwired as '0'

5 Hardwired as ‘1’

4-0 Hardwired as '0'

REGISTER 4-29: MCHP_ID – MANUFACTURER ID REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MCHP_ID<7:0>							
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **MCHP_ID<7:0>**: Unique manufacturer ID for Microchip

REGISTER 4-30: REVISION – REVISION REGISTER (ADDRESS FFH)

R-0	R-0	R-0	R-1	R-0	R-0	R-0	R-0
REVISION<7:0>							
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

7-0 **REVISION<7:0>**: DIE revision number

TABLE 4-8: TEMP DECODE

TEMP[1:0]		
1	**0**	**TEMPERATURE CHANNEL**
0	0	Internal Diode
0	1	External Diode 1
1	0	External Diode 2
1	1	External Diode 3 (APD only)

5.0 PACKAGING INFORMATION

TABLE 5-1: SMBUS ADDRESS DECODE - LOWER BITS

ADDR_SEL_EN	ADDR	SMBUS SLAVE ADDRESS LOWER 4 BITS
0	0	1001_100xb
0	1	1001_101xb
1	0	1_100xb
1	1	1_101xb

TABLE 5-2: I^2C ADDRESS DECODE - LOWER BITS

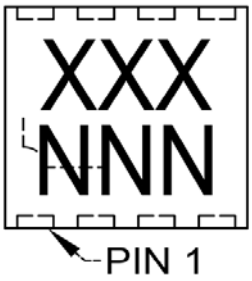
ADDR_SEL_EN	ADDR	I^2C SLAVE ADDRESS LOWER 4 BITS
0	0	1001_100xb
0	1	1001_101xb
1	0	1_100xb
1	1	1_101xb

TABLE 5-3: I^2C ADDRESS DECODE - UPPER BITS

RESISTOR	FUNC_SEL[2:0]			I^2C SLAVE ADDRESS UPPER 3 BITS
	2	1	0	
4.7k	0	0	0	111b
6.8k	0	0	1	101b
10k	0	1	0	100b
15k	0	1	1	110b
22k	1	0	0	001b
33k	1	0	1	011b

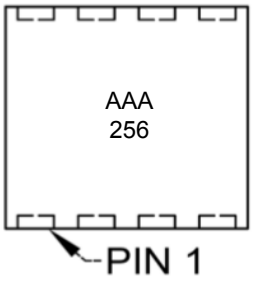
5.1 Package Marking Information

8-Lead WDFN (2 x 2 x 0.9)



Product Number	Code
MCP9902-E/RW	AAA
MCP9902T-E/RW	AAA
MCP9902T-1E/RW	AAC
MCP9902T-2E/RW	AAD
MCP9902T-AE/RW	AAB

Example

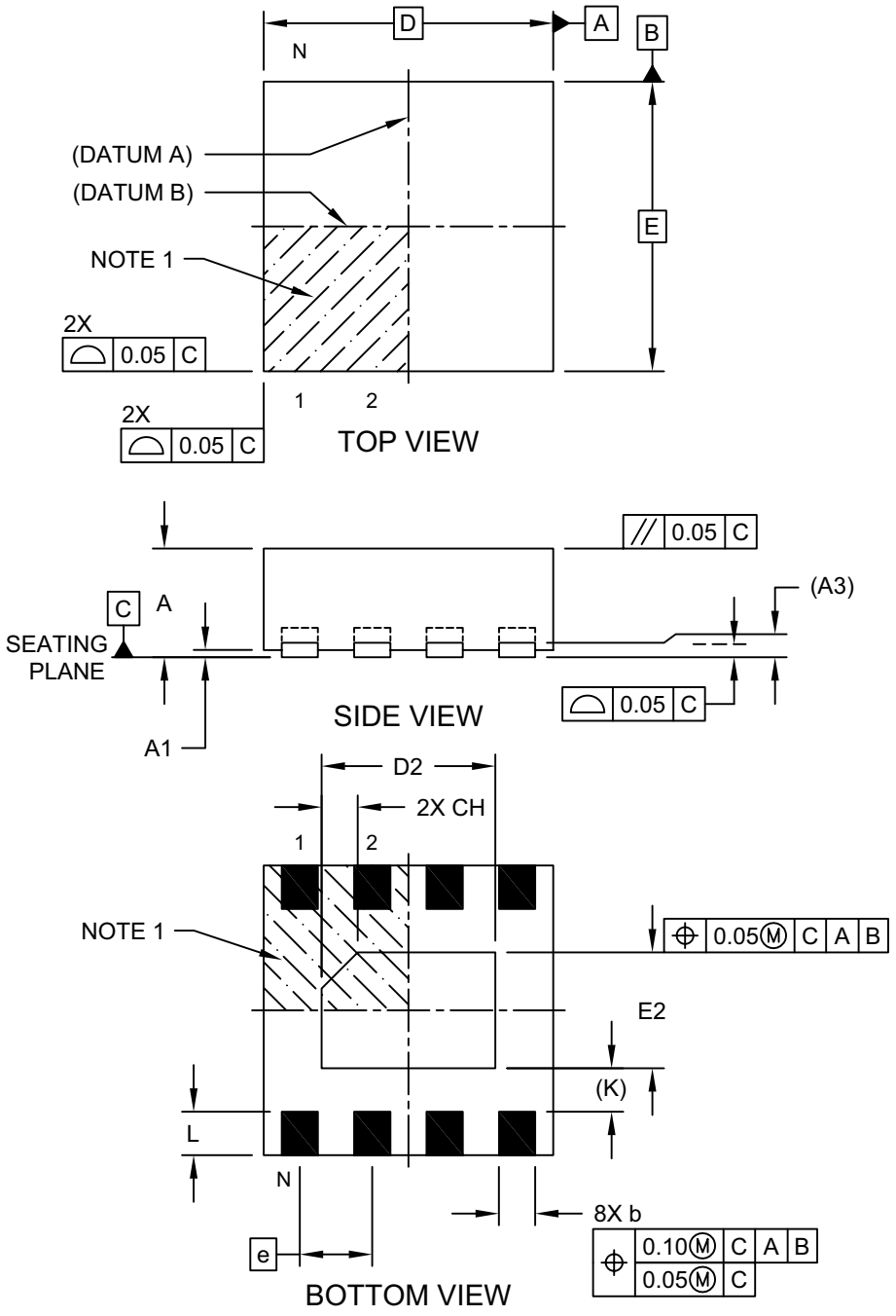


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

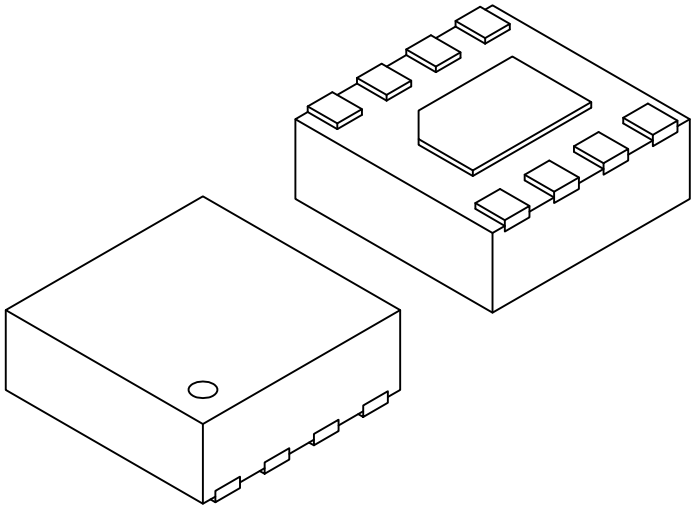
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-261A Sheet 1 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.10 REF	
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.70	0.80	0.90
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Exposed Pad Chamfer	CH	-	0.25	-
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	(K)	0.30	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

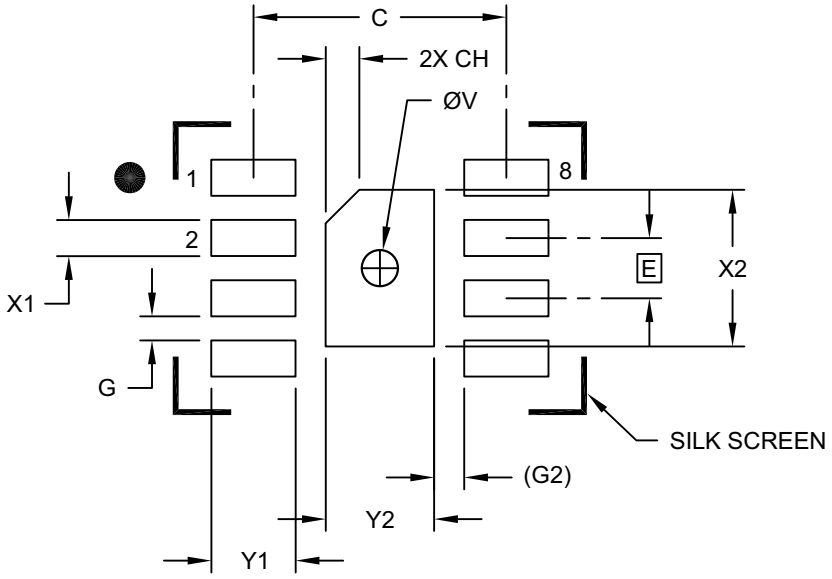
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-261A Sheet 2 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			0.90
Optional Center Pad Length	X2			1.30
Contact Pad Spacing	C		2.10	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.70
Contact Pad to Contact Pad (X6)	G1	0.20		
Contact Pad to Center Pad (X8)	G1		0.25 REF	
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerances, for reference only.

Microchip Technology Drawing C04-2261A

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	X	/XX
Device	SMBUS Address	Temperature Range	Package

Device:	MCP9902:	High-Accuracy, Low-Cost, SMBus Temperature Sensor
	MCP9902T:	High-Accuracy, Low-Cost, SMBus Temperature Sensor (Tape and Reel)
XXX:	1 =	1001_100(r/$\overline{w}$)
	2 =	1000_101(r/$\overline{w}$)
	A =	Adjustable
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	RW =	8-Lead Plastic Dual Flat, No Lead – 2x2x0.9 mm body (WDFN)

Examples:

a) MCP9902-E/RW: Extended temperature, 8L-WDFN package

b) MCP9902T-E/RW:Tape and reel, extended temperature, 8L-WDFN package

c) MCP9902T-1E/RW:Tape and reel extended temperature, 8L-WDFN package

d) MCP9902T-2E/RW:Tape and reel extended temperature, 8L-WDFN package

e) MCP9902T-3E/RW:Tape and reel extended temperature, 8L-WDFN package

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