



FEATURES

- 1.8 V supply operation
- Low power: 110 mW per channel at 125 MSPS with scalable power options
- SNR = 74 dB (to Nyquist)
- SFDR = 90 dBc (to Nyquist)
- DNL = ± 0.75 LSB (typical); INL = ± 2.0 LSB (typical)
- Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- Serial port control
 - Full chip and individual channel power-down modes
 - Flexible bit orientation
 - Built-in and custom digital test pattern generation
 - Multichip sync and clock divider
 - Programmable output clock and data alignment
 - Programmable output resolution
 - Standby mode

APPLICATIONS

- Medical ultrasound
- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Test equipment

GENERAL DESCRIPTION

The AD9253 is a quad, 14-bit, 80 MSPS/105 MSPS/125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual-channel power-down is supported and typically consumes less than 2 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

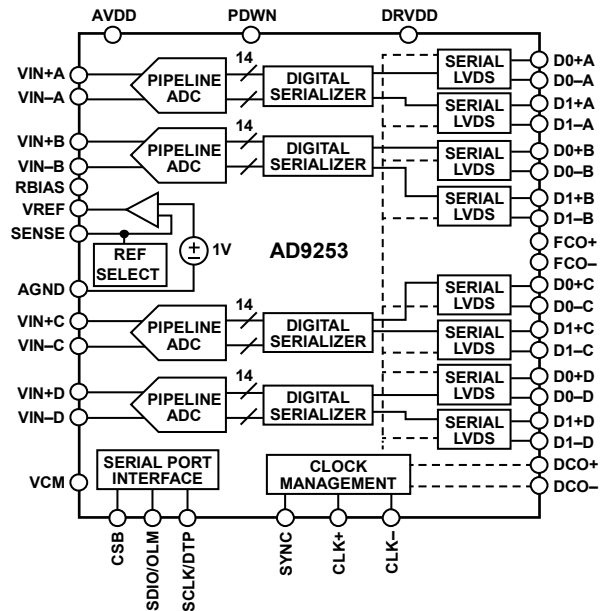


Figure 1.

10065-001

as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9253 is available in a RoHS-compliant, 48-lead LFCSP. It is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Small Footprint. Four ADCs are contained in a small, space-saving package.
2. Low power of 110 mW/channel at 125 MSPS with scalable power options.
3. Pin compatible to the AD9633 12-bit quad ADC.
4. Ease of Use. A data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
5. User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements.

TABLE OF CONTENTS

| | | | |
|--|----|--|----|
| Features | 1 | Clock Input Considerations..... | 23 |
| Applications..... | 1 | Power Dissipation and Power-Down Mode | 25 |
| General Description | 1 | Digital Outputs and Timing | 26 |
| Functional Block Diagram | 1 | Output Test Modes..... | 29 |
| Product Highlights | 1 | Serial Port Interface (SPI)..... | 30 |
| Revision History | 2 | Configuration Using the SPI..... | 30 |
| Specifications..... | 3 | Hardware Interface..... | 31 |
| DC Specifications | 3 | Configuration Without the SPI | 31 |
| AC Specifications..... | 4 | SPI Accessible Features..... | 31 |
| Digital Specifications | 5 | Memory Map | 32 |
| Switching Specifications | 6 | Reading the Memory Map Register Table..... | 32 |
| Timing Specifications | 6 | Memory Map Register Table..... | 33 |
| Absolute Maximum Ratings..... | 10 | Memory Map Register Descriptions..... | 36 |
| Thermal Resistance | 10 | Applications Information | 38 |
| ESD Caution..... | 10 | Design Guidelines | 38 |
| Pin Configuration and Function Descriptions..... | 11 | Power and Ground Recommendations | 38 |
| Typical Performance Characteristics | 13 | Clock Stability Considerations | 38 |
| AD9253-80 | 13 | Exposed Pad Thermal Heat Slug Recommendations..... | 38 |
| AD9253-105 | 15 | VCM..... | 38 |
| AD9253-125 | 17 | Reference Decoupling..... | 38 |
| Equivalent Circuits | 20 | SPI Port | 38 |
| Theory of Operation | 21 | Crosstalk Performance | 39 |
| Analog Input Considerations..... | 21 | Outline Dimensions | 40 |
| Voltage Reference | 22 | Ordering Guide | 40 |

REVISION HISTORY

10/15—Rev. A to Rev. B

| | |
|--|----|
| Added Note 4, Table 4..... | 6 |
| Changes to Digital Outputs and Timing Section | 27 |
| Changes to Clock Stability Considerations Section..... | 38 |

9/14—Rev. 0 to Rev. A

| | |
|--|----|
| Changes to Table 2..... | 4 |
| Added Propagation Delay Parameters of 1.5 ns (Min) and 3.1 ns (Max); Table 4, Changed t_{SSYNC} from 0.24 ns Typ to 1.2 ns Min, and Changed t_{HSYNC} from 0.40 ns Typ to -0.2 ns Min; Table 5 | 6 |
| Changes to Figure 3..... | 7 |
| Changes to Figure 5..... | 8 |
| Changes to Pin 9 to Pin 14 and Pin 23 to Pin 28 Descriptions | 11 |

| | |
|--|----|
| Changes to Figure 48 and Figure 49 | 20 |
| Changes to Clock Input Options Section..... | 23 |
| Changes to Jitter Considerations Section..... | 25 |
| Changes to Digital Outputs and Timing Section | 26 |
| Changes to Table 11 | 28 |
| Changes to Table 12 | 29 |
| Changes to Channel-Specific Registers Section | 32 |
| Changes to Output Phase (Register 0x16) Section | 36 |
| Changes to Resolution/Sample Rate Override (Register 0x100) Section..... | 37 |
| Added Clock Stability Considerations Section..... | 38 |
| Updated Outline Dimensions..... | 40 |

10/11—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 1.

| Parameter ¹ | Temp | AD9253-80 | | | AD9253-105 | | | AD9253-125 | | | Unit |
|---|------|------------|------|------|------------|-------|------|------------|-------|------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | 14 | | | 14 | | | 14 | | | Bits |
| ACCURACY | | Guaranteed | | | Guaranteed | | | Guaranteed | | | |
| No Missing Codes | Full | Guaranteed | | | Guaranteed | | | Guaranteed | | | |
| Offset Error | Full | -0.7 | -0.3 | +0.1 | -0.7 | -0.3 | +0.1 | -0.7 | -0.3 | +0.1 | % FSR |
| Offset Matching | Full | -0.6 | +0.2 | +0.6 | -0.6 | +0.2 | +0.6 | -0.6 | +0.2 | +0.6 | % FSR |
| Gain Error | Full | -10 | -5 | 0 | -10 | -5 | 0 | -10 | -5 | 0 | % FSR |
| Gain Matching | Full | | 1 | 1.6 | | 1 | 1.6 | | 1.1 | 1.6 | % FSR |
| Differential Nonlinearity (DNL) | Full | -1 | | +1.6 | -0.8 | | +1.5 | -0.8 | | +1.5 | LSB |
| | 25°C | | ±0.8 | | | ±0.75 | | | ±0.75 | | LSB |
| Integral Nonlinearity (INL) | Full | -4.0 | | +4.0 | -4.0 | | 4.0 | -4.0 | | +4.0 | LSB |
| | 25°C | | ±1.5 | | | ±2.0 | | | ±2.0 | | LSB |
| TEMPERATURE DRIFT | | | | | | | | | | | |
| Offset Error | Full | | ±2 | | | ±2 | | | ±2 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | | | | | | | |
| Output Voltage (1 V Mode) | Full | 0.98 | 1.0 | 1.02 | 0.98 | 1.0 | 1.02 | 0.98 | 1.0 | 1.02 | V |
| Load Regulation at 1.0 mA (V _{REF} = 1 V) | Full | | 2 | | | 2 | | | 2 | | mV |
| Input Resistance | Full | | 7.5 | | | 7.5 | | | 7.5 | | kΩ |
| INPUT-REFERRED NOISE | | | | | | | | | | | |
| V _{REF} = 1.0 V | 25°C | | 0.94 | | | 0.94 | | | 0.94 | | LSB rms |
| ANALOG INPUTS | | | | | | | | | | | |
| Differential Input Voltage (V _{REF} = 1 V) | Full | | 2 | | | 2 | | | 2 | | V p-p |
| Common-Mode Voltage | Full | | 0.9 | | | 0.9 | | | 0.9 | | V |
| Differential Input Resistance | | | 5.2 | | | 5.2 | | | 5.2 | | kΩ |
| Differential Input Capacitance | Full | | 3.5 | | | 3.5 | | | 3.5 | | pF |
| POWER SUPPLY | | | | | | | | | | | |
| AVDD | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| DRVDD | Full | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| I _{AVDD} ² | Full | | 131 | 144 | | 158 | 172 | | 183 | 200 | mA |
| I _{DRVDD} (ANSI-644 Mode) ² | Full | | 63 | 81 | | 67 | 95 | | 71 | 100 | mA |
| I _{DRVDD} (Reduced Range Mode) ² | 25°C | | 42 | | | 48 | | | 53 | | mA |
| TOTAL POWER CONSUMPTION | | | | | | | | | | | |
| DC Input | Full | | 326 | | | 375 | | | 423 | | mW |
| Sine Wave Input (Four Channels Including Output Drivers ANSI-644 Mode) | Full | | 349 | 405 | | 405 | 481 | | 457 | 540 | mW |
| Sine Wave Input (Four Channels Including Output Drivers Reduced Range Mode) | 25°C | | 311 | | | 371 | | | 425 | | mW |
| Power-Down | Full | | 2 | | | 2 | | | 2 | | mW |
| Standby ³ | Full | | 178 | | | 209 | | | 236 | | mW |

¹ See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

² Measured with a low input frequency, full-scale sine wave on all four channels.

³ Can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 2.

| Parameter ¹ | Temp | AD9253-80 | | | AD9253-105 | | | AD9253-125 | | | Unit |
|---|------|-----------|------|-----|------------|------|-----|------------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SIGNAL-TO-NOISE RATIO (SNR) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | 75.4 | | | 75.1 | | | 75.3 | | dBFS |
| $f_{IN} = 30.5$ MHz | 25°C | | 74.9 | | | 75.0 | | | 75.2 | | dBFS |
| $f_{IN} = 70$ MHz | Full | 72.2 | 74.7 | | 72.2 | 74.4 | | 73 | 74.2 | | dBFS |
| $f_{IN} = 140$ MHz | 25°C | | 72.3 | | | 73.1 | | | 72.2 | | dBFS |
| $f_{IN} = 200$ MHz | 25°C | | 70.7 | | | 71.2 | | | 70.7 | | dBFS |
| SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | 75.3 | | | 75.0 | | | 75.2 | | dBFS |
| $f_{IN} = 30.5$ MHz | 25°C | | 74.8 | | | 74.9 | | | 75.1 | | dBFS |
| $f_{IN} = 70$ MHz | Full | 71.8 | 74.6 | | 70.8 | 74.2 | | 72.6 | 74.1 | | dBFS |
| $f_{IN} = 140$ MHz | 25°C | | 72.1 | | | 72.8 | | | 71.9 | | dBFS |
| $f_{IN} = 200$ MHz | 25°C | | 70.5 | | | 70.8 | | | 70.4 | | dBFS |
| EFFECTIVE NUMBER OF BITS (ENOB) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | 12.2 | | | 12.1 | | | 12.2 | | Bits |
| $f_{IN} = 30.5$ MHz | 25°C | | 12.1 | | | 12.1 | | | 12.1 | | Bits |
| $f_{IN} = 70$ MHz | Full | 11.6 | 11.9 | | 11.5 | 12.0 | | 11.8 | 12.0 | | Bits |
| $f_{IN} = 140$ MHz | 25°C | | 11.6 | | | 11.8 | | | 11.6 | | Bits |
| $f_{IN} = 200$ MHz | 25°C | | 11.5 | | | 11.5 | | | 11.4 | | Bits |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | 98 | | | 98 | | | 98 | | dBc |
| $f_{IN} = 30.5$ MHz | 25°C | | 93 | | | 92 | | | 92 | | dBc |
| $f_{IN} = 70$ MHz | Full | 77 | 94 | | 75 | 89 | | 77 | 90 | | dBc |
| $f_{IN} = 140$ MHz | 25°C | | 85 | | | 85 | | | 85 | | dBc |
| $f_{IN} = 200$ MHz | 25°C | | 84 | | | 82 | | | 83 | | dBc |
| WORST HARMONIC (SECOND OR THIRD) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | -98 | | | -98 | | | -98 | | dBc |
| $f_{IN} = 30.5$ MHz | 25°C | | -93 | | | -92 | | | -92 | | dBc |
| $f_{IN} = 70$ MHz | Full | | -94 | -77 | | -89 | -75 | | -90 | -77 | dBc |
| $f_{IN} = 140$ MHz | 25°C | | -85 | | | -85 | | | -85 | | dBc |
| $f_{IN} = 200$ MHz | 25°C | | -84 | | | -82 | | | -83 | | dBc |
| WORST OTHER (EXCLUDING SECOND OR THIRD) | | | | | | | | | | | |
| $f_{IN} = 9.7$ MHz | 25°C | | -99 | | | -98 | | | -100 | | dBc |
| $f_{IN} = 30.5$ MHz | 25°C | | -98 | | | -98 | | | -99 | | dBc |
| $f_{IN} = 70$ MHz | Full | | -97 | -77 | | -94 | -77 | | -94 | -84 | dBc |
| $f_{IN} = 140$ MHz | 25°C | | -97 | | | -97 | | | -95 | | dBc |
| $f_{IN} = 200$ MHz | 25°C | | -94 | | | -91 | | | -91 | | dBc |
| TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = -7.0 dBFS | | | | | | | | | | | |
| $f_{IN1} = 70.5$ MHz, $f_{IN2} = 72.5$ MHz | 25°C | | 90 | | | 88 | | | 86 | | dBc |
| CROSSTALK ² | | | | | | | | | | | |
| | Full | | -95 | | | -95 | | | -95 | | dB |
| CROSSTALK (OVERRANGE CONDITION) ³ | | | | | | | | | | | |
| | 25°C | | -89 | | | -89 | | | -89 | | dB |
| POWER SUPPLY REJECTION RATIO (PSRR) ^{1,4} | | | | | | | | | | | |
| AVDD | 25°C | | 48 | | | 48 | | | 48 | | dB |
| DRVDD | 25°C | | 75 | | | 75 | | | 75 | | dB |
| ANALOG INPUT BANDWIDTH, FULL POWER | | | | | | | | | | | |
| | 25°C | | 650 | | | 650 | | | 650 | | MHz |

¹ See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

² Crosstalk is measured at 70 MHz with -1.0 dBFS analog input on one channel and no input on the adjacent channel.

³ Overrange condition is specified as being 3 dB above the full-scale input range.

⁴ PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage, expressed in decibels.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 3.

| Parameter ¹ | Temp | Min | Typ | Max | Unit |
|--|------|------------|------------------|------------|-------|
| CLOCK INPUTS (CLK+, CLK-) | | | | | |
| Logic Compliance | | | CMOS/LVDS/LVPECL | | |
| Differential Input Voltage ² | Full | 0.2 | | 3.6 | V p-p |
| Input Voltage Range | Full | AGND - 0.2 | | AVDD + 0.2 | V |
| Input Common-Mode Voltage | Full | | 0.9 | | V |
| Input Resistance (Differential) | 25°C | | 15 | | kΩ |
| Input Capacitance | 25°C | | 4 | | pF |
| LOGIC INPUTS (PDWN, SYNC, SCLK) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 30 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC INPUT (CSB) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 26 | | kΩ |
| Input Capacitance | 25°C | | 2 | | pF |
| LOGIC INPUT (SDIO) | | | | | |
| Logic 1 Voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 Voltage | Full | 0 | | 0.8 | V |
| Input Resistance | 25°C | | 26 | | kΩ |
| Input Capacitance | 25°C | | 5 | | pF |
| LOGIC OUTPUT (SDIO) ³ | | | | | |
| Logic 1 Voltage (I _{OH} = 800 μA) | Full | | 1.79 | | V |
| Logic 0 Voltage (I _{OL} = 50 μA) | Full | | | 0.05 | V |
| DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644 | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage (V _{OD}) | Full | 290 | 345 | 400 | mV |
| Output Offset Voltage (V _{OS}) | Full | 1.15 | 1.25 | 1.35 | V |
| Output Coding (Default) | | | Twos complement | | |
| DIGITAL OUTPUTS (D0±x, D1±x), LOW POWER, REDUCED SIGNAL OPTION | | | | | |
| Logic Compliance | | | LVDS | | |
| Differential Output Voltage (V _{OD}) | Full | 160 | 200 | 230 | mV |
| Output Offset Voltage (V _{OS}) | Full | 1.15 | 1.25 | 1.35 | V |
| Output Coding (Default) | | | Twos complement | | |

¹ See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for definitions and for details on how these tests were completed.

² This is specified for LVDS and LVPECL only.

³ This is specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = -1.0 dBFS, unless otherwise noted.

Table 4.

| Parameter ^{1,2} | Temp | Min | Typ | Max | Unit |
|--|------|---------------------------------|--|---------------------------------|--------------|
| CLOCK³ | | | | | |
| Input Clock Rate | Full | 10 | | 1000 | MHz |
| Conversion Rate ⁴ | Full | 10 | | 80/105/125 | MSPS |
| Clock Pulse Width High (t _{EH}) | Full | | 6.25/4.76/4.00 | | ns |
| Clock Pulse Width Low (t _{EL}) | Full | | 6.25/4.76/4.00 | | ns |
| OUTPUT PARAMETERS³ | | | | | |
| Propagation Delay (t _{PD}) | Full | 1.5 | 2.3 | 3.1 | ns |
| Rise Time (t _r) (20% to 80%) | Full | | 300 | | ps |
| Fall Time (t _f) (20% to 80%) | Full | | 300 | | ps |
| FCO Propagation Delay (t _{FCO}) | Full | 1.5 | 2.3 | 3.1 | ns |
| DCO Propagation Delay (t _{CPD}) ⁵ | Full | | t _{FCO} + (t _{SAMPLE} /16) | | ns |
| DCO to Data Delay (t _{DATA}) ⁵ | Full | (t _{SAMPLE} /16) - 300 | (t _{SAMPLE} /16) | (t _{SAMPLE} /16) + 300 | ps |
| DCO to FCO Delay (t _{FRAME}) ⁵ | Full | (t _{SAMPLE} /16) - 300 | (t _{SAMPLE} /16) | (t _{SAMPLE} /16) + 300 | ps |
| Lane Delay (t _{LD}) | | | 90 | | ps |
| Data to Data Skew (t _{DATA-MAX} - t _{DATA-MIN}) | Full | | ±50 | ±200 | ps |
| Wake-Up Time (Standby) | 25°C | | 250 | | ns |
| Wake-Up Time (Power-Down) ⁶ | 25°C | | 375 | | µs |
| Pipeline Latency | Full | | 16 | | Clock cycles |
| APERTURE | | | | | |
| Aperture Delay (t _A) | 25°C | | 1 | | ns |
| Aperture Uncertainty (Jitter, t _j) | 25°C | | 135 | | fs rms |
| Out-of-Range Recovery Time | 25°C | | 1 | | Clock cycles |

¹ See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

² Measured on standard FR-4 material.

³ Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.

⁴ The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.

⁵ t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. t_{SAMPLE} = 1/f_S.

⁶ Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

| Parameter | Description | Limit | Unit |
|---------------------------------|--|-------|--------|
| SYNC TIMING REQUIREMENTS | | | |
| t _{SSYNC} | SYNC to rising edge of CLK+ setup time | 1.2 | ns min |
| t _{HSYNC} | SYNC to rising edge of CLK+ hold time | -0.2 | ns min |
| SPI TIMING REQUIREMENTS | | | |
| | See Figure 74 | | |
| t _{DS} | Setup time between the data and the rising edge of SCLK | 2 | ns min |
| t _{DH} | Hold time between the data and the rising edge of SCLK | 2 | ns min |
| t _{CLK} | Period of the SCLK | 40 | ns min |
| t _S | Setup time between CSB and SCLK | 2 | ns min |
| t _H | Hold time between CSB and SCLK | 2 | ns min |
| t _{HIGH} | SCLK pulse width high | 10 | ns min |
| t _{LOW} | SCLK pulse width low | 10 | ns min |
| t _{EN_SDIO} | Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 74) | 10 | ns min |
| t _{DIS_SDIO} | Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 74) | 10 | ns min |

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 21 for SPI register settings.

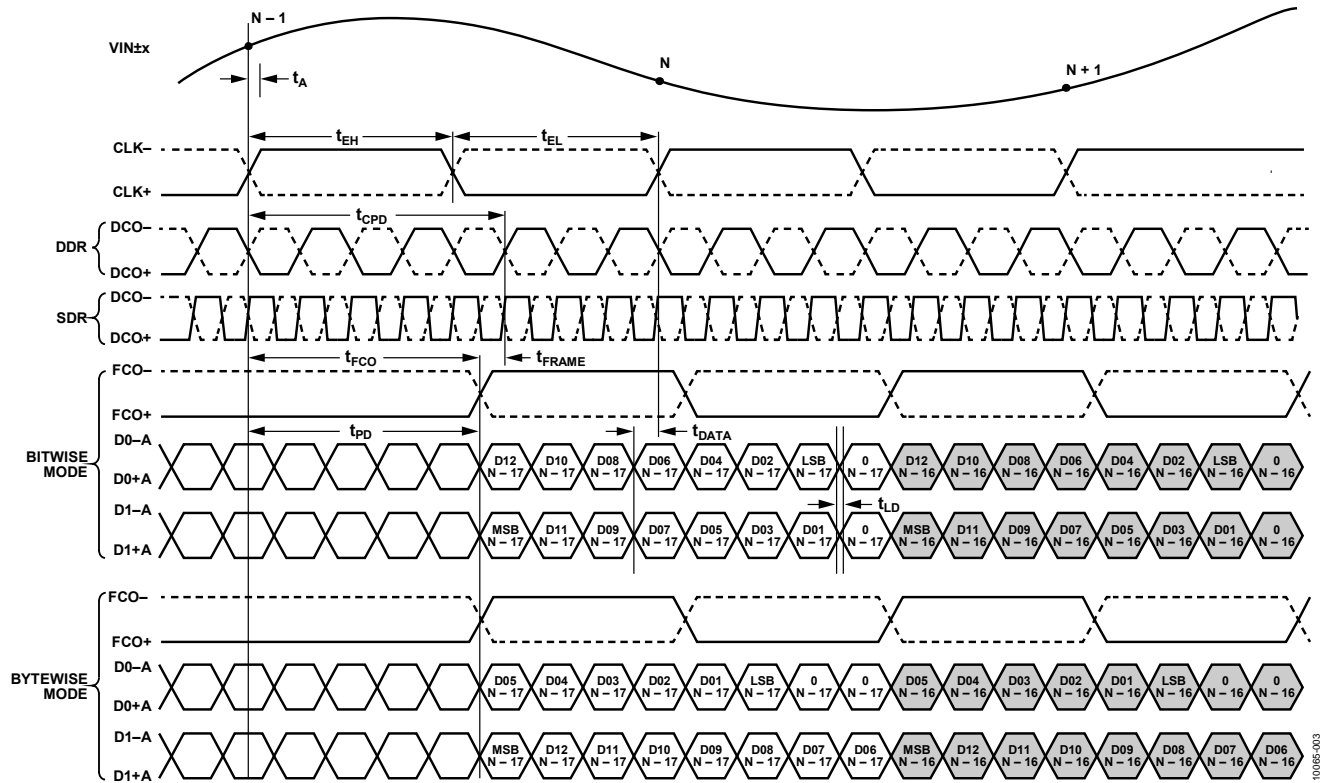


Figure 2. 16-Bit DDR/SDR, Two-Lane, 1x Frame Mode (Default)

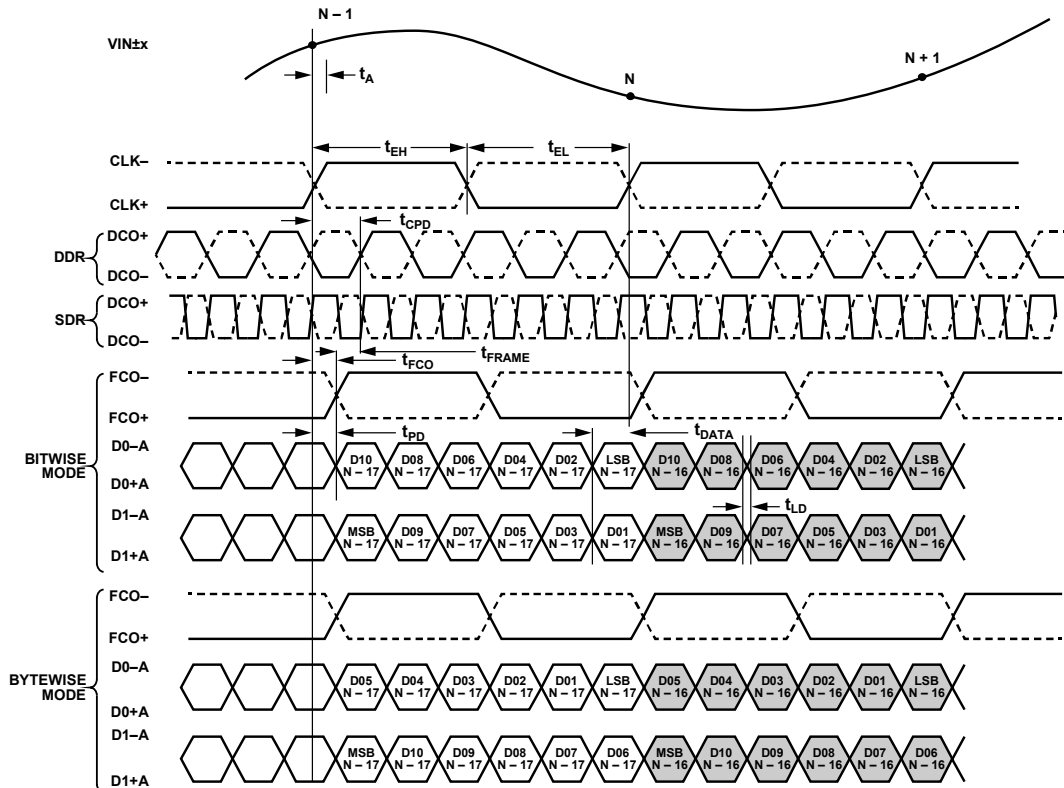


Figure 3. 12-Bit DDR/SDR, Two-Lane, 1x Frame Mode

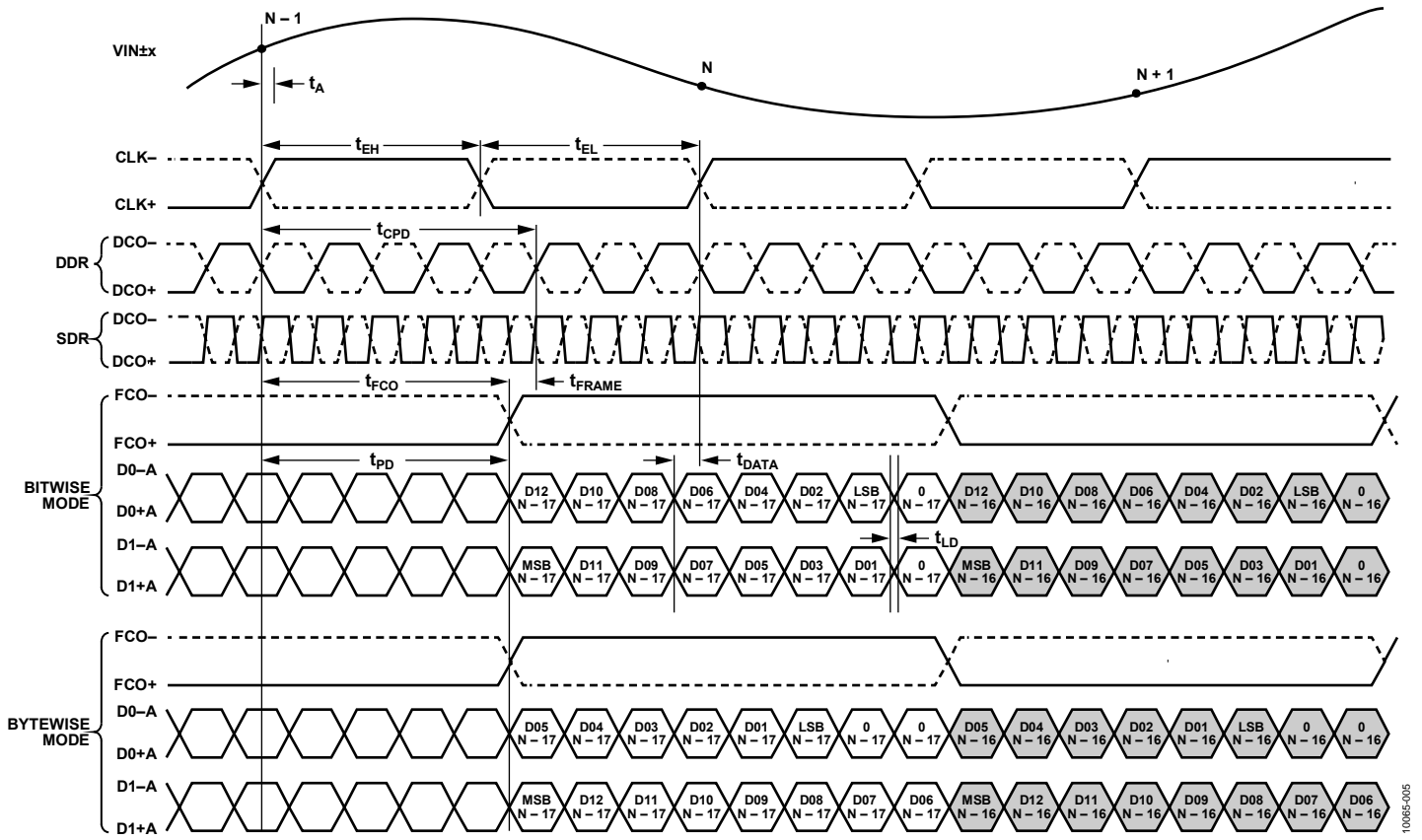


Figure 4. 16-Bit DDR/SDR, Two-Lane, 2x Frame Mode

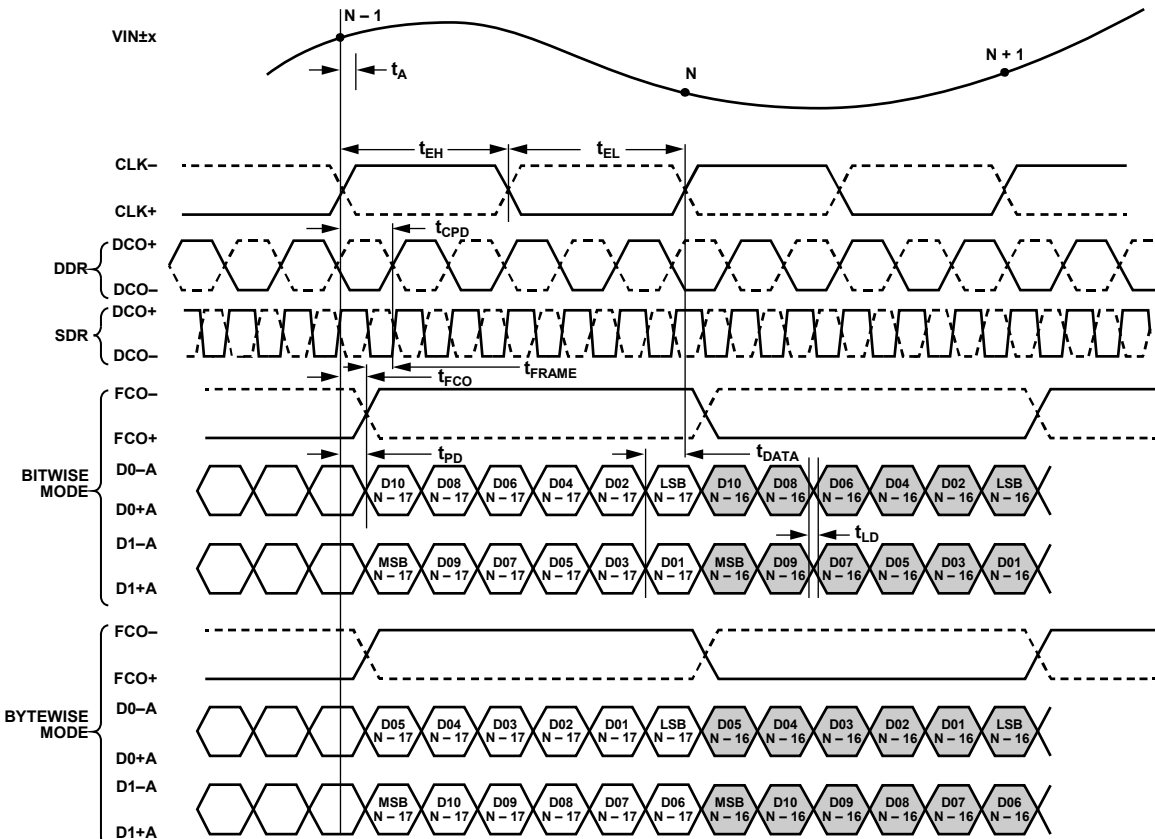


Figure 5. 12-Bit DDR/SDR, Two-Lane, 2x Frame Mode

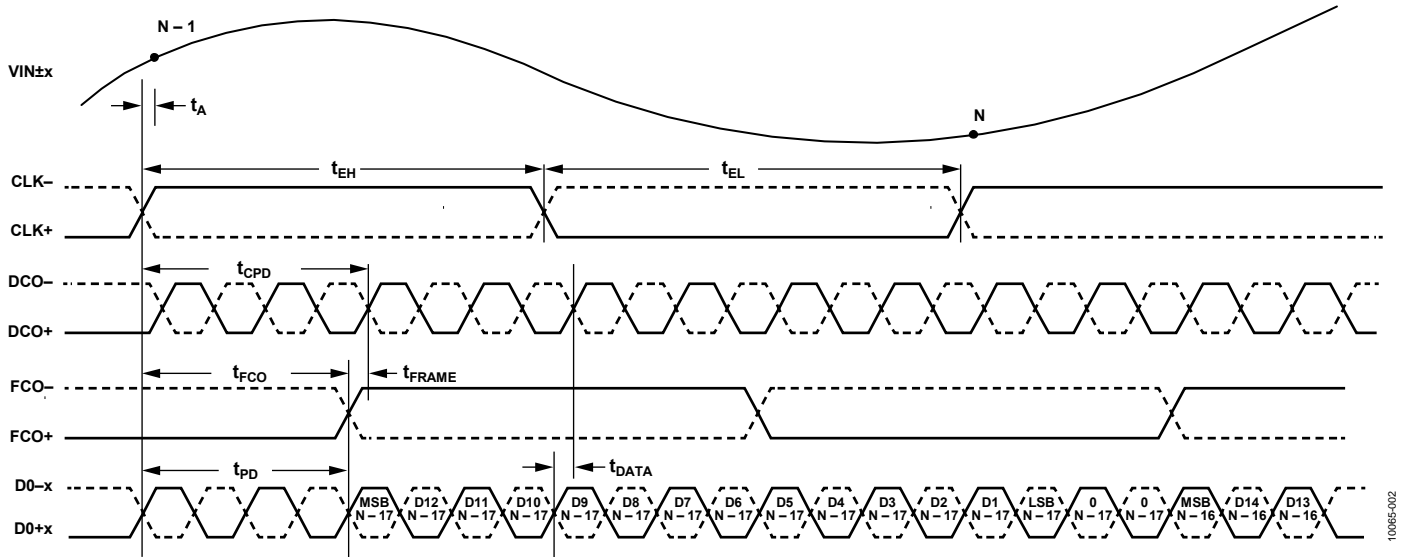


Figure 6. Wordwise DDR, One-Lane, 1x Frame, 16-Bit Output Mode

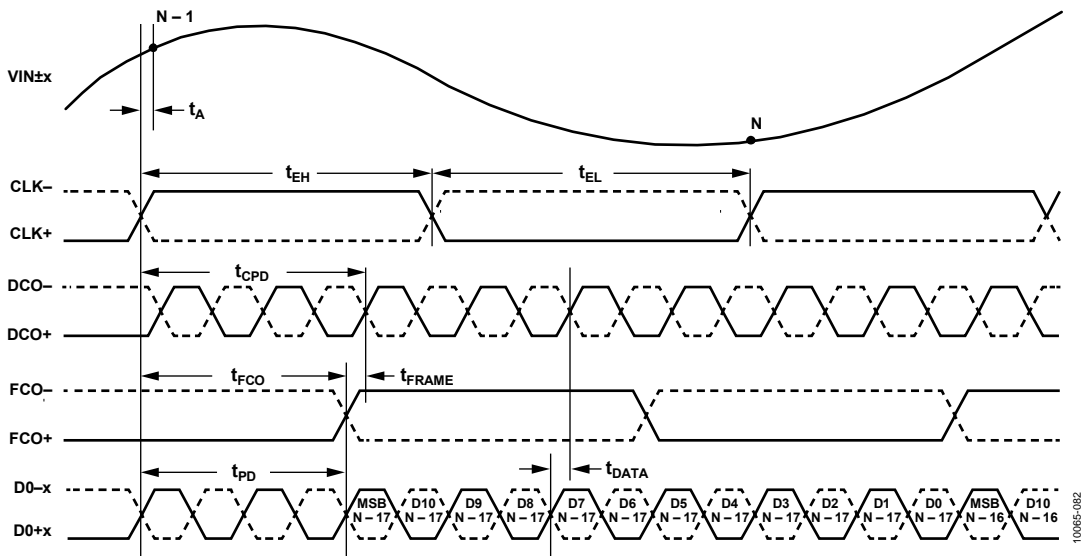


Figure 7. Wordwise DDR, One-Lane, 1x Frame, 12-Bit Output Mode

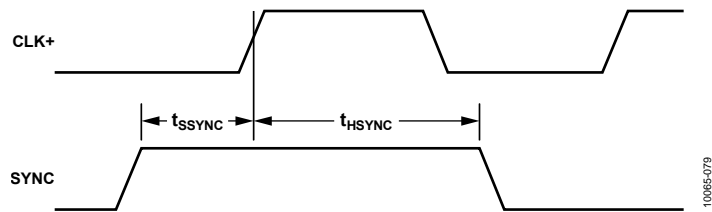


Figure 8. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

| Parameter | Rating |
|--|------------------|
| Electrical | |
| AVDD to AGND | −0.3 V to +2.0 V |
| DRVDD to AGND | −0.3 V to +2.0 V |
| Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND | −0.3 V to +2.0 V |
| CLK+, CLK− to AGND | −0.3 V to +2.0 V |
| VIN+x, VIN−x to AGND | −0.3 V to +2.0 V |
| SCLK/DTP, SDIO/OLM, CSB to AGND | −0.3 V to +2.0 V |
| SYNC, PDWN to AGND | −0.3 V to +2.0 V |
| RBIAS to AGND | −0.3 V to +2.0 V |
| VREF, SENSE to AGND | −0.3 V to +2.0 V |
| Environmental | |
| Operating Temperature Range (Ambient) | −40°C to +85°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Storage Temperature Range (Ambient) | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 7. Thermal Resistance

| Package Type | Air Flow Velocity (m/sec) | θ_{JA}^1 | θ_{JB} | θ_{JC} | Unit |
|---------------------------|---------------------------|-----------------|---------------|---------------|------|
| 48-Lead LFCSP | 0.0 | 23.7 | 7.8 | 7.1 | °C/W |
| 7 mm × 7 mm (CP-48-13) | 1.0 | 20.0 | N/A | N/A | °C/W |
| | 2.5 | 18.7 | N/A | N/A | °C/W |

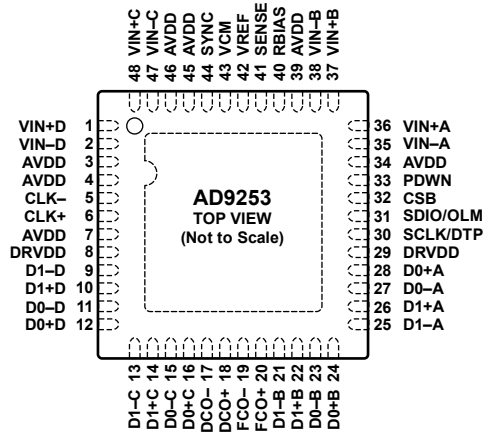
¹ θ_{JA} for a 4-layer PCB with solid ground plane (simulated). Exposed pad soldered to PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 9. 48-Lead LFCSP Pin Configuration, Top View

Table 8. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|-------------------------|-------------------|--|
| 0 | AGND, Exposed Pad | Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation. |
| 1 | VIN+D | ADC D Analog Input True. |
| 2 | VIN-D | ADC D Analog Input Complement. |
| 3, 4, 7, 34, 39, 45, 46 | AVDD | 1.8 V Analog Supply Pins. |
| 5, 6 | CLK-, CLK+ | Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs. |
| 8, 29 | DRVDD | Digital Output Driver Supply. |
| 9, 10 | D1-D, D1+D | Channel D Digital Outputs, (Disabled in One-Lane Mode ¹). |
| 11, 12 | D0-D, D0+D | Channel D Digital Outputs, (Disabled in One-Lane Mode ¹). |
| 13, 14 | D1-C, D1+C | Channel C Digital Outputs, (Channel D Digital Outputs in One-Lane Mode ¹). |
| 15, 16 | D0-C, D0+C | Channel C Digital Outputs. |
| 17, 18 | DCO-, DCO+ | Data Clock Outputs. |
| 19, 20 | FCO-, FCO+ | Frame Clock Outputs. |
| 21, 22 | D1-B, D1+B | Channel B Digital Outputs. |
| 23, 24 | D0-B, D0+B | Channel B Digital Outputs, (Channel A Digital Outputs in One-Lane Mode ¹). |
| 25, 26 | D1-A, D1+A | Channel A Digital Outputs, (Disabled in One-Lane Mode ¹). |
| 27, 28 | D0-A, D0+A | Channel A Digital Outputs, (Disabled in One-Lane Mode ¹). |
| 30 | SCLK/DTP | SPI Clock Input/Digital Test Pattern. |
| 31 | SDIO/OLM | SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode. |
| 32 | CSB | SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up. |
| 33 | PDWN | Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation. |
| 35 | VIN-A | ADC A Analog Input Complement. |
| 36 | VIN+A | ADC A Analog Input True. |
| 37 | VIN+B | ADC B Analog Input True. |
| 38 | VIN-B | ADC B Analog Input Complement. |
| 40 | RBIAS | Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground. |
| 41 | SENSE | Reference Mode Selection. |
| 42 | VREF | Voltage Reference Input and Output. |
| 43 | VCM | Analog Input Common-Mode Voltage. |

| Pin No. | Mnemonic | Description |
|---------|----------|---|
| 44 | SYNC | Digital Input. SYNC input to clock divider. |
| 47 | VIN-C | ADC C Analog Input Complement. |
| 48 | VIN+C | ADC C Analog Input True. |

¹ Output channel assignments are shown first for default two-lane mode. If one-lane mode is used, output channel assignments change as indicated in parenthesis. Register 0x21 Bits[6:4] invoke one-lane mode.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9253-80

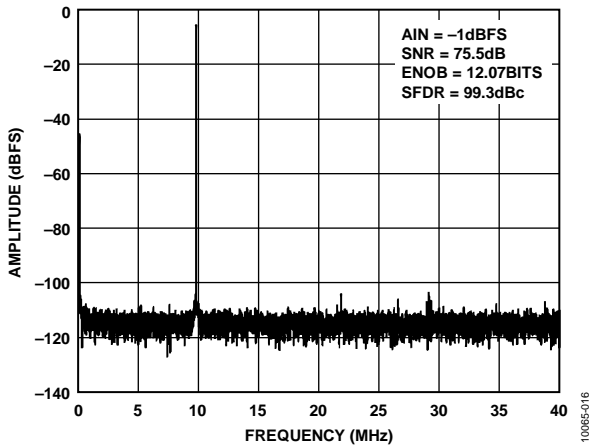


Figure 10. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 80$ MSPS

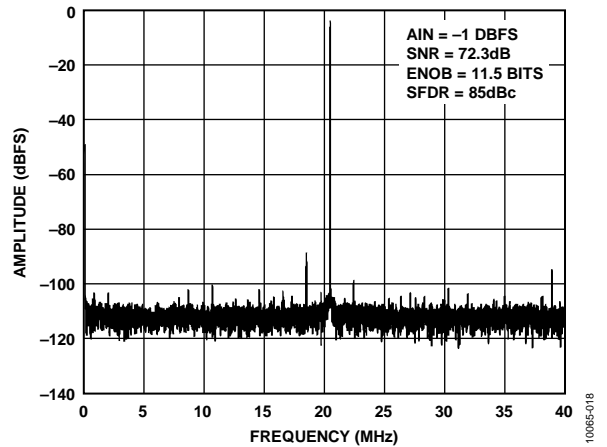


Figure 13. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 80$ MSPS

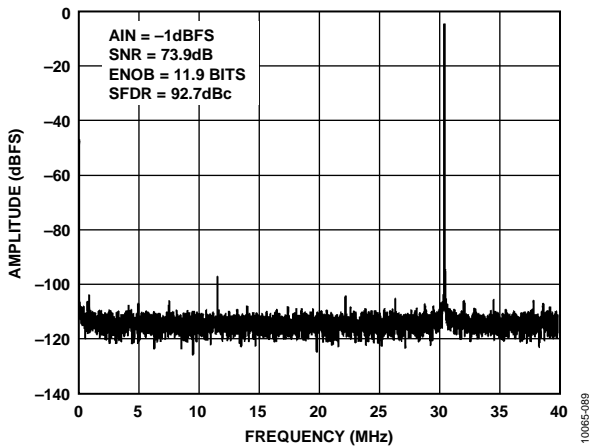


Figure 11. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 80$ MSPS

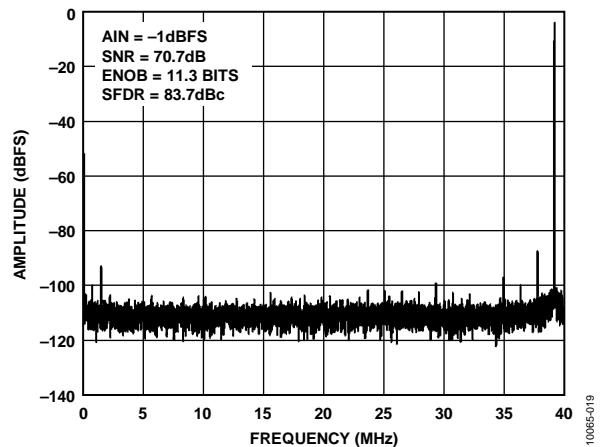


Figure 14. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 80$ MSPS

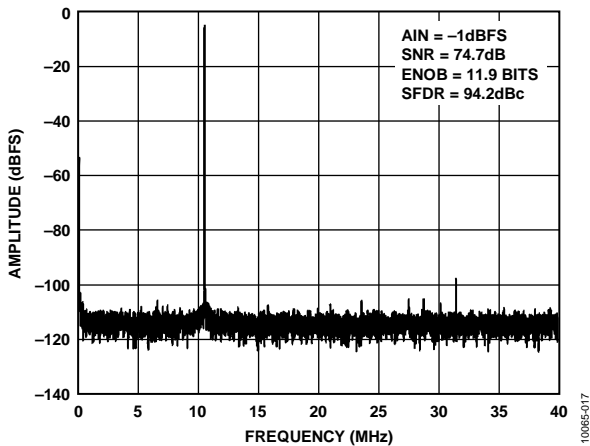


Figure 12. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 80$ MSPS

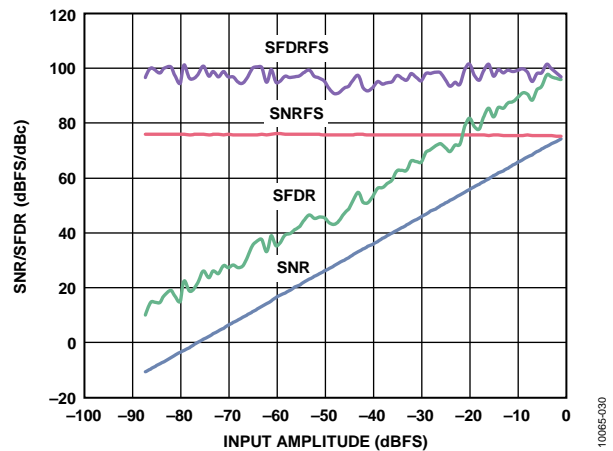


Figure 15. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 80$ MSPS

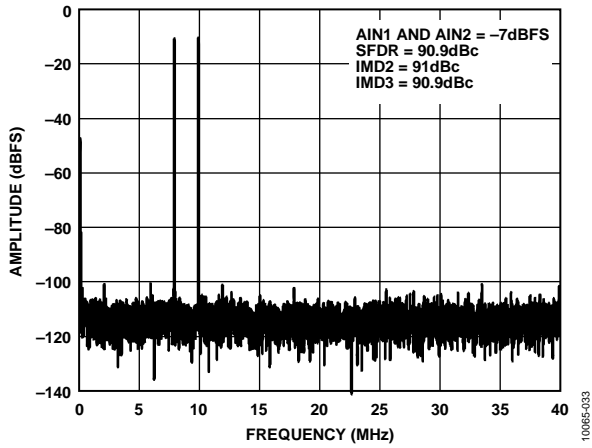


Figure 16. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 80$ MSPS

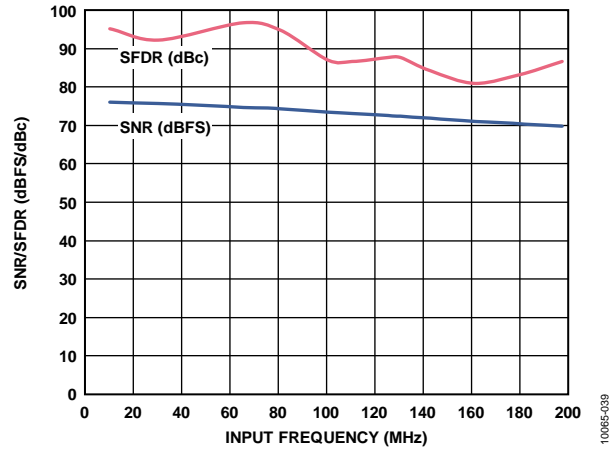


Figure 18. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 80$ MSPS

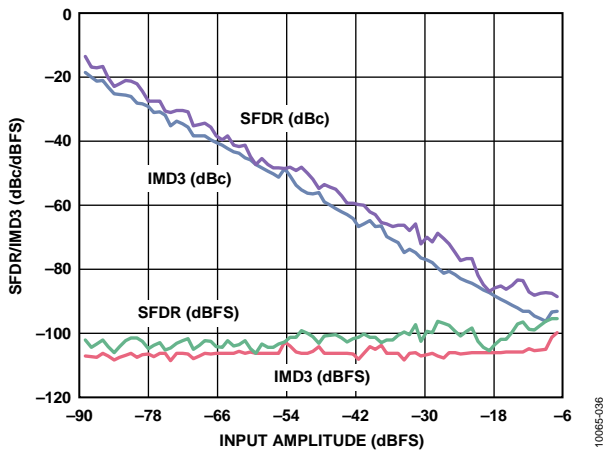


Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 80$ MSPS

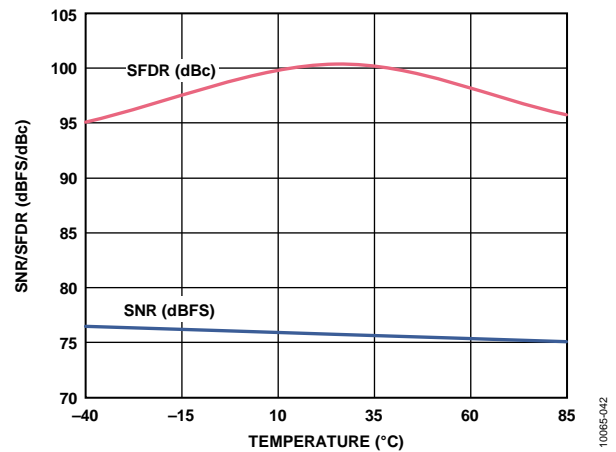


Figure 19. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 80$ MSPS

AD9253-105

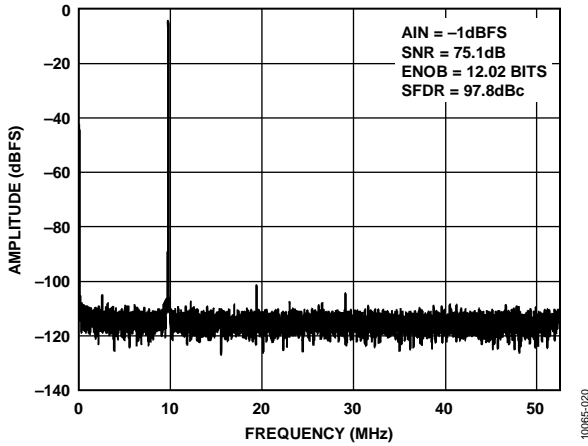


Figure 20. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 105$ MSPS

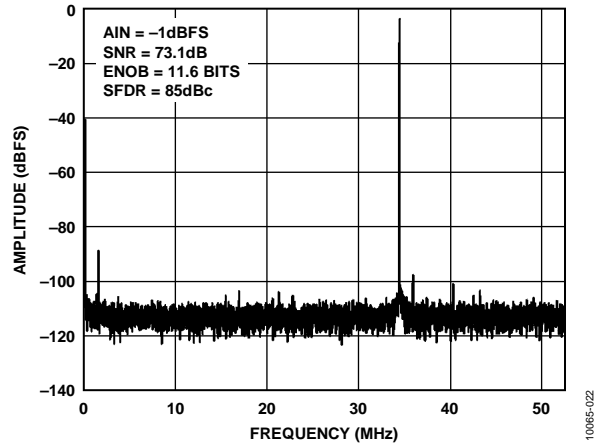


Figure 23. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 105$ MSPS

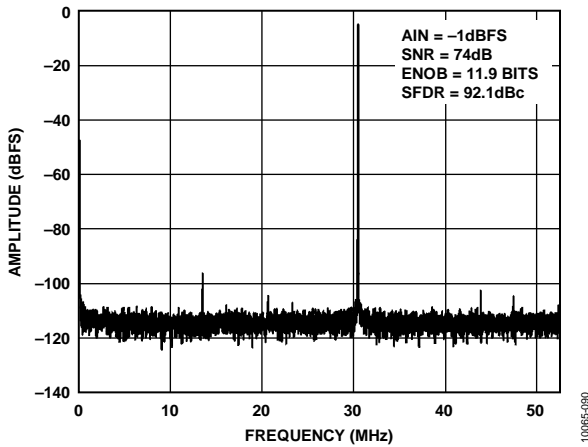


Figure 21. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 105$ MSPS

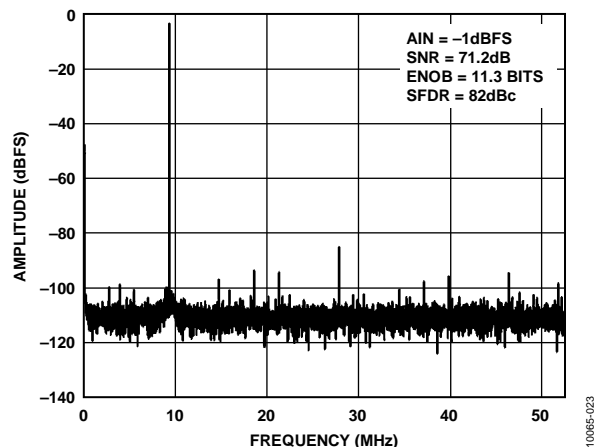


Figure 24. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 105$ MSPS

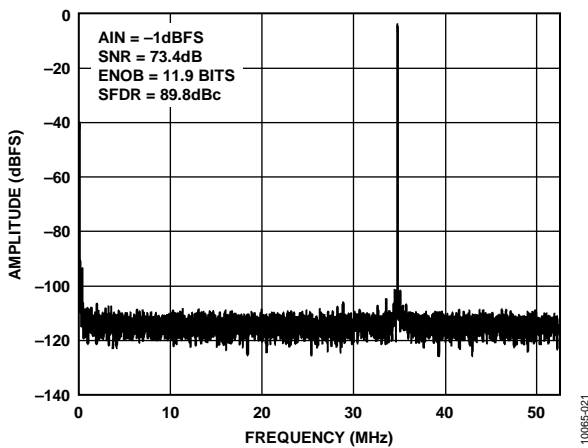


Figure 22. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 105$ MSPS

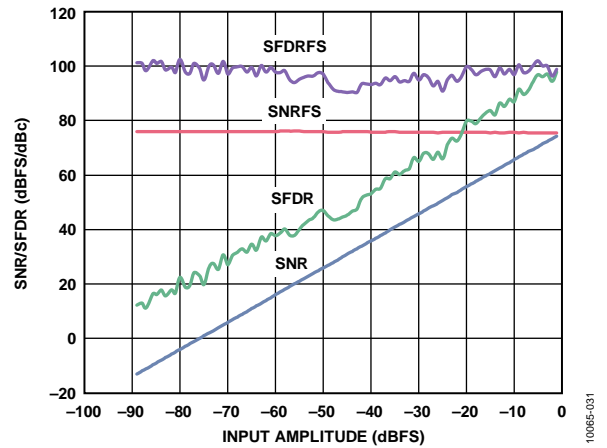


Figure 25. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 105$ MSPS

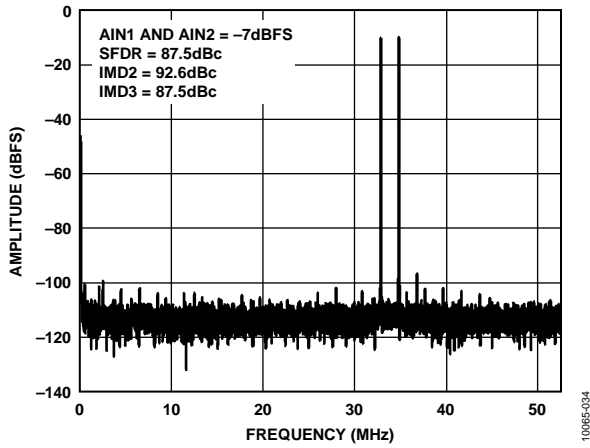


Figure 26. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 105$ MSPS

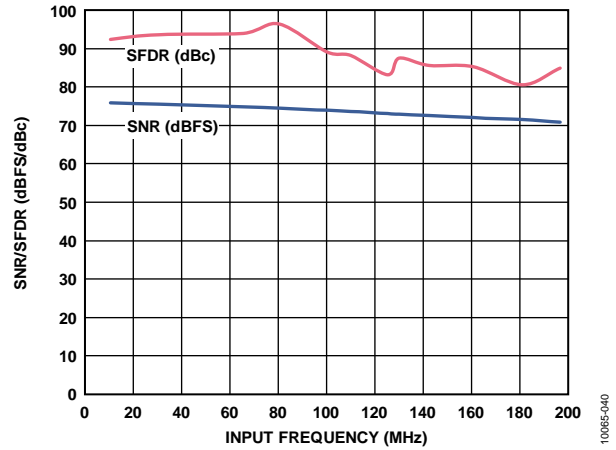


Figure 28. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 105$ MSPS

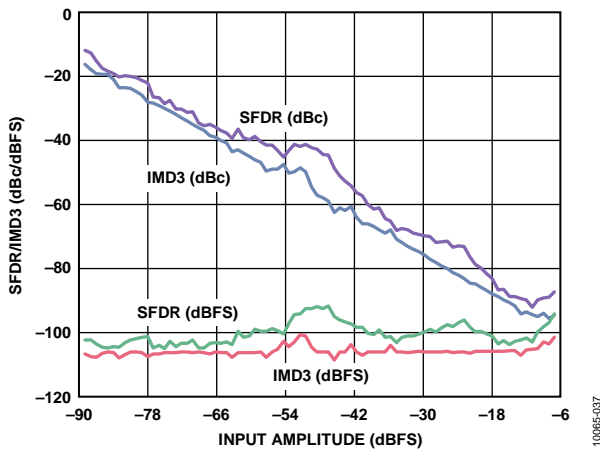


Figure 27. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 105$ MSPS

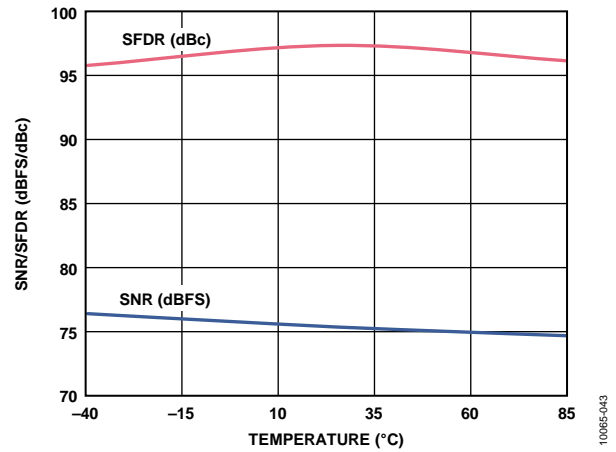


Figure 29. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 105$ MSPS

AD9253-125

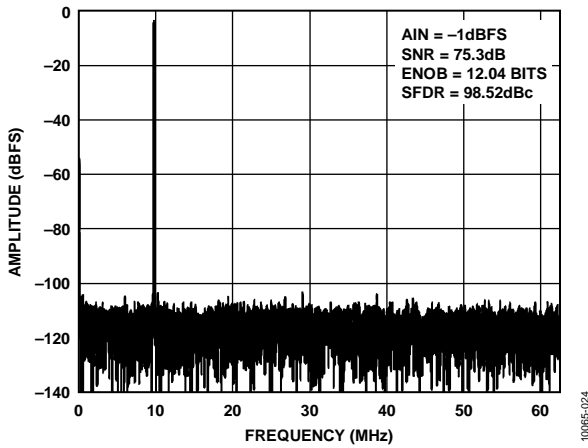


Figure 30. Single-Tone 16k FFT with $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

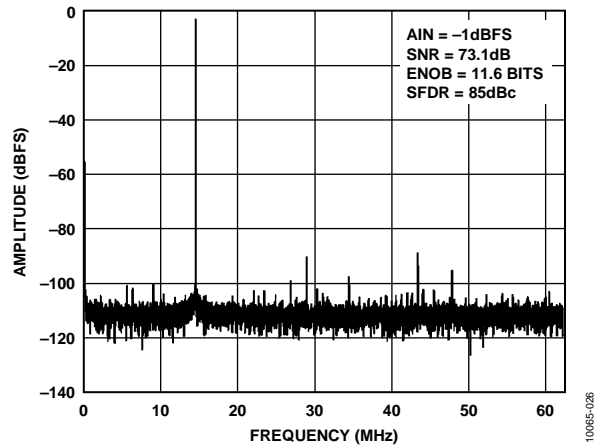


Figure 33. Single-Tone 16k FFT with $f_{IN} = 140$ MHz, $f_{SAMPLE} = 125$ MSPS

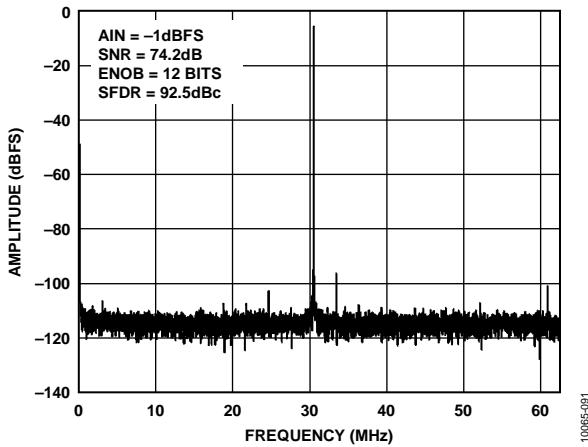


Figure 31. Single-Tone 16k FFT with $f_{IN} = 30.5$ MHz, $f_{SAMPLE} = 125$ MSPS

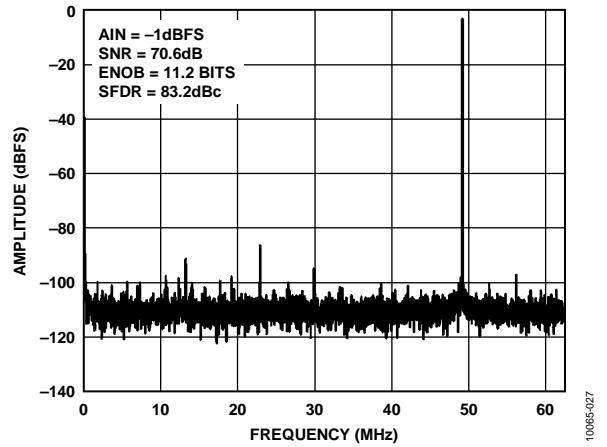


Figure 34. Single-Tone 16k FFT with $f_{IN} = 200$ MHz, $f_{SAMPLE} = 125$ MSPS

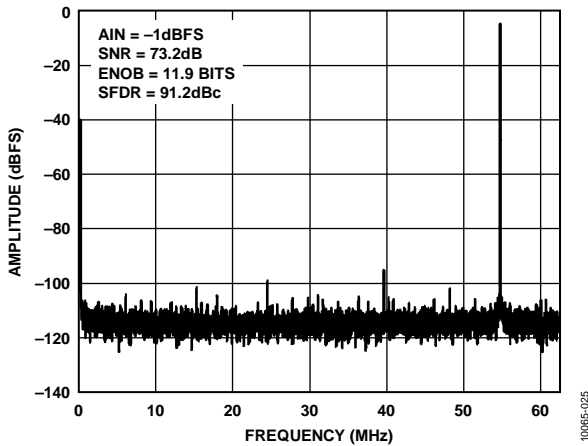


Figure 32. Single-Tone 16k FFT with $f_{IN} = 70$ MHz, $f_{SAMPLE} = 125$ MSPS

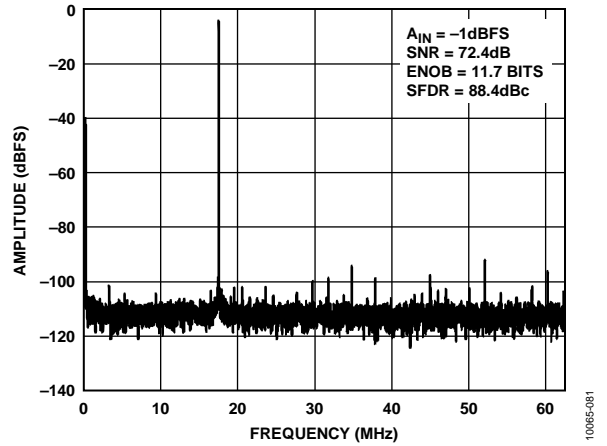


Figure 35. Single-Tone 16k FFT with $f_{IN} = 140$ MHz at $f_{SAMPLE} = 122.88$ MSPS

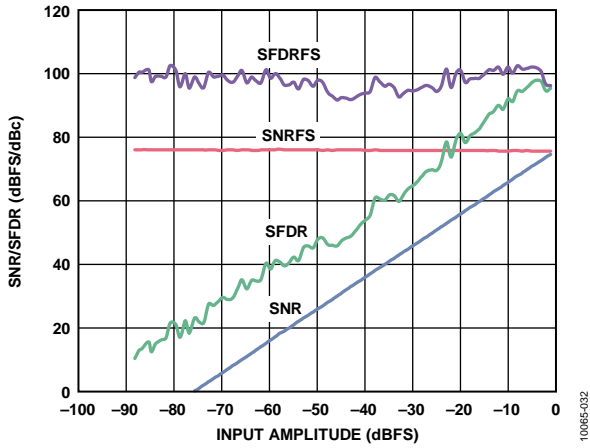


Figure 36. SNR/SFDR vs. Analog Input Level, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

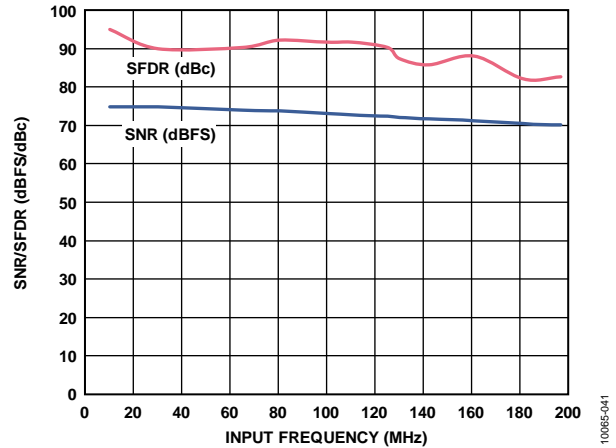


Figure 39. SNR/SFDR vs. f_{IN} , $f_{SAMPLE} = 125$ MSPS

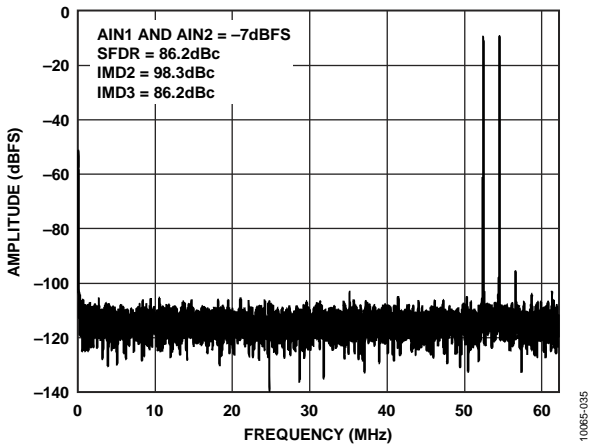


Figure 37. Two-Tone 16k FFT with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 125$ MSPS

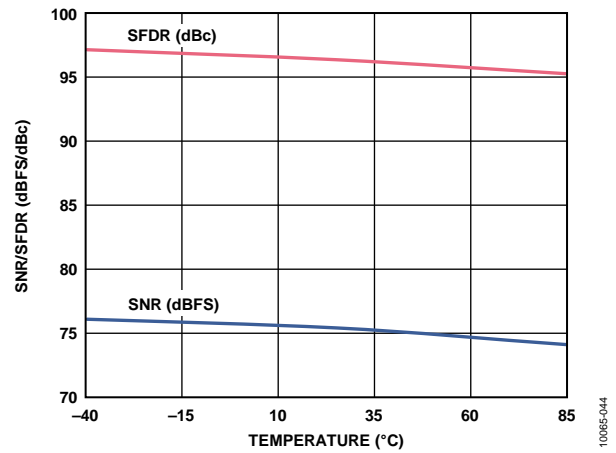


Figure 40. SNR/SFDR vs. Temperature, $f_{IN} = 10.3$ MHz, $f_{SAMPLE} = 125$ MSPS

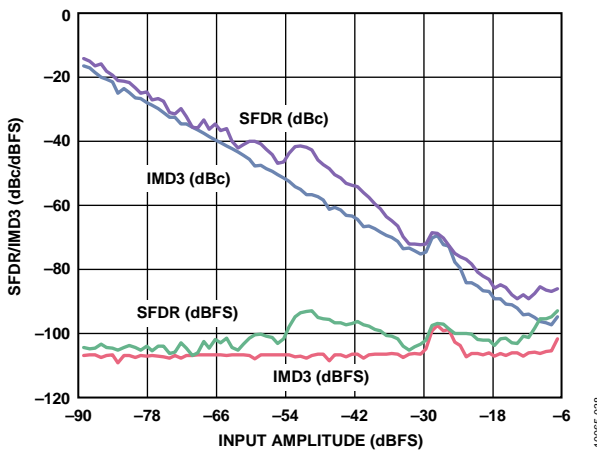


Figure 38. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with $f_{IN1} = 70.5$ MHz and $f_{IN2} = 72.5$ MHz, $f_{SAMPLE} = 125$ MSPS

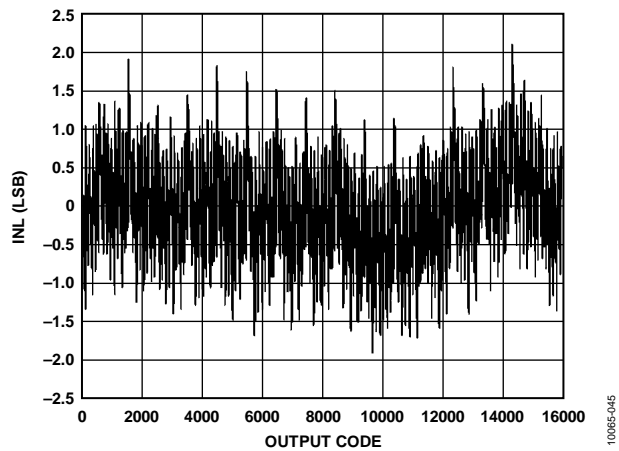


Figure 41. INL, $f_{IN} = 9.7$ MHz, $f_{SAMPLE} = 125$ MSPS

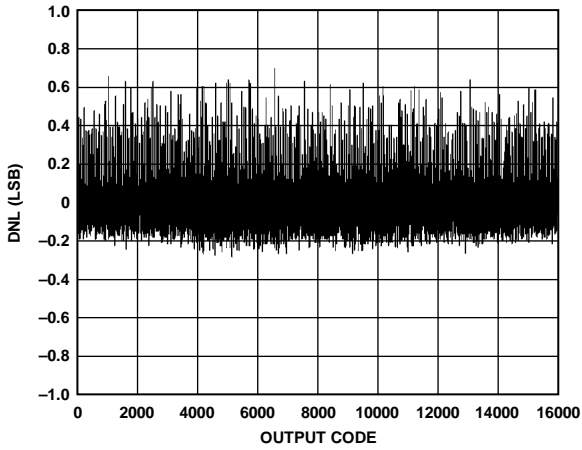


Figure 42. DNL, $f_{IN} = 9.7 \text{ MHz}$, $f_{SAMPLE} = 125 \text{ MSPS}$

10065-046

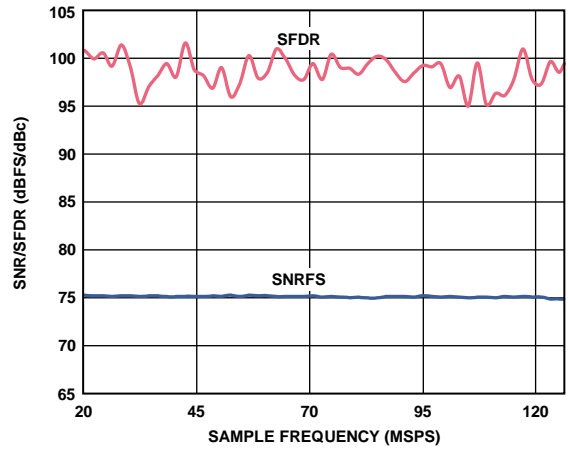


Figure 45. SNR/SFDR vs. Encode, $f_{IN} = 9.7 \text{ MHz}$, $f_{SAMPLE} = 125 \text{ MSPS}$

10065-028

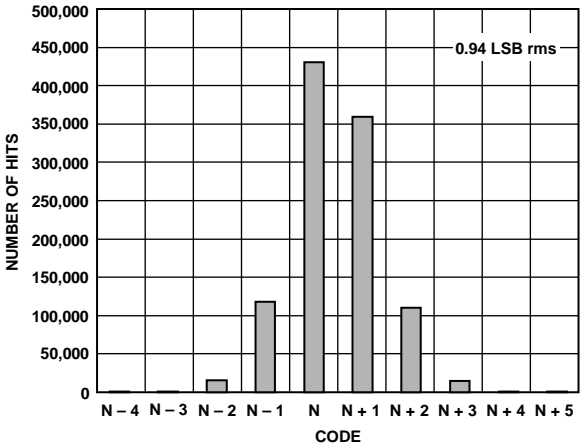


Figure 43. Input-Referred Noise Histogram, $f_{SAMPLE} = 125 \text{ MSPS}$

10065-050

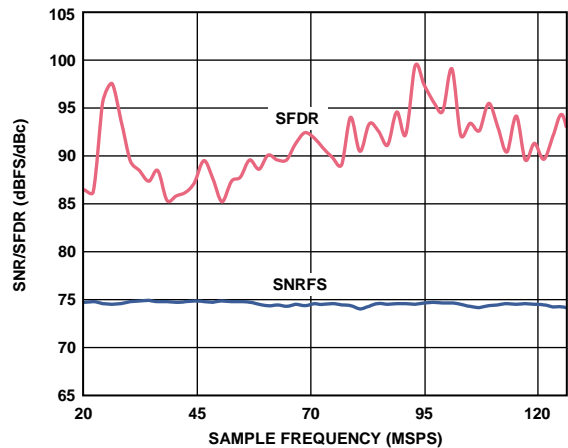


Figure 46. SNR/SFDR vs. Encode, $f_{IN} = 70 \text{ MHz}$, $f_{SAMPLE} = 125 \text{ MSPS}$

10065-029

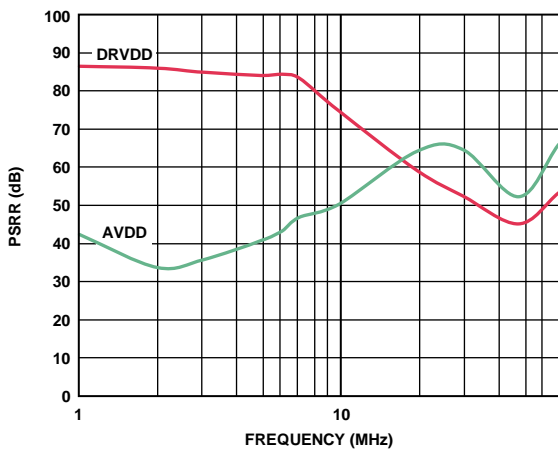


Figure 44. PSRR vs. Frequency, $f_{CLK} = 125 \text{ MHz}$, $f_{SAMPLE} = 125 \text{ MSPS}$

10065-087

EQUIVALENT CIRCUITS

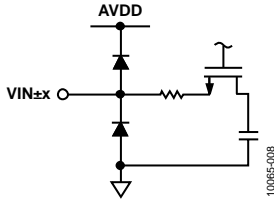


Figure 47. Equivalent Analog Input Circuit

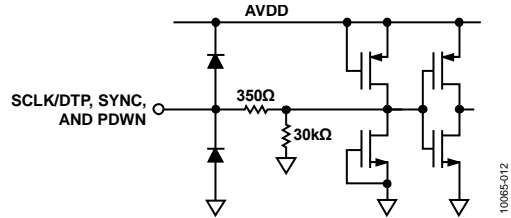


Figure 51. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

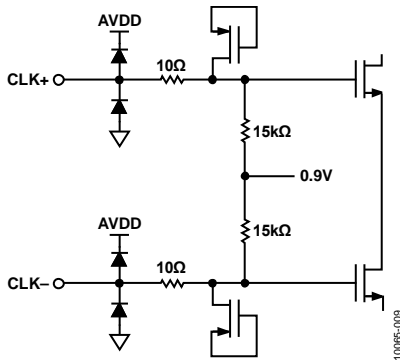


Figure 48. Equivalent Clock Input Circuit

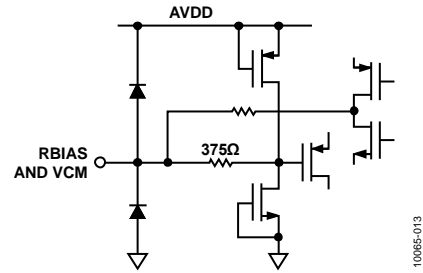


Figure 52. Equivalent RBIAS and VCM Circuit

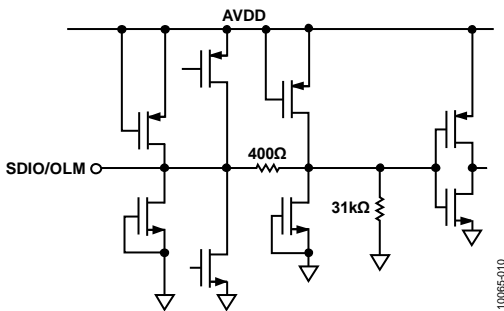


Figure 49. Equivalent SDIO/OLM Input Circuit

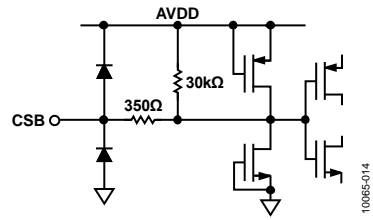


Figure 53. Equivalent CSB Input Circuit

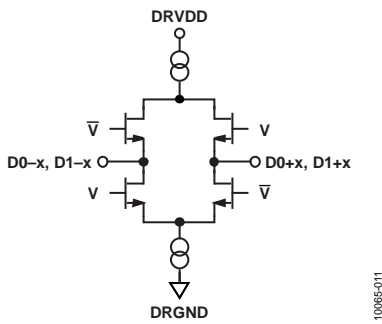


Figure 50. Equivalent Digital Output Circuit

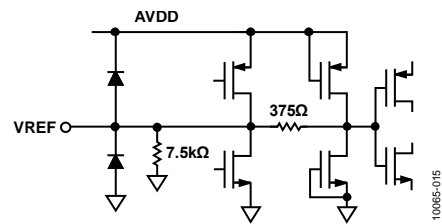


Figure 54. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9253 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 16-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9253 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

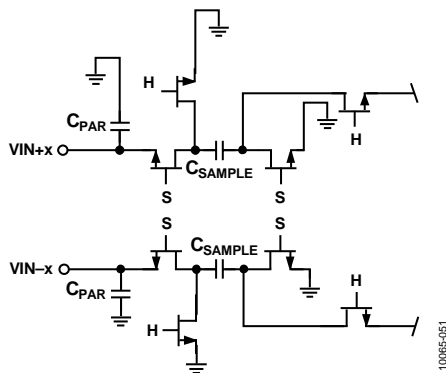


Figure 55. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 55). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from

the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the Analog Dialogue article “Transformer-Coupled Front-End for Wideband A/D Converters” (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9253 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 56.

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 μF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9253, the largest input span available is 2 V p-p.

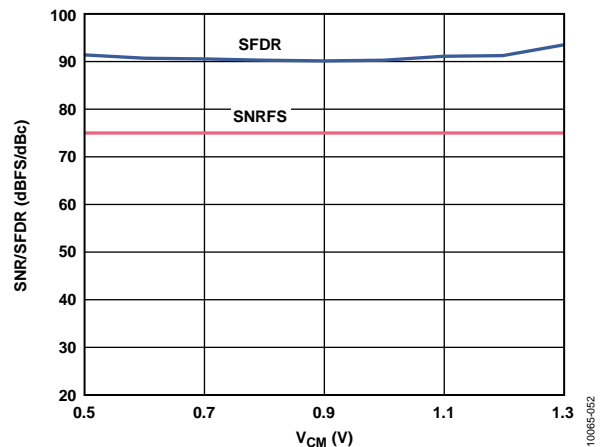


Figure 56. SNR/SFDR vs. Common-Mode Voltage, $f_{IN} = 9.7 \text{ MHz}$, $f_{SAMPLE} = 125 \text{ MSPS}$

If the internal reference of the AD9253 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 60 shows how the internal reference voltage is affected by loading.

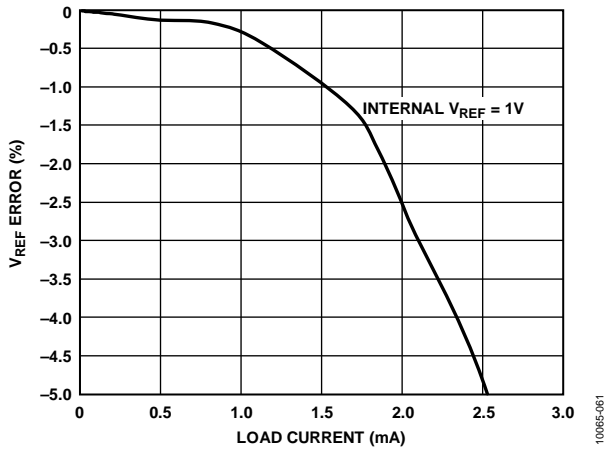


Figure 60. VREF Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 61 shows the typical drift characteristics of the internal reference in 1.0 V mode.

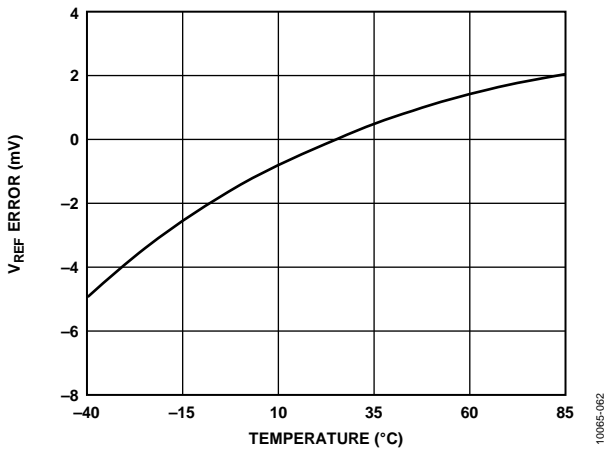


Figure 61. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 54). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

It is not recommended to leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9253 sample clock inputs, CLK+ and CLK-, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally (see Figure 48) and require no external bias.

Clock Input Options

The AD9253 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 62 and Figure 63 show two preferred methods for clocking the AD9253 (at clock rates up to 1 GHz prior to internal CLK divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200 MHz. The antiparallel Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9253 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9253 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken in choosing the appropriate signal limiting diode.

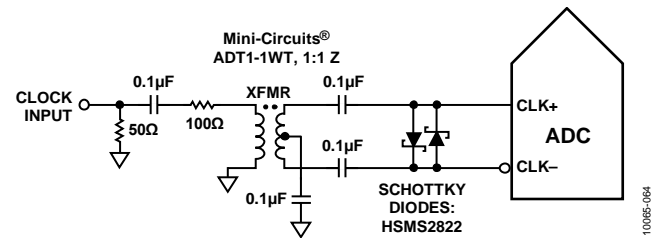


Figure 62. Transformer-Coupled Differential Clock (Up to 200 MHz)

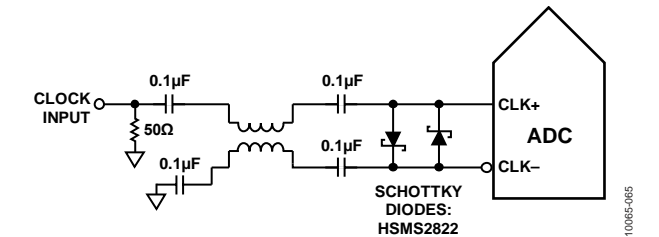


Figure 63. Balun-Coupled Differential Clock (Up to 1 GHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 65. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 66. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK- pin to ground with a 0.1 μF capacitor (see Figure 67).

Input Clock Divider

The AD9253 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8.

The AD9253 clock divider can be synchronized using the external SYNC input. Bit 0 and Bit 1 of Register 0x109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9253 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9253. Noise and distortion perform-

ance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 64.

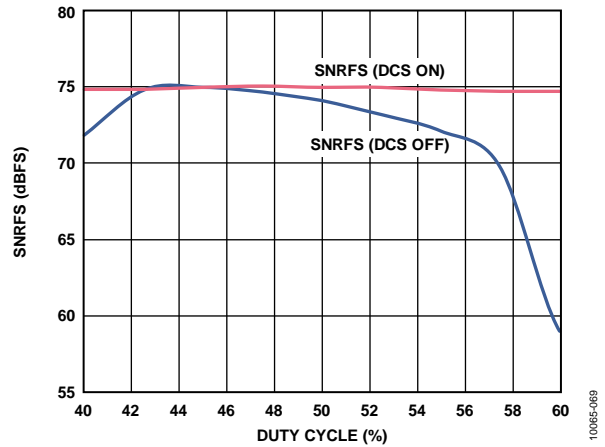


Figure 64. SNR vs. DCS On/Off

jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 μs to 5 μs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

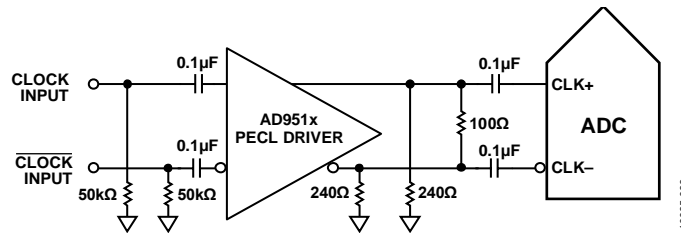


Figure 65. Differential PECL Sample Clock (Up to 1 GHz)

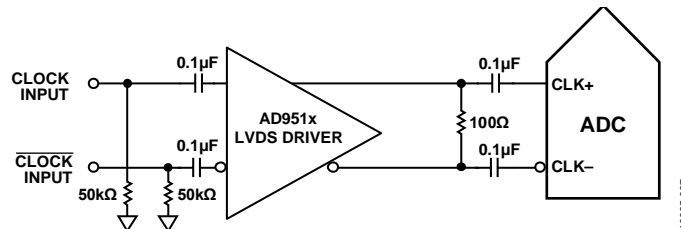


Figure 66. Differential LVDS Sample Clock (Up to 1 GHz)

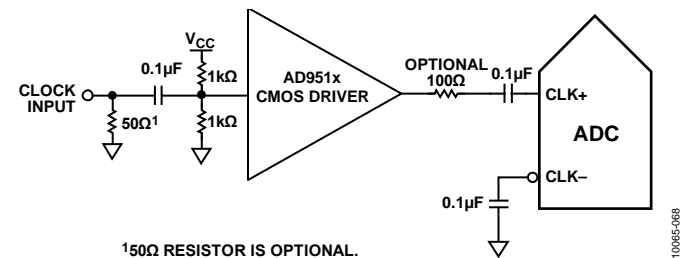


Figure 67. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_j) can be calculated by

$$SNR \text{ Degradation} = 20 \log_{10} \left(\frac{1}{2\pi \times f_A \times t_j} \right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 68).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9253. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the [AN-501 Application Note](#) and the [AN-756 Application Note](#) for more in-depth information about jitter performance as it relates to ADCs.

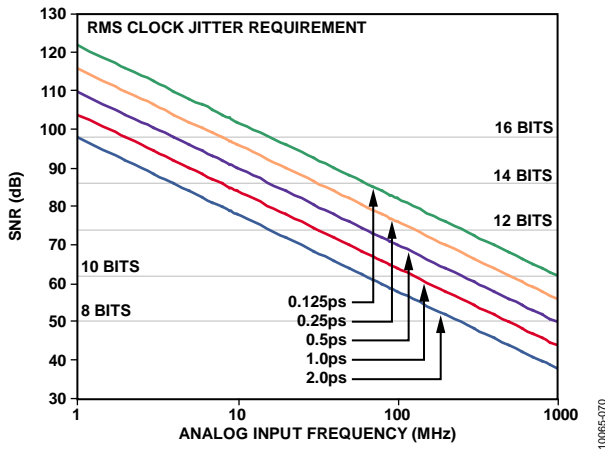


Figure 68. Ideal SNR vs. Input Frequency and Jitter

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 69, the power dissipated by the AD9253 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

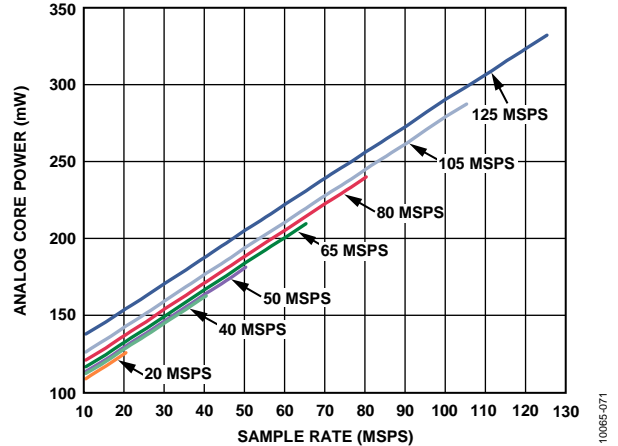


Figure 69. Analog Core Power vs. f_{SAMPLE} for $f_{IN} = 10.3 \text{ MHz}$

The AD9253 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9253 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9253 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current is reduced to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The AD9253 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 24 inches and that the differential output traces be close together and at equal lengths. An example of the FCO and data stream with proper trace length and position is shown in Figure 70. Figure 71 shows the LVDS output timing example in reduced range mode.

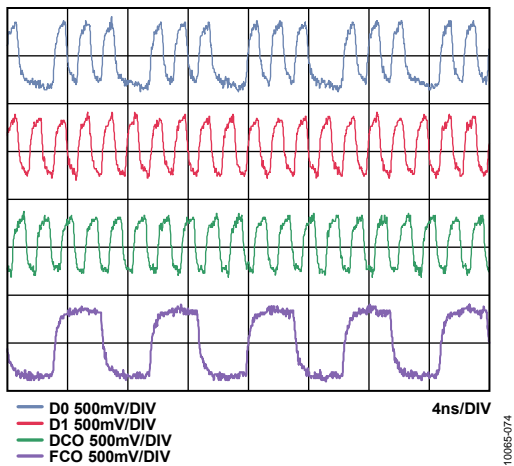


Figure 70. AD9253-125, LVDS Output Timing Example in ANSI-644 Mode (Default)

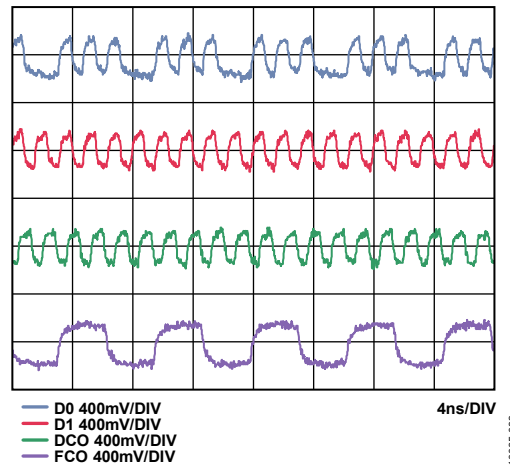


Figure 71. AD9253-125, LVDS Output Timing Example in Reduced Range Mode

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on standard FR-4 material is shown in Figure 72.

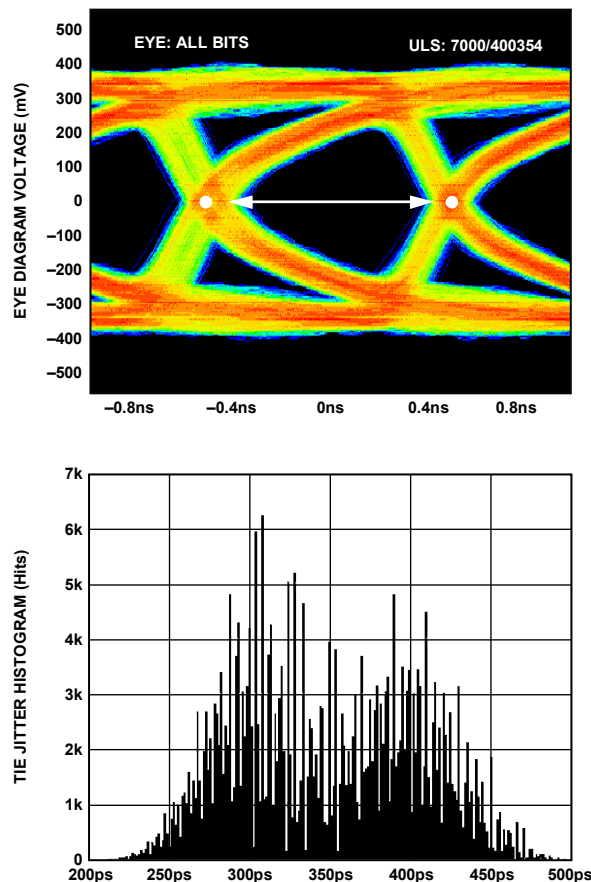


Figure 72. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Less than 24 Inches on Standard FR-4 Material, External 100 Ω Far-End Termination Only

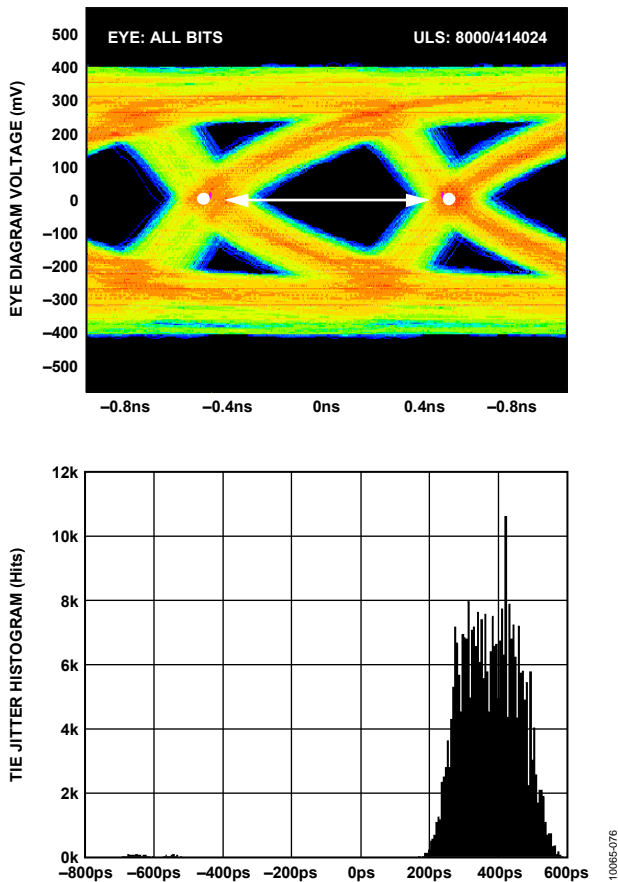


Figure 73. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater than 24 Inches on Standard FR-4 Material, External 100 Ω Far-End Termination Only

Figure 73 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the user’s responsibility to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of all four outputs to drive longer trace lengths. This can be achieved by programming Register 0x15. Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used.

The format of the output data is twos complement by default. An example of the output coding format can be found in Table 10. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in two lanes in DDR mode. The data rate for each serial stream is equal to 16 bits times the sample clock rate divided by the number of lanes, with a maximum of 1000 Mbps/lane [(16 bits × 125 MSPS)/2 = 1000 Mbps/lane]. The maximum allowable output data rate is 1 Gbps/lane. If one-lane mode is used, the data rate doubles for a given sample rate. To stay within the maximum data rate of 1 Gbps/lane, the sample rate is limited to a maximum of 62.5 MSPS in one-lane output mode.

The lowest typical conversion rate is 10 MSPS.

Two output clocks are provided to assist in capturing data from the AD9253. The DCO is used to clock the output data and is equal to four times the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the AD9253 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The FCO is used to signal the start of a new output byte and is equal to the sample clock rate in 1× frame mode. See the Timing Diagrams section for more information.

Table 10. Digital Output Coding

| Input (V) | Condition (V) | Offset Binary Output Mode | Twos Complement Mode |
|-------------|------------------|---------------------------|----------------------|
| VIN+ – VIN– | <–VREF – 0.5 LSB | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ – VIN– | –VREF | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ – VIN– | 0 V | 1000 0000 0000 0000 | 0000 0000 0000 0000 |
| VIN+ – VIN– | +VREF – 1.0 LSB | 1111 1111 1111 1100 | 0111 1111 1111 1100 |
| VIN+ – VIN– | >+VREF – 0.5 LSB | 1111 1111 1111 1100 | 0111 1111 1111 1100 |

Table 11. Flexible Output Test Modes

| Output Test Mode Bit Sequence | Pattern Name | Digital Output Word 1 | Digital Output Word 2 | Subject to Data Format Select | Notes |
|-------------------------------|--------------------------------|---|---|-------------------------------|--|
| 0000 | Off (default) | N/A | N/A | N/A | |
| 0001 | Midscale short | 1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit) | N/A | Yes | Offset binary code shown |
| 0010 | +Full-scale short | 1111 1111 1111 (12-bit) 1111 1111 1111 1100 (16-bit) | N/A | Yes | Offset binary code shown |
| 0011 | –Full-scale short | 0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit) | N/A | Yes | Offset binary code shown |
| 0100 | Checkerboard | 1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit) | 0101 0101 0101 (12-bit) 0101 0101 0101 0100 (16-bit) | No | |
| 0101 | PN sequence long ¹ | N/A | N/A | Yes | PN23 ITU 0.150 $X^{23} + X^{18} + 1$ |
| 0110 | PN sequence short ¹ | N/A | N/A | Yes | PN9 ITU 0.150 $X^9 + X^5 + 1$ |
| 0111 | One-/zero-word toggle | 1111 1111 1111 (12-bit) 111 1111 1111 1100 (16-bit) | 0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit) | No | |
| 1000 | User input | Register 0x19 to Register 0x1A | Register 0x1B to Register 0x1C | No | |
| 1001 | 1-/0-bit toggle | 1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit) | N/A | No | |
| 1010 | 1× sync | 0000 0011 1111 (12-bit) 0000 0001 1111 1100 (16-bit) | N/A | No | |
| 1011 | One bit high | 1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit) | N/A | No | Pattern associated with the external pin |
| 1100 | Mixed frequency | 1010 0011 0011 (12-bit) 1010 0001 1001 1100 (16-bit) | N/A | No | |

¹ All test mode options except PN sequence short and PN sequence long can support 12-bit to 16-bit word lengths to verify data capture to the receiver.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to one data cycle (30° relative to one DCO cycle). This enables the user to refine system timing margins if required. The default DCO± to output data edge timing, as shown in Figure 2, is 180° relative to one data cycle (90° relative to one DCO cycle).

A 12-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility to lower resolution systems. When changing the resolution to a 12-bit serial stream, the data stream is shortened. See Figure 3 for the 12-bit example. However, in the default option with the serial output number of bits at 16, the data stream stuffs two 0s at the end of the 14-bit serial data.

In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. This can be inverted so that the LSB is first in the data output serial stream by using the SPI.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 11 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various

ways, depending on the test pattern chosen. Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 12 for the initial values). The output is a parallel representation of the serial PN9 sequence in MSB-first format. The first output word is the first 14 bits of the PN9 sequence in MSB aligned form.

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 12 for the initial values) and the [AD9253](#) inverts the bit stream with relation to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB-first format. The first output word is the first 14 bits of the PN23 sequence in MSB aligned form.

Table 12. PN Sequence

| Sequence | Initial Value | Next Three Output Samples (MSB First) Twos Complement |
|-------------------|---------------|---|
| PN Sequence Short | 0x1FE0 | 0x1DF1, 0x3CC8, 0x294E |
| PN Sequence Long | 0x1FFF | 0x1FE0, 0x2001, 0x1C00 |

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/OLM Pin

For applications that do not require SPI mode operation, the CSB pin is tied to AVDD, and the SDIO/OLM pin controls the output lane mode according to Table 13.

For applications where this pin is not used, CSB should be tied to AVDD. When using the one-lane mode, the encode rate should be ≤ 62.5 MSPS to meet the maximum output rate of 1 Gbps.

Table 13. Output Lane Mode Pin Settings

| OLM Pin Voltage | Output Mode |
|-----------------|--|
| AVDD (Default) | Two-lane. 1× frame, 16-bit serial output |
| GND | One-lane. 1× frame, 16-bit serial output |

SCLK/DTP Pin

The SCLK/DTP pin is for use in applications that do not require SPI mode operation. This pin can enable a single digital test pattern if it and the CSB pin are held high during device power-up. When SCLK/DTP is tied to AVDD, the ADC channel outputs shift out the following pattern: 1000 0000 0000 0000. The FCO and DCO function normally while all channels shift out the repeatable test pattern. This pattern allows the user to perform timing alignment adjustments among the FCO, DCO,

and output data. This pin has an internal 10 kΩ resistor to GND. It can be left unconnected.

Table 14. Digital Test Pattern Pin Settings

| Selected DTP | DTP Voltage | Resulting D0±x and D1±x |
|------------------|---------------|-------------------------|
| Normal Operation | 10 kΩ to AGND | Normal operation |
| DTP | AVDD | 1000 0000 0000 0000 |

Additional and custom test patterns can also be observed when commanded from the SPI port. Consult the Memory Map section for information about the options available.

CSB Pin

The CSB pin should be tied to AVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored.

RBIAS Pin

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at the RBIAS pin.

OUTPUT TEST MODES

The output test options are described in Table 11 and controlled by the output test mode bits at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

SERIAL PORT INTERFACE (SPI)

The AD9253 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 15). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

| Pin | Function |
|------|---|
| SCLK | Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes. |
| SDIO | Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame. |
| CSB | Chip select bar. An active low control that gates the read and write cycles. |

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 74 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB-first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

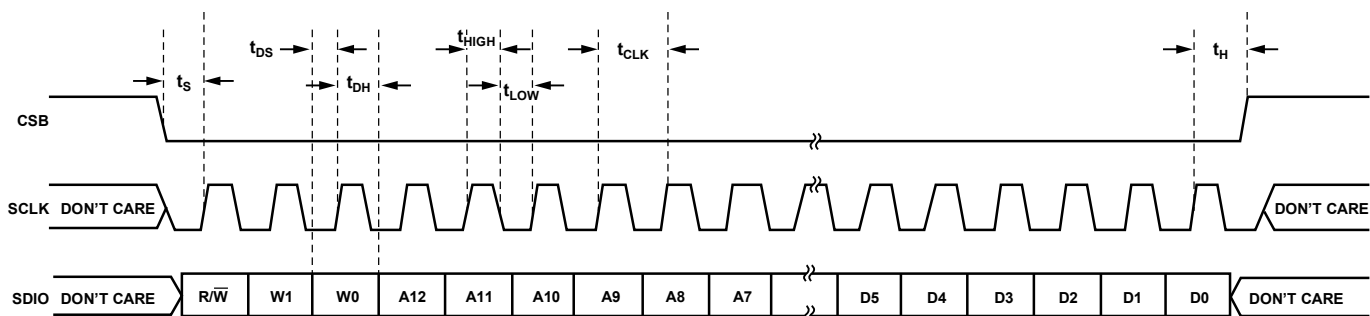


Figure 74. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the [AD9253](#). The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the [AN-812 Application Note, Microcontroller-Based Serial Port Interface \(SPI\) Boot Circuit](#).

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the [AD9253](#) to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. Table 16 describes the strappable functions supported on the [AD9253](#).

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/OLM pin, the SCLK/DTP pin, and the PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, and power-down feature control. In this mode, CSB should be connected to AVDD, which disables the serial port interface.

When the device is in SPI mode, the PDWN pin (if enabled) remains active. For SPI control of power-down, the PDWN pin should be set to its default state.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#). The [AD9253](#) part-specific features are described in detail following Table 17, the external memory map register table.

Table 16. Features Accessible Using the SPI

| Feature Name | Description |
|----------------|--|
| Power Mode | Allows the user to set either power-down mode or standby mode |
| Clock | Allows the user to access the DCS, set the clock divider, set the clock divider phase, and enable the sync |
| Offset | Allows the user to digitally adjust the converter offset |
| Test I/O | Allows the user to set test modes to have known data on output bits |
| Output Mode | Allows the user to set the output mode |
| Output Phase | Allows the user to set the output clock polarity |
| ADC Resolution | Allows for power consumption scaling with respect to sample rate. |

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the device index and transfer registers (Address 0x05 and Address 0xFF); and the global ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x109).

The memory map register table (see Table 17) lists the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x05, the device index register, has a hexadecimal default value of 0x3F. This means that in Address 0x05, Bits[7:6] = 0, and the remaining Bits[5:0] = 1. This setting is the default channel index setting. The default value results in both ADC channels receiving the next write command. For more information on this function and others, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#). This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers are documented in the Memory Map Register Descriptions section.

Open Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x05). If the entire address location is open or not listed in Table 17 (for example, Address 0x13), this address location should not be written.

Default Values

After the AD9253 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 17.

Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

Channel-Specific Registers

Some channel setup functions can be programmed differently for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate data channel bits (A, B, C, or D) and the clock channel DCO bit (Bit 5) and FCO bit (Bit 4) in Register 0x05. If all the bits are set, the subsequent write affects the registers of all channels and the DCO/FCO clock channels. In a read cycle, only one of the channels (A, B, C, or D) should be set to read one of the four registers. If all the bits are set during a SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 17 affect the entire part or the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

The AD9253 uses a 3-wire interface and 16-bit addressing and, therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1. When Bit 5 in Register 0x00 is set high,

the SPI enters a soft reset, where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 17.

| ADDR (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Comments |
|-------------------------------------|------------------------|---|--|--|--------------------|--------------------|----------------|---|---|---------------------|--|
| Chip Configuration Registers | | | | | | | | | | | |
| 0x00 | SPI port configuration | 0 = SDO active | LSB first | Soft reset | 1 = 16-bit address | 1 = 16-bit address | Soft reset | LSB first | 0 = SDO active | 0x18 | The nibbles are mirrored so that LSB-first or MSB-first mode registers correctly. The default for ADCs is 16-bit mode. |
| 0x01 | Chip ID (global) | 8-bit chip ID, Bits[7:0] AD9253 0x8F = quad 14-bit 80 MSPS/105 MSPS/125 MSPS serial LVDS | | | | | | | | 0x8F | Unique chip ID used to differentiate devices; read only. |
| 0x02 | Chip grade (global) | Open | Speed grade ID[6:4] 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS | | | Open | Open | Open | Open | | Unique speed grade ID used to differentiate graded devices; read only. |
| Device Index and Transfer Registers | | | | | | | | | | | |
| 0x05 | Device index | Open | Open | Clock Channel DCO | Clock Channel FCO | Data Channel D | Data Channel C | Data Channel B | Data Channel A | 0x3F | Bits are set to determine which device on chip receives the next write command. The default is all devices on chip. |
| 0xFF | Transfer | Open | Open | Open | Open | Open | Open | Open | Initiate override | 0x00 | Set resolution/sample rate override. |
| Global ADC Function Registers | | | | | | | | | | | |
| 0x08 | Power modes (global) | Open | Open | External power-down pin function 0 = full power-down 1 = standby | Open | Open | Open | Power mode 00 = chip run 01 = full power-down 10 = standby 11 = reset | | 0x00 | Determines various generic modes of chip operation. |
| 0x09 | Clock (global) | Open | Open | Open | Open | Open | Open | Open | Duty cycle stabilize 0 = off 1 = on | 0x01 | Turns duty cycle stabilizer on or off. |

| ADDR (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Comments |
|------------|---|--|--|---|--------------------|---|---|-------|--|--|---|
| 0x0B | Clock divide (global) | Open | Open | Open | Open | Open | Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8 | | | 0x00 | |
| 0x0C | Enhancement control | Open | Open | Open | Open | Open | Chop mode 0 = off 1 = on | Open | Open | 0x00 | Enables/disables chop mode. |
| 0x0D | Test mode (local except for PN sequence resets) | User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once (affects user input test mode only, Bits[3:0] = 1000) | | Reset PN long gen | Reset PN short gen | Output test mode[3:0] (local) 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency | | | | 0x00 | When set, the test data is placed on the output pins in place of normal data. |
| 0x10 | Offset adjust (local) | 8-bit device offset adjustment [7:0] (local) Offset adjust in LSBs from +127 to -128 (twos complement format) | | | | | | | | 0x00 | Device offset trim. |
| 0x14 | Output mode | Open | LVDS-ANSI/ LVDS-IEEE option 0 = LVDS-ANSI 1 = LVDS-IEEE reduced range link (global) see Table 18 | Open | Open | Open | Output invert (local) | Open | Output format 0 = offset binary 1 = twos complement (global) | 0x01 | Configures the outputs and the format of the data. |
| 0x15 | Output adjust | Open | Open | Output driver termination[1:0] 00 = none 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω | | Open | Open | Open | Output drive 0 = 1× drive 1 = 2× drive | 0x00 | Determines LVDS or other output properties. |
| 0x16 | Output phase | Open | Input clock phase adjust[6:4] (value is number of input clock cycles of phase delay) see Table 19 | | | Output clock phase adjust[3:0] (0000 through 1011) see Table 20 | | | 0x03 | On devices that use global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected. | |

| ADDR (Hex) | Parameter Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | Comments |
|------------|-------------------------------------|-----------------------|--|--|-------|----------------|---|--|--------------------|---------------------|--|
| 0x18 | V _{REF} | Open | Open | Open | Open | Open | Internal V _{REF} adjustment digital scheme[2:0] 000 = 1.0 V p-p 001 = 1.14 V p-p 010 = 1.33 V p-p 011 = 1.6 V p-p 100 = 2.0 V p-p | | | 0x04 | Selects and/or adjusts the V _{REF} . |
| 0x19 | USER_PATT1_LSB (global) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User Defined Pattern 1 LSB. |
| 0x1A | USER_PATT1_MSB (global) | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User Defined Pattern 1 MSB. |
| 0x1B | USER_PATT2_LSB (global) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User Defined Pattern 2 LSB. |
| 0x1C | USER_PATT2_MSB (global) | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User Defined Pattern 2 MSB. |
| 0x21 | Serial output data control (global) | LVDS output LSB first | SDR/DDR one-lane/two-lane, bitwise/bytewise[6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise 100 = DDR one-lane | | | Open | Select 2x frame | Serial output number of bits 00 = 16 bits 10 = 12 bits | | 0x30 | Serial stream control. Default causes MSB first and the native bit stream. |
| 0x22 | Serial channel status (local) | Open | Open | Open | Open | Open | Open | Channel output reset | Channel power-down | 0x00 | Used to power down individual sections of a converter. |
| 0x100 | Resolution/sample rate override | Open | Resolution/sample rate override enable | Resolution 01 = 14 bits 10 = 12 bits | | Open | Sample rate 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS | | | 0x00 | Resolution/sample rate override (requires transfer register, 0xFF). |
| 0x101 | User I/O Control 2 | Open | Open | Open | Open | Open | Open | Open | SDIO pull-down | 0x00 | Disables SDIO pull-down. |
| 0x102 | User I/O Control 3 | Open | Open | Open | Open | VCM power-down | Open | Open | Open | 0x00 | VCM control. |
| 0x109 | Sync | Open | Open | Open | Open | Open | Open | Sync next only | Enable sync | 0x00 | |

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

Device Index (Register 0x05)

There are certain features in the map that can be set independently for each channel, whereas other features apply globally to all channels (depending on context) regardless of which are selected. The first four bits in Register 0x05 can be used to select which individual data channels are affected. The output clock channels can be selected in Register 0x05 as well. A smaller subset of the independent feature list can be applied to those devices.

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of this transfer register high initializes the settings in the ADC sample rate override register (Address 0x100).

Power Modes (Register 0x08)

Bits[7:6]—Open

Bit 5—External Power-Down Pin Function

If set, the external PDWN pin initiates power-down mode. If cleared, the external PDWN pin initiates standby mode.

Bits[4:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), all ADC channels are active.

In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled while the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset).

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the AD9253 is a feature that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$ where it can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit chooses LVDS-IEEE (reduced range) option. The default setting is LVDS-ANSI. As described in Table 18, when LVDS-ANSI or LVDS-IEEE reduced range link is selected, the user can select the driver termination. The driver current is automatically selected to give the proper output swing.

Table 18. LVDS-ANSI/LVDS-IEEE Options

| Output Mode, Bit 6 | Output Mode | Output Driver Termination | Output Driver Current |
|--------------------|------------------------------|---------------------------|---|
| 0 | LVDS-ANSI | User selectable | Automatically selected to give proper swing |
| 1 | LVDS-IEEE reduced range link | User selectable | Automatically selected to give proper swing |

Bits[5:3]—Open

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, this bit is set to send the data output in twos complement format. Resetting this bit changes the output mode to offset binary.

Output Adjust (Register 0x15)

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0—Output Drive

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO and DCO outputs only. The default values set the drive to 1× while the drive can be increased to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0. These features cannot be used with the output driver termination select. The termination selection takes precedence over the 2× driver strength on FCO and DCO when both the output driver termination and output drive are selected.

Output Phase (Register 0x16)

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase of the external clock the sampling occurs. This is applicable only when the clock divider is used. It is prohibited to select a value for Bits[6:4] that is greater

than the value of Bits[2:0], Register 0x0B. See Table 19 for more information.

Table 19. Input Clock Phase Adjust Options

| Input Clock Phase Adjust, Bits[6:4] | Number of Input Clock Cycles of Phase Delay |
|-------------------------------------|---|
| 000 (Default) | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

Bits[3:0]—Output Clock Phase Adjust

Table 20. Output Clock Phase Adjust Options

| Output Clock (DCO), Phase Adjust, Bits[3:0] | DCO Phase Adjustment (Degrees Relative to D0±x/D1±x Edge) |
|---|---|
| 0000 | 0 |
| 0001 | 60 |
| 0010 | 120 |
| 0011 (Default) | 180 |
| 0100 | 240 |
| 0101 | 300 |
| 0110 | 360 |
| 0111 | 420 |
| 1000 | 480 |
| 1001 | 540 |
| 1010 | 600 |
| 1011 | 660 |

Table 21. SPI Register Options

| Register 0x21 Contents | Serialization Options Selected | | | DCO Multiplier | Timing Diagram |
|------------------------|-------------------------------------|------------|----------------------|----------------|----------------------------|
| | Serial Output Number of Bits (SONB) | Frame Mode | Serial Data Mode | | |
| 0x30 | 16-bit | 1× | DDR two-lane bitwise | $4 \times f_s$ | Figure 2 (default setting) |
| 0x20 | 16-bit | 1× | DDR two-lane bitwise | $4 \times f_s$ | Figure 2 |
| 0x10 | 16-bit | 1× | SDR two-lane bitwise | $8 \times f_s$ | Figure 2 |
| 0x00 | 16-bit | 1× | SDR two-lane bitwise | $8 \times f_s$ | Figure 2 |
| 0x34 | 16-bit | 2× | DDR two-lane bitwise | $4 \times f_s$ | Figure 4 |
| 0x24 | 16-bit | 2× | DDR two-lane bitwise | $4 \times f_s$ | Figure 4 |
| 0x14 | 16-bit | 2× | SDR two-lane bitwise | $8 \times f_s$ | Figure 4 |
| 0x04 | 16-bit | 2× | SDR two-lane bitwise | $8 \times f_s$ | Figure 4 |
| 0x40 | 16-bit | 1× | DDR one-lane | $8 \times f_s$ | Figure 6 |
| 0x32 | 12-bit | 1× | DDR two-lane bitwise | $3 \times f_s$ | Figure 3 |
| 0x22 | 12-bit | 1× | DDR two-lane bitwise | $3 \times f_s$ | Figure 3 |
| 0x12 | 12-bit | 1× | SDR two-lane bitwise | $6 \times f_s$ | Figure 3 |
| 0x02 | 12-bit | 1× | SDR two-lane bitwise | $6 \times f_s$ | Figure 3 |
| 0x36 | 12-bit | 2× | DDR two-lane bitwise | $3 \times f_s$ | Figure 5 |
| 0x26 | 12-bit | 2× | DDR two-lane bitwise | $3 \times f_s$ | Figure 5 |
| 0x16 | 12-bit | 2× | SDR two-lane bitwise | $6 \times f_s$ | Figure 5 |
| 0x06 | 12-bit | 2× | SDR two-lane bitwise | $6 \times f_s$ | Figure 5 |
| 0x42 | 12-bit | 1× | DDR one-lane | $6 \times f_s$ | Figure 7 |

Serial Output Data Control (Register 0x21)

The serial output data control register is used to program the AD9253 in various output data modes depending upon the data capture solution. Table 21 describes the various serialization options available in the AD9253.

Resolution/Sample Rate Override (Register 0x100)

This register is designed to allow the user to downgrade the device (that is, establish lower power) for applications that do not require full sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is set to 1.

This function does not affect the sample rate; it affects the maximum sample rate capability of the ADC, as well as the resolution.

User I/O Control 2 (Register 0x101)

Bits[7:1]—Open

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—Open

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the [AD9253](#) as a system, it is recommended that the designer become familiar with these guidelines, which describes the special circuit connections and layout requirements that are needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the [AD9253](#), it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the [AD9253](#). With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

CLOCK STABILITY CONSIDERATIONS

When powered on, the [AD9253](#) enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the [AD9253](#) needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, an initialization sequence must be reinvoked after the ADC clock is stable by issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF} , ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. In the case where V_{REF} and/or V_{CM} are supplied by an external source, these, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. The pseudo code sequence for a digital reset is as follows:

```
SPI_Write (0x08, 0x03);   Digital Reset
SPI_Write (0x08, 0x00);   Can be asserted as
                           soon as the next
                           SPI instruction,
                           normal operation
                           resumes after 2.9
                           million sample
                           clock cycles, ADC
                           outputs 0s until
                           the reset is
                           complete.
```

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the [AD9253](#). An exposed continuous copper plane on the PCB should mate to the [AD9253](#) exposed pad, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 75 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the [AN-772 Application Note, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package \(LFCSP\)](#), at www.analog.com.

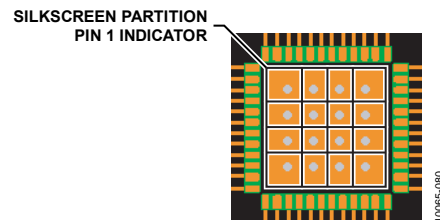


Figure 75. Typical PCB Layout

VCM

The VCM pin should be decoupled to ground with a 0.1 μF capacitor.

REFERENCE DECOUPLING

The VREF pin should be externally decoupled to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

SPI PORT

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the [AD9253](#) to keep these signals from transitioning at the converter inputs during critical sampling periods.

CROSTALK PERFORMANCE

The AD9253 is available in a 48-lead LFCSP package with the input pairs on either corner of the chip. See Figure 9 for the pin configuration. To maximize the crosstalk performance on the board, add grounded filled vias in between the adjacent channels as shown in Figure 76.

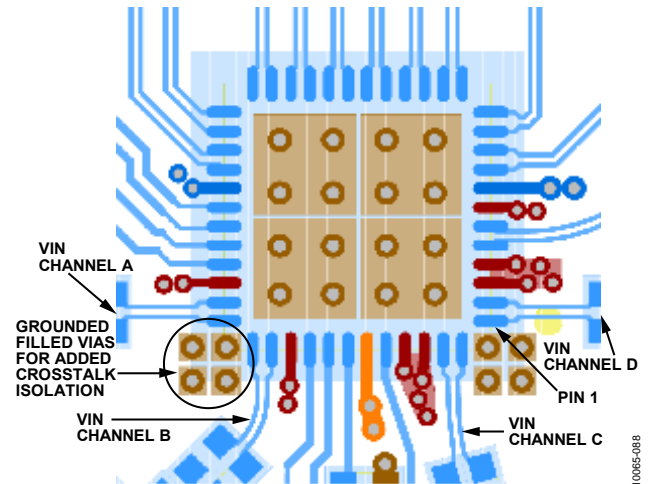
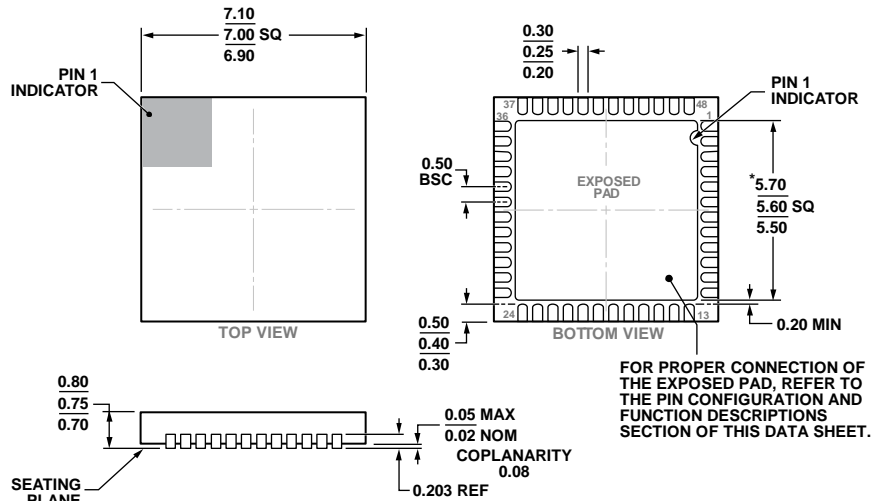


Figure 76. Layout Technique to Maximize Crosstalk Performance

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-WKGD-2 WITH THE EXCEPTION OF THE EXPOSED PAD DIMENSION.

Figure 77. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 7 mm × 7 mm Body, Very Very Thin Quad
 (CP-48-13)
 Dimensions shown in millimeters

10-24-2013-D

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| AD9253BCPZ-80 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253BCPZRL7-80 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253BCPZ-105 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253BCPZRL7-105 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253BCPZ-125 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253BCPZRL7-125 | -40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-48-13 |
| AD9253-125EBZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.