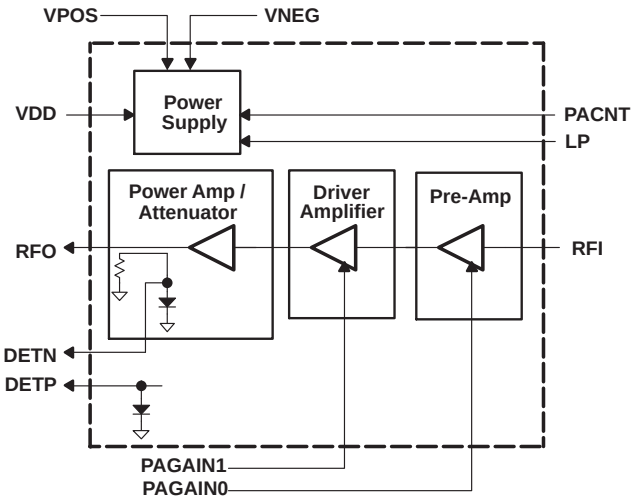
3.3-GHz To 3.8-GHz 1-W Power Amplifier

FEATURES

- **1 W P-1dB Linear, 30-dB Gain Transmitter**
- **Operates Over the 3300-MHz to 3800-MHz Range**
- **Two TTL Controlled, 1-Bit, 16-dB Gain Steps for 32 dB of Total Gain Control**
- **Superior Linearity (+45 dBm IP3) Over the Entire Frequency Range**
- **Auto-Bias Design With PA Enable**
- **Temperature Compensated Directional Coupler Detector**
- **Low Power Bias Mode**
- **Internally Matched 50-Ω Input and Output**



DESCRIPTION

The TRF1223 is a highly integrated linear transmitter / power amplifier (PA) MMIC. The chip has two 16-dB gain steps that provide a total of 32-dB gain control via 1-bit TTL control signals. The chip also integrates a TTL mute function that turns off the amplifiers for power critical or TDD applications. A temperature compensated detector is included for output power monitor or ALC applications. The chip has a P_{1dB} of +30 dBm and a third order intercept of +45 dBm.

The TRF1223 is designed to function as a part of Texas Instruments complete 3.5-GHz chip set. The TRF1223 is the output power amplifier or a driver amplifier for higher power applications. The linear nature of the transmitter makes it ideal for complex modulations schemes such as high order QAM or OFDM.

KEY SPECIFICATIONS

- OP_{1dB} = +30 dBm
- Output IP3 = +45 dBm, Typical
- Gain = 30 dB, Typical
- Gain Flatness over Transmit Band ±2 dB
- Frequency Range = 3300 MHz to 3800 MHz
- ±0.5-dB Detected Output Voltage vs Temperature

BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1.

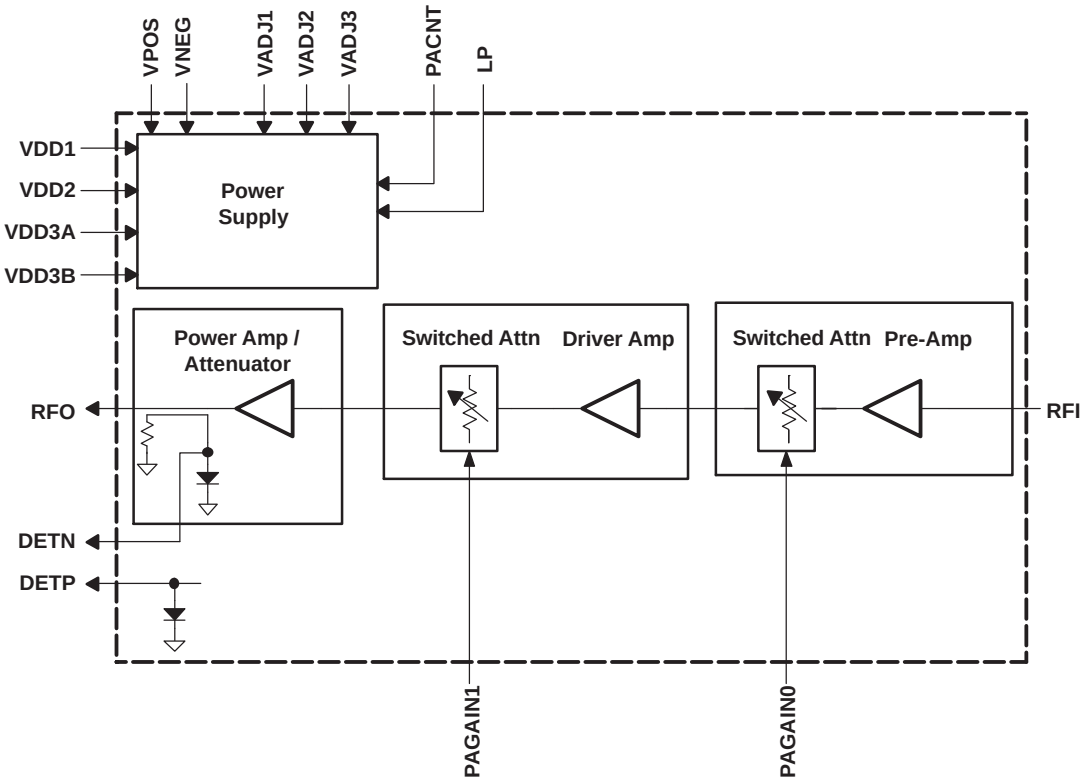


Figure 1. Detailed Block Diagram of TRF1223

ELECTROSTATIC DISCHARGE NOTE

The TRF1223 contain Class 1 devices. The following electrostatic discharge (ESD) precautions are recommended:

- Protective outer garments
- Handling in ESD safeguarded work area
- Transporting in ESD shielded containers
- Frequent monitoring and testing all ESD protection equipment
- Treating the TRF1223 as extremely sensitive to ESD

PINOUT TABLE

Table 1. Pin Out of TRF1223 (1)

PIN #	PIN NAME	I/O	TYPE	DESCRIPTION
1	VDD1	I	Power	Stage 1 dc drain supply power. The dc current through this pin is typically 5% of I_{DD}.
2	VADJ1	I	Analog	No connection required for normal operation. May be used to adjust FET1 bias. DO NOT GROUND THIS PIN OR CONNECT TO ANY OTHER PIN.
3	GND	-	-	Ground
4	RFI	I	Analog	RF input to power amplifier, dc blocked internally
5	RFI	I	Analog	RF input to power amplifier, dc blocked internally
6	VNEG	I	Power	Negative power supply –5 V. Used to set gate voltage. This voltage must be sequenced with V_{DD}. See (1).
7	VPOS	I	Power	Positive power supply for bias circuits. Bias is +5 V. Used to set gate bias and logic input level.

(1) Proper sequencing: In order to avoid permanent damage to the power amplifier, the supply voltages must be sequenced. The proper power up sequence is V_{NEG}, then V_{POS},and then V_{DD}. The proper power down sequence is remove V_{DD}, then V_{POS}, and then V_{NEG}.

Table 1. Pin Out of TRF1223 (continued)

PIN #	PIN NAME	I/O	TYPE	DESCRIPTION
8	PAGAIN0	I	Digital	First 16-dB attenuator gain control. Logic high is high gain and logic low is low gain.
9	PAGAIN1	I	Digital	Second 16-dB gain control. Logic high is high gain and logic low is low gain.
10	VADJ2	I	Analog	No connection required for normal operation. May be used to adjust FET2 bias. DO NOT GROUND THIS PIN OR CONNECT TO ANY OTHER PIN.
11-14	GND	-	-	Ground
15	VADJ3	I	Analog	No connection required for normal operation. May be used to adjust FET3 bias DO NOT GROUND THIS PIN OR CONNECT TO ANY OTHER PIN.
16	LP	I	Digital	Low power mode: Active high. Low power mode is lower dc and P_{OUT} mode.
17	PACNT	I	Digital	Power amplifier enable, High is PA on, logic low is PA off (low current)
18	VDD3B	I	Power	Stage 3 dc-drain supply power. This pin is internally dc connected to pin 23 (VDD3A). Bias must be provided to both pins for optimal performance. The total dc-current through these two pins is typically 70% of IDD.
19	GND	-	-	Ground
20	RFO	O	Analog	RF output, internal dc block
21	RFO	O	Analog	RF output, internal dc block
22	GND	-	-	Ground
23	VDD3A	I	Power	Stage 3 dc-rain supply power. This pin is internally dc connected to pin 18 (VDD3B). Bias must be provided to both pins for optimal performance. The total dc-current through these two pins is typically 70% of I_{DD}.
24	DETP	O	Analog	Detector output, positive. Voltage will be 0.5 V with/without RF output
25	DETN	O	Analog	Detector output, negative. Voltage is 0.5 V with no RF and decreases with increasing RF output power.
26-31	GND	-	-	Ground
32	VDD2	I	Power	Stage 2 dc-drain supply power. The dc current through this pin is typically 25% of I_{DD}.
	Back	-	-	Back of package has a metal base which must be grounded for thermal and RF performance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
VDD	DC supply voltage		0	8	V
VPOS			0	5.5	V
VNEG			-5.5	0	V
I_{DD}	Current consumption			1300	mA
Pin	RF input power			20	dBm
T_j	Junction temperature			175	°C
Pd	Power dissipation			6.5	W
	Digital input pins		-0.3	5.5	
Θ_{jc}	Thermal resistance junction to case(1)			20	°C/W
T_{stg}	Storage temperature		-40	105	°C
T_{op}	Operating temperature	Maximum case temperature derate for PCB thermal resistance	-40	85	°C
	Lead temperature	40 sec maximum		220	°C

(1) Thermal resistance is junction to case assuming thermal pad with 25 thermal vias under package metal base. See the recommended layout Figure 6 and application note RA1005 for more detail.

DC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	VDD supply voltage	-40°C, PACNTRL = High, V_{DD} = 5 V, LP = Low		5	7	V
I_{DD}	VDD supply current high power	25°C, PACNTRL = High, V_{DD} = 5 V, LP = Low		875		mA
				925		
				950		
I_{DD}	VDD supply current low power	85°C, PACNTRL = High, V_{DD} = 5 V, LP = Low		475		mA
				550		
				600		
V_{NEG}	Negative supply voltage	-40°C, PACNTRL = High, V_{DD} = 5 V, LP = High, 25°C	-5.25	-5	-4.75	V
I_{NEG}	Negative supply current	25°C, PACNTRL = High, V_{DD} = 5 V, LP = High, 25°C		15	25	mA
V_{POS}	Positive supply digital voltage	85°C, PACNTRL = High, V_{DD} = 5 V, LP = High, 25°C	4.75	5	5.25	V
I_{POS}	Positive supply digital current			35	50	mA
V_{IH}	Input high voltage		2.5		5	V
V_{IL}	Input low voltage				0.8	V
I_{IH}	Input high current				300	µA
I_{IL}	Input low current				-50	µA

POWER AMPLIFIER CHARACTERISTICS

Unless otherwise stated: V_{DD} = 5 V_S, I_{DD} = 1050 mA, V_{POS} = 5 V, V_{NEG} = -5 V, PAGAIN0 = 1, PAGAIN1 = 1, PACNT = 1, T = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F	Frequency		3300		3800	MHz
G	Gain		26	30	32.5	dB
σ_G	Standard deviation part-to-part gain	At a single frequency, full gain		0.3		dB
G_{HG}	Gain flatness full band	F = 3300 MHz to 3800 MHz		4	6	dB
G_{NB}	Gain flatness / 2 MHz			0.2		dB
OP-1dB	Output power at 1-dB compression	High power bias mode	30	31		dBm
OP-1dB	Output power at 1-dB compression	Low power bias mode		27		dBm
OIP3	Output third order intercept point	High power bias mode	43	48		dBm
OIP3	Output third order intercept point	Low power bias mode		38		dBm
Vdet	Detector voltage output, differential (DETP-DETN)	At POUT = 27 ±0.75 dBm, F = 3300 MHz to 3800 MHz at 25°C		150		mV
	Detector accuracy vs temperature	F = 3550 MHz, -30 to 75°C,		±0.5		dB
	Gain step size 1st step	PAGAIN0 = Low, PAGAIN1 = High	13	16	19	dB
	Gain step size 2nd step	PAGAIN0 = Low, PAGAIN1 = Low	26	32	38	dB
t_{STEP}	Gain step response time			1	5	µs
$P_{ON/OFF}$	On to Off Power ratio	Max gain-to-gain with PACNT = Low	35			dB
NF_{HG}	Noise figure, max gain	PAGAIN0 = High, PAGAIN1 = High		6	7	dB
NF_{LG}	Noise figure min gain	PAGAIN0 = Low, PAGAIN1 = Low			20	dB
S_{12}	Reverse isolation		30			dB
S_{11}	Input return loss	Z = 50 Ω	-10	-12		dB
S_{22}	Output return loss	Z = 50 Ω		-8		dB

TYPICAL PERFORMANCE

All data was taken on parts mounted on PCBs using the pad layout specified in Figure 6 and the filled via process illustrated in Figure 7.

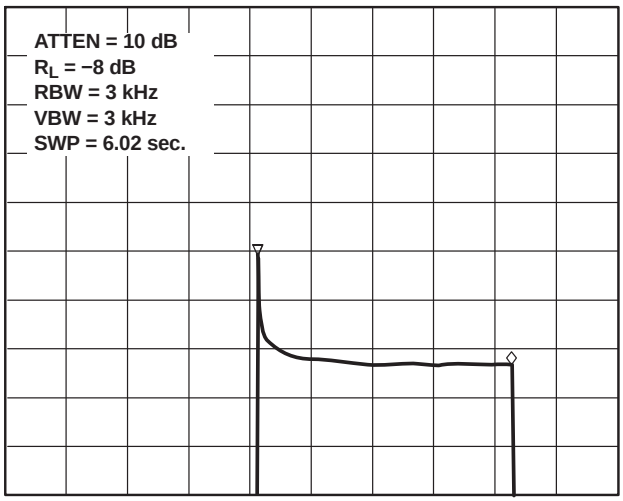


Figure 2. Pulse Droop

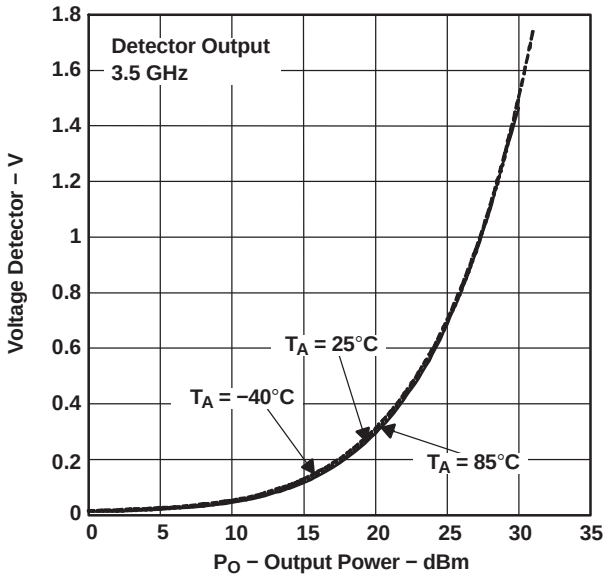


Figure 3. Detector vs Temperature

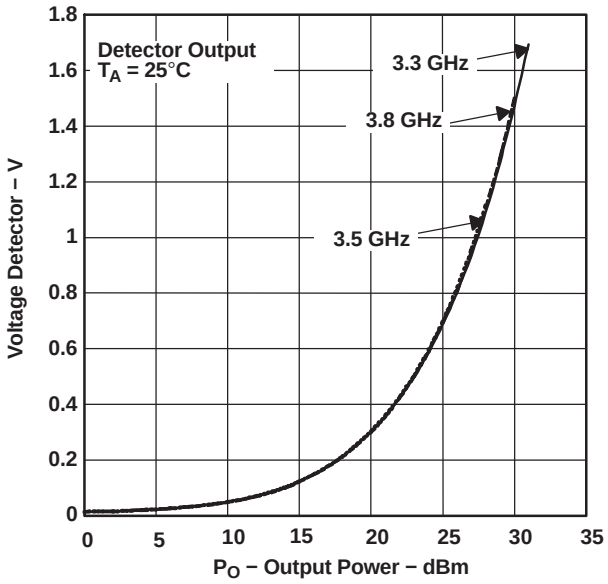


Figure 4. Detector Output vs Frequency

APPLICATION INFORMATION

A typical application schematic is shown in Figure 5.

The recommended PCB layout mask is shown in Figure 6, along with recommendations on the board material in Table 2 and construction in Figure 7.

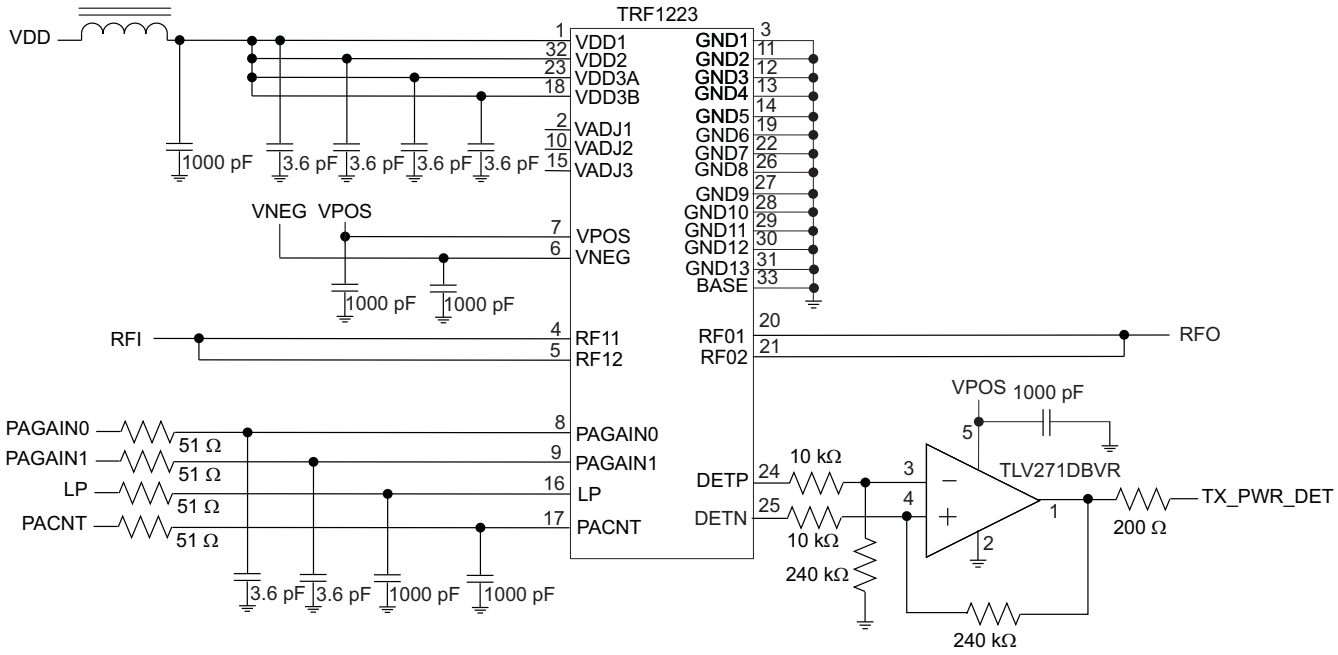
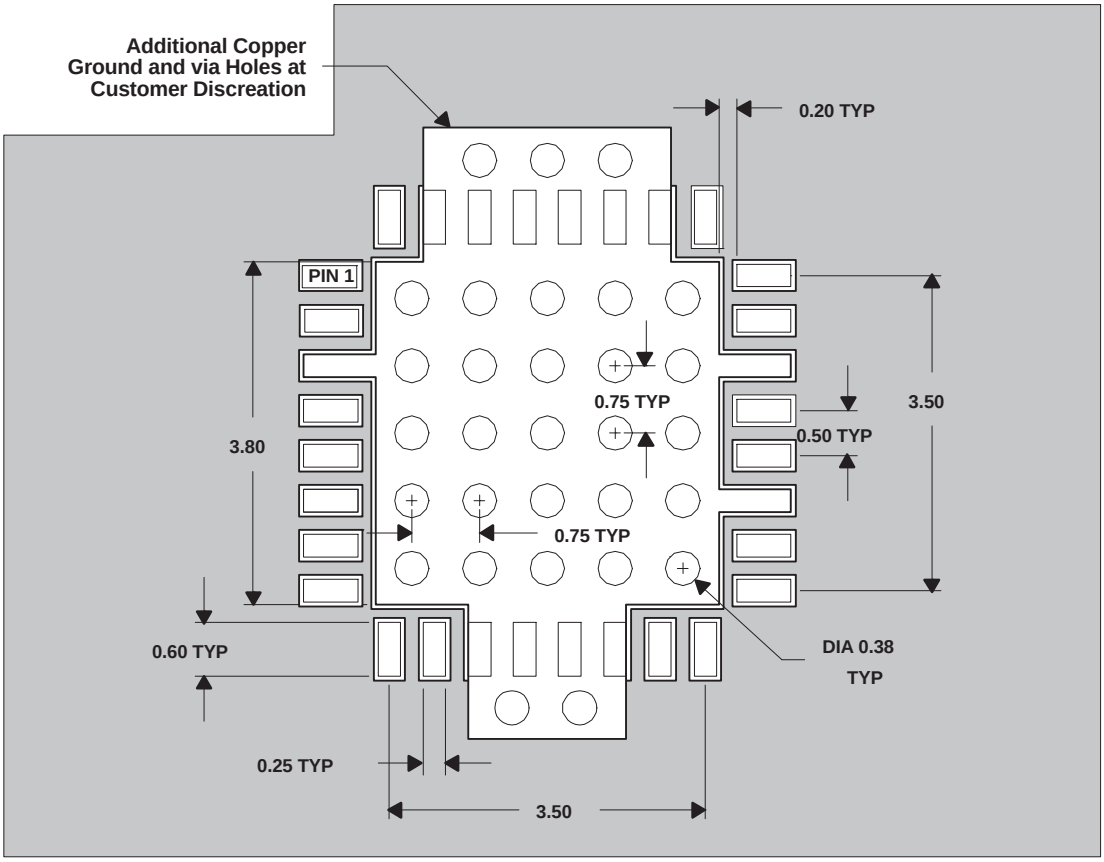


Figure 5. Recommended TRF1223 Application Schematic

Table 2. PCB Recommendations

Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz
Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	0.5 oz
Final Plate	White immersion tin
Final Board Thickness	33 to 37 mil



SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

25 VIA HOLES, MIN, EACH 0.38 mm.
DIMENSIONS in mm

Figure 6. Recommended Pad Layout

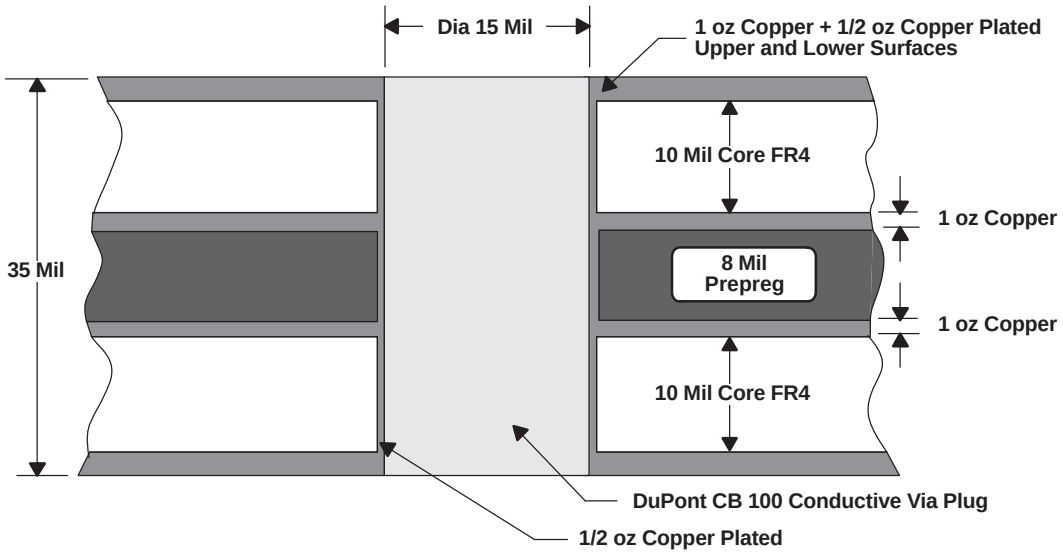


Figure 7. Via Cross Section

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (September 2006) to C Revision	Page
• Changed pin names for pins 22 - 25	2
• Changed Figure 5	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1223IRTMR	OBSOLETE	VQFN	RTM	32		TBD	Call TI	Call TI	-40 to 85	TRF 1223	
TRF1223IRTMT	OBSOLETE	VQFN	RTM	32		TBD	Call TI	Call TI	-40 to 85	TRF 1223	
TRF1223IRTMTG3	OBSOLETE	VQFN	RTM	32		TBD	Call TI	Call TI	-40 to 85	TRF 1223	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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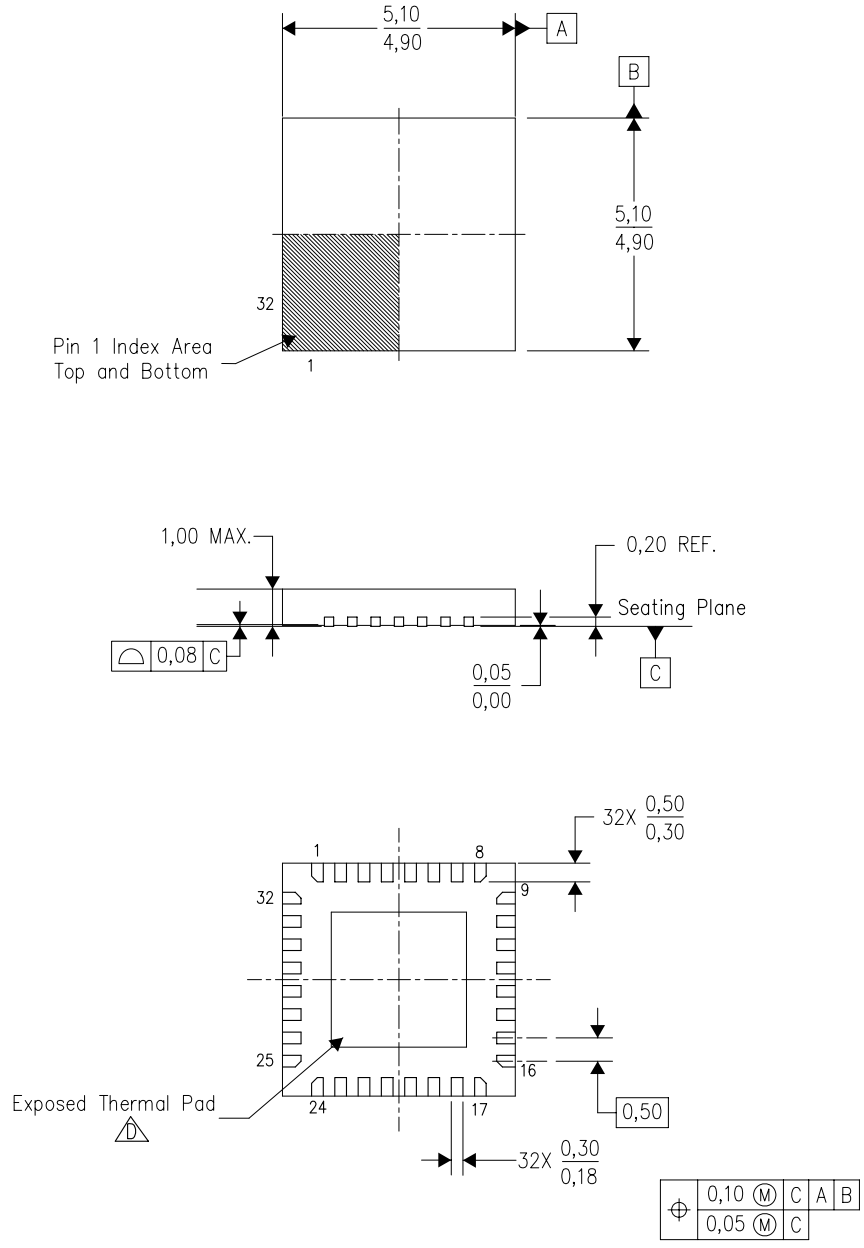
RTM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220.

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