



FDD4141

P-Channel PowerTrench[®] MOSFET

-40V, -50A, 12.3mΩ

Features

- Max $r_{DS(on)}$ = 12.3mΩ at $V_{GS} = -10V$, $I_D = -12.7A$
- Max $r_{DS(on)}$ = 18.0mΩ at $V_{GS} = -4.5V$, $I_D = -10.4A$
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant

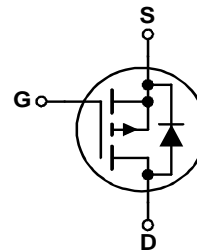
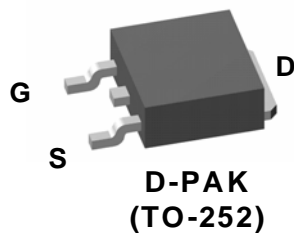


General Description

This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench[®] technology to deliver low $r_{DS(on)}$ and optimized $Bvdss$ capability to offer superior performance benefit in the applications. and optimized switching performance capability reducing power dissipation losses in converter/inverter applications.

Applications

- Inverter
- Power Supplies



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	-50	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$	-58	
	-Continuous $T_A = 25^\circ C$ (Note 1a)	-10.8	
	-Pulsed	-100	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	337	mJ
P_D	Power Dissipation $T_C = 25^\circ C$	69	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4141	FDD4141	D-PAK (TO-252)	13"	16mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-29		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}, V_{GS} = 0\text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		5.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -12.7\text{A}$		10.1	12.3	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -10.4\text{A}$		14.5	18.0	
		$V_{GS} = -10\text{V}, I_D = -12.7\text{A}, T_J = 125^\circ\text{C}$		15.3	18.7	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -12.7\text{A}$		38		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2085	2775	pF
C_{oss}	Output Capacitance			360	480	pF
C_{rss}	Reverse Transfer Capacitance			210	310	pF
R_g	Gate Resistance		$f = 1\text{MHz}$		4.6	Ω

Switching Characteristics

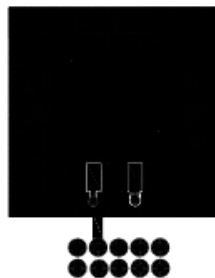
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{V}, I_D = -12.7\text{A}, V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		10	19	ns	
t_r	Rise Time			7	13	ns	
$t_{d(off)}$	Turn-Off Delay Time			38	60	ns	
t_f	Fall Time			15	27	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{V to } -10\text{V}$		36	50	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{V to } -5\text{V}$	$V_{DD} = -20\text{V}, I_D = -12.7\text{A}$		19	27	nC
Q_{gs}	Gate to Source Charge				7		nC
Q_{gd}	Gate to Drain "Miller" Charge				8		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -12.7\text{A}$ (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -12.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$		29	44	ns
Q_{rr}	Reverse Recovery Charge			26	40	nC

Notes:

- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $52^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $100^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

2: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3: Starting $T_J = 25^\circ\text{C}$, $L = 3\text{mH}$, $I_{AS} = 15\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

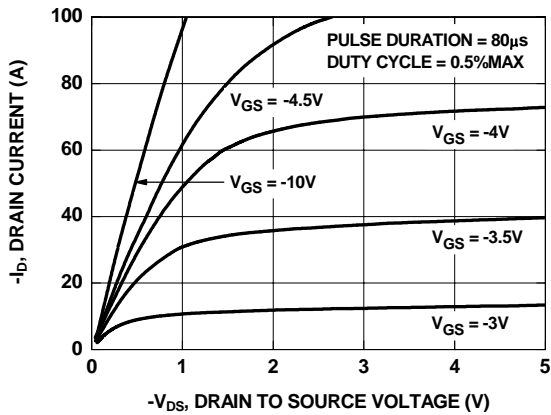


Figure 1. On-Region Characteristics

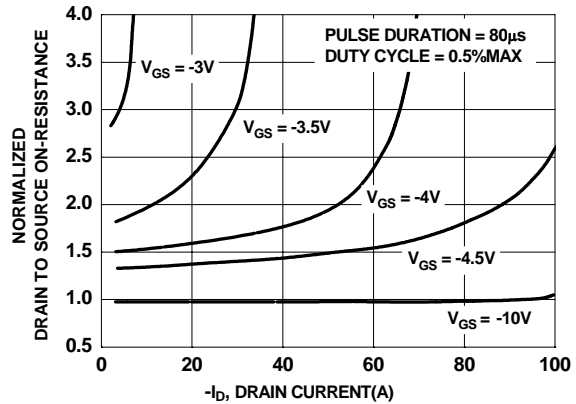


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

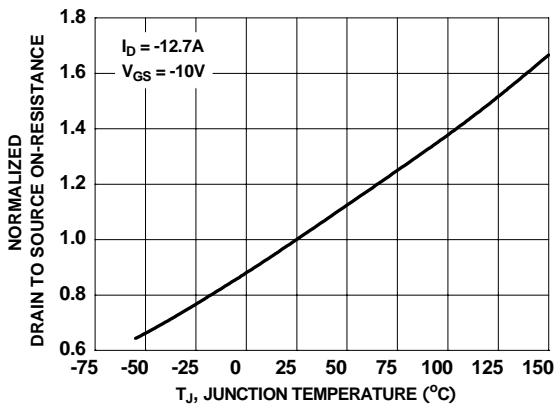


Figure 3. Normalized On-Resistance vs Junction Temperature

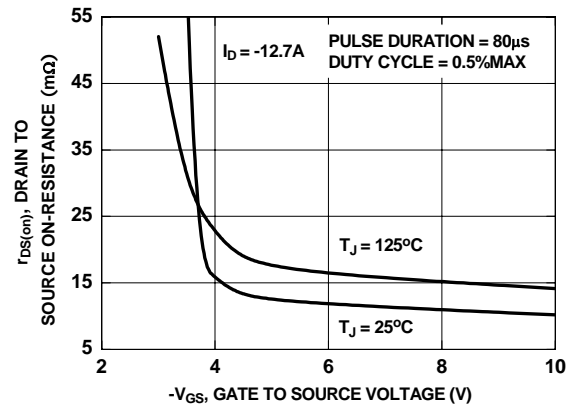


Figure 4. On-Resistance vs Gate to Source Voltage

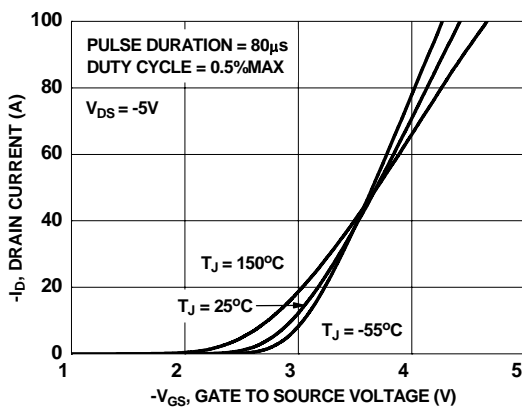


Figure 5. Transfer Characteristics

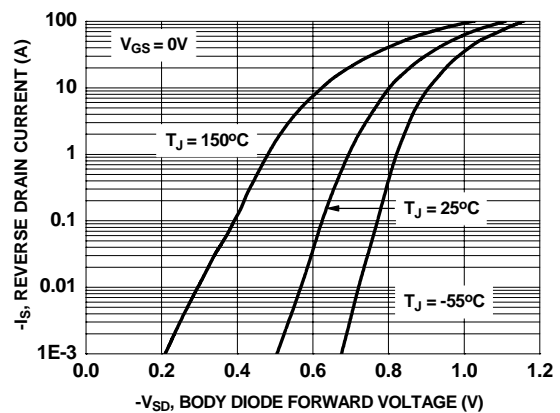


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

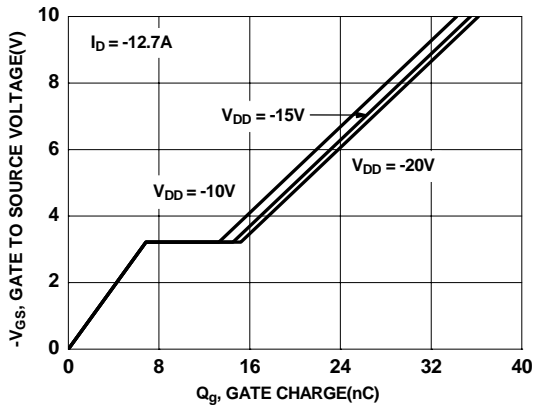


Figure 7. Gate Charge Characteristics

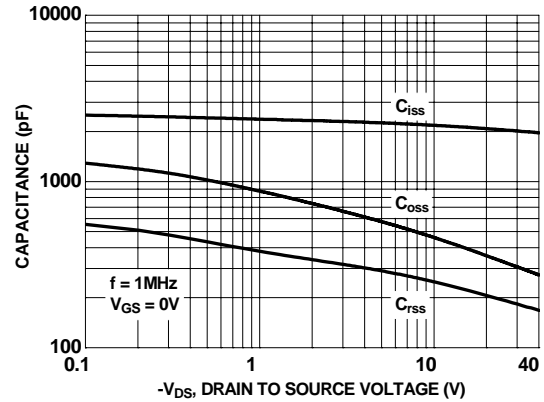


Figure 8. Capacitance vs Drain to Source Voltage

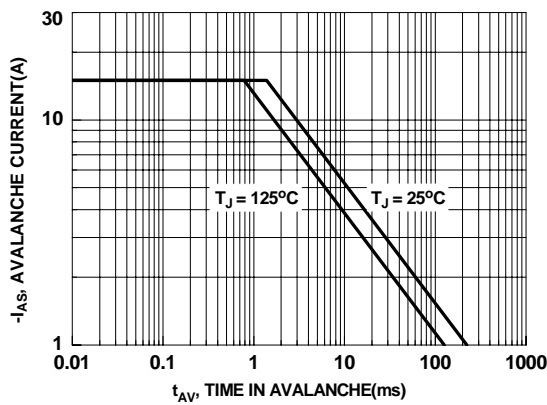


Figure 9. Unclamped Inductive Switching Capability

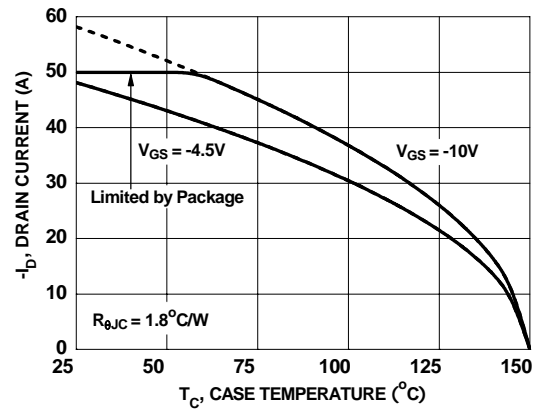


Figure 10. Maximum Continuous Drain Current vs Case Temperature

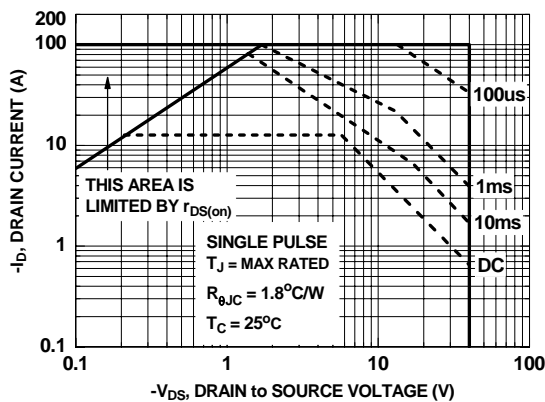


Figure 11. Forward Bias Safe Operating Area

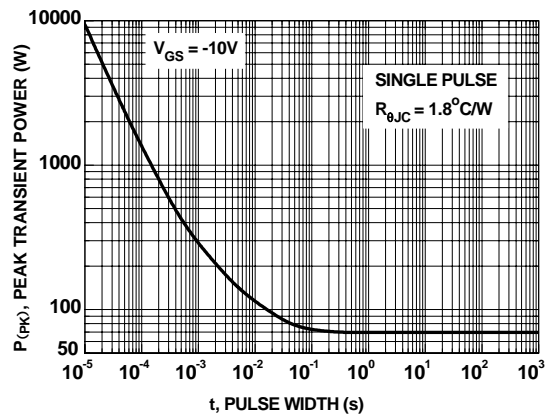
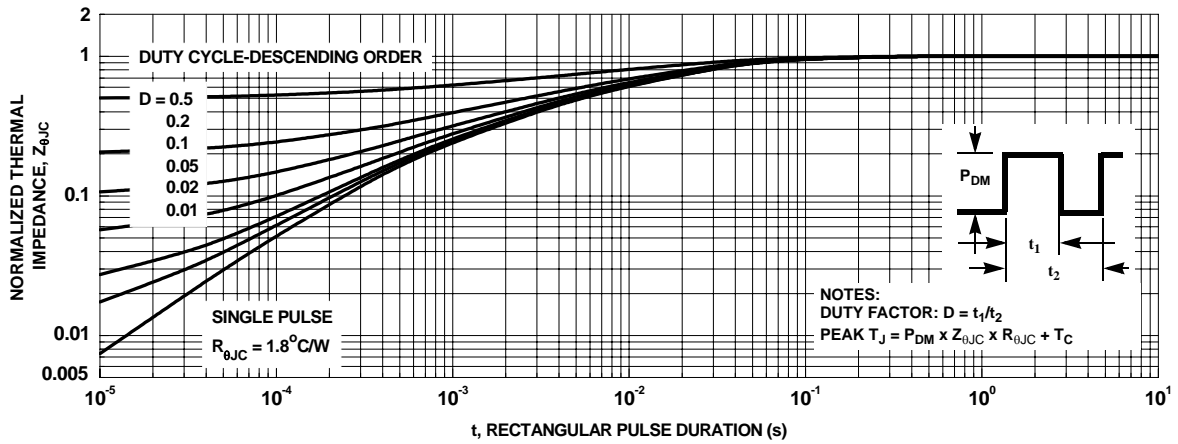
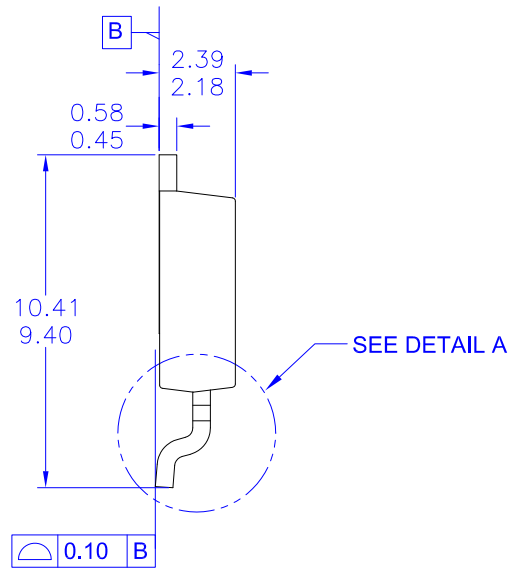
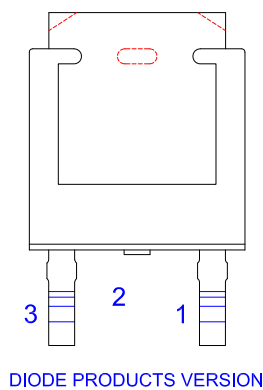
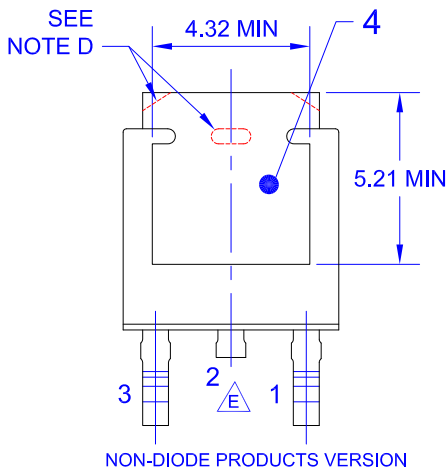
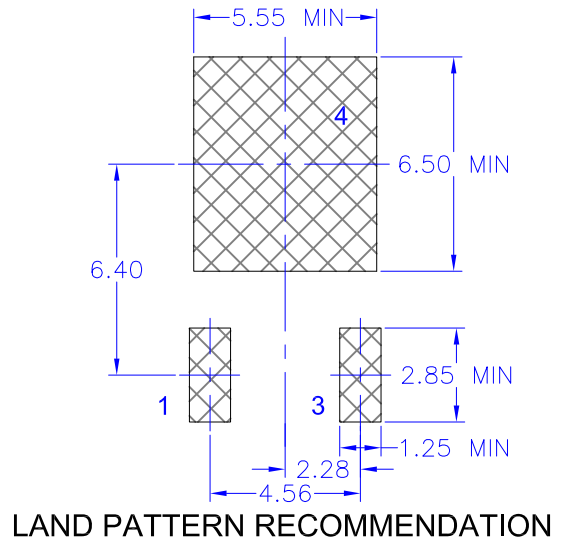
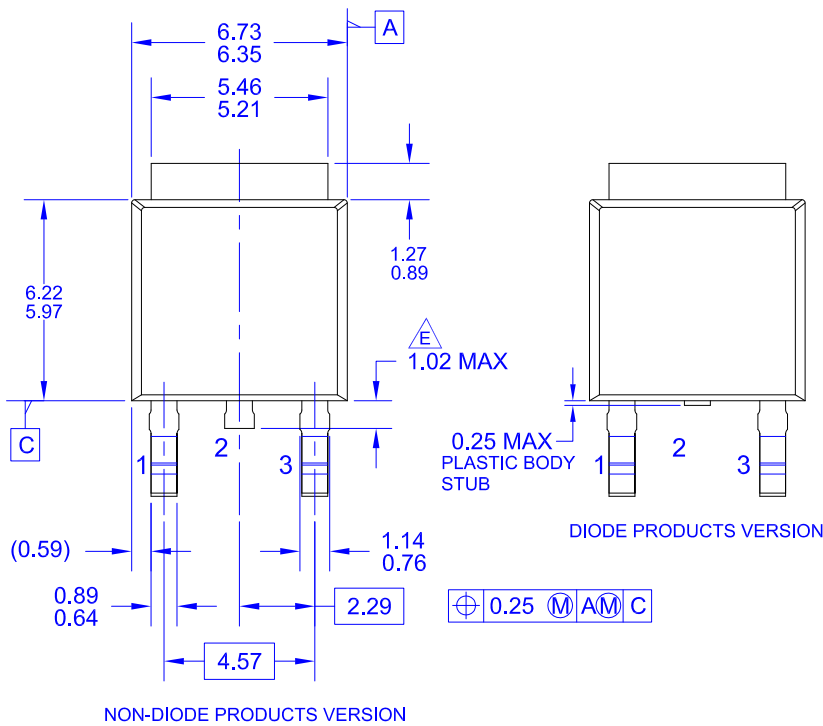


Figure 12. Single Pulse Maximum Power Dissipation

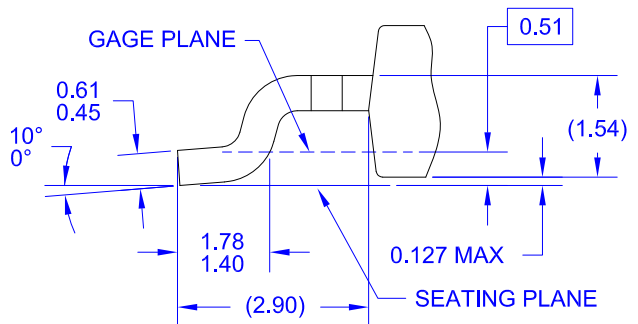
Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



DETAIL A
(ROTATED -90°)
SCALE: 12X





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I77