LP8861-Q1 Low-EMI, High-Performance Four-Channel LED Driver for Automotive Lighting

1 Features

- Qualified for Automotive Applications
- AECQ100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
- Input Voltage Operating Range 4.5 V to 40 V
- Four High-Precision Current Sinks
  - Current Matching 1% (typical)
  - LED String Current up to 100 mA/Channel
  - Dimming Ratio 10 000:1 at 200 Hz
- Integrated Boost/SEPIC for LED String Power
  - Output Voltage up to 45 V
  - Switching Frequency 300 kHz to 2.2 MHz
  - Boost/SEPIC Synchronization Input
  - Spread Spectrum
- Power-Line FET Control for Inrush Current Protection and Standby Energy Saving
- Extensive Fault Detection and Tolerance Features
  - Fault Output
  - Input Voltage OVP, UVLO, and OCP
  - Open and Shorted LED Fault Detection
  - Automatic LED Current Reduction With External Temperature Sensor
  - Thermal Shutdown
- Minimum Number of External Components

2 Applications

Automotive Infotainment, Instrument Clusters, and Backlighting Systems

3 Description

The LP8861-Q1 is an automotive high-efficiency, low-EMI, easy-to-use LED driver with integrated boost/SEPIC converter. It has four high-precision current sinks that can provide high dimming ratio brightness control with a PWM input signal.

The boost/SEPIC converter has adaptive output voltage control based on the LED current sink headroom voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions. Boost/SEPIC controller supports spread spectrum for switching frequency and an external synchronization with dedicated pin. The high switching frequency allows the LP8861-Q1 to avoid disturbance for AM radio band.

The LP8861-Q1 has option to drive an external p-FET to disconnect the input supply from the system in the event of a fault and reduce inrush current and standby power consumption. The device has ability to reduce LED current based on temperature measured with external NTC sensor to protect LED from overheating and extend LED life time.

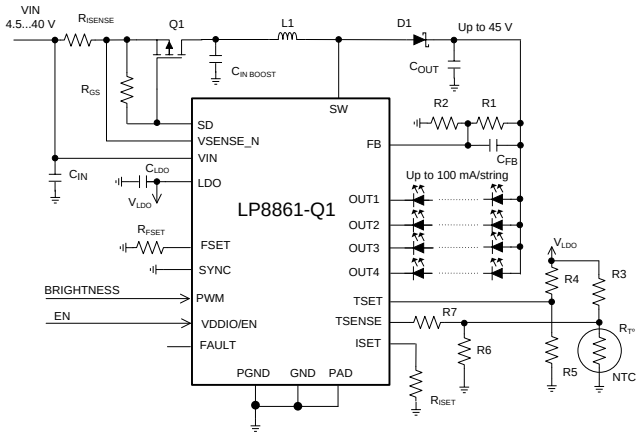
The input voltage range for the LP8861-Q1 is from 4.5 V to 40 V to support automotive stop/start and load dump condition. The device supports PWM brightness dimming ratio 10 000:1 for input PWM frequency
200 Hz. The LP8861-Q1 integrates extensive fault detection and protection features.

Device Information(1)

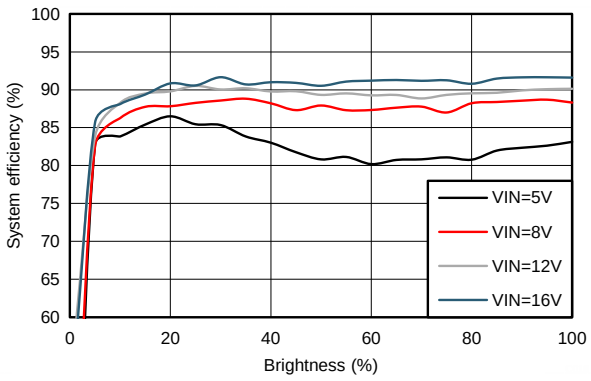
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8861-Q1	TSSOP (20)	6.50 × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



System Efficiency



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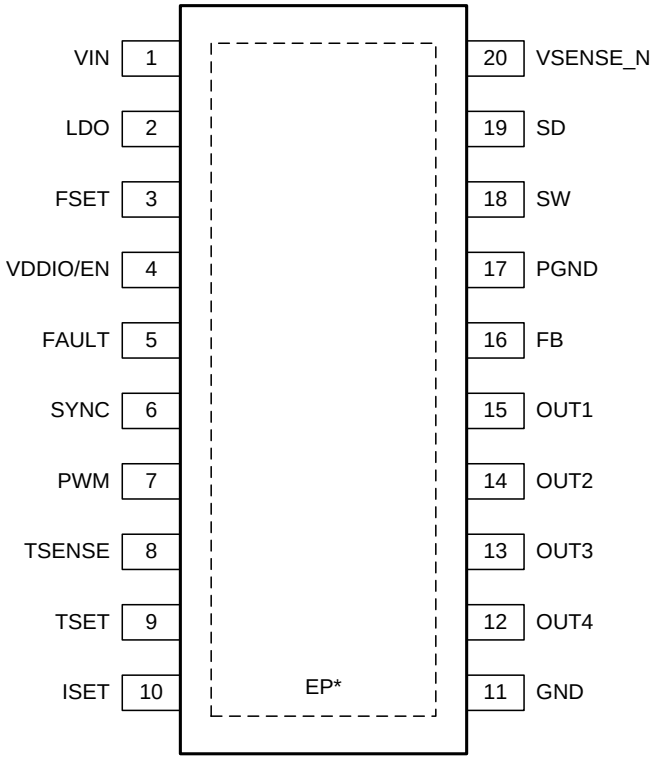
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2015) to Revision A	Page
• Changed maximum T_{stg} from 160°C to 150°C	5
• Added last 2 sentences to end of *Internal LDO* subsection	15
• Changed Equation 3	15
• Changed Figure 29 to update VIN and VSENSE_N pin connections; removed RISENSE row from sub-section *8.2.2.1 Design Requirements*	27

5 Pin Configuration and Functions

PWP Package
20-Pin TSSOP with Exposed Thermal Pad
Top View



*EXPOSED PAD

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	VIN	P	Input power pin as well as the positive input for an optional current sense resistor.
2	LDO	A	Output of internal LDO; connect a 1-µF decoupling capacitor between this pin and noise-free ground.
3	FSET	A	Boost/SEPIC switching frequency setting resistor.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins
5	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
6	SYNC	I	Input for synchronizing boost/SEPIC. In synchronization is not used, connect this pin to GND to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	TSENSE	A	Input for NTC bridge. If unused, the pin may be left floating.
9	TSET	A	Input for NTC bridge. This pin must be connected to GND if not used.
10	ISET	A	LED current setting resistor
11	GND	G	Ground.
12	OUT4	A	Current sink output. This pin must be connected to GND if not used.
13	OUT3	A	Current sink output. This pin must be connected to GND if not used.
14	OUT2	A	Current sink output. This pin must be connected to GND if not used.
15	OUT1	A	Current sink output. This pin must be connected to GND if not used.
16	FB	A	Boost/SEPIC feedback input.
17	PGND	G	Boost/SEPIC power ground.
18	SW	A	Boost/SEPIC switch pin.
19	SD	A	Power-line FET control. If unused, the pin may be left floating.
20	VSENSE_N	A	Input current sense pin. Connect to VIN pin when optional input current sense resistor is not used.

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage on pins	VIN, VSENSE_N, SD, SW, FB	–0.3	50	V
	OUT1…OUT4	–0.3	45	
	LDO, SYNC, FSET, ISET, TSENSE, TSET, PWM, VDDIO/EN, FAULT	–0.3	5.5	
Continuous power dissipation(3)		Internally Limited		
Ambient temperature range, T_A(4)		–40	125	ºC
Junction temperature range, T_J(4)		–40	150	ºC
Maximum lead temperature (soldering)			See(5)	ºC
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 150°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.
(5) For detailed soldering specifications and information, refer to the *PowerPAD™ Thermally Enhanced Package Application Note* (SLMA002).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Other pins	±500	
			Corner pins (1,10,11,20)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

Over operating free-air temperature range (unless otherwise noted) .

		MIN	MAX	UNIT
Voltage on pins	VIN	4.5	45	V
	VSENSE_N, SD, SW	0	45	
	OUT1…OUT4	0	40	
	FB, FSET, LDO, ISET, TSENSE, TSET, VDDIO/EN, FAULT	0	5.25	
	SYNC, PWM	0	VDDIO/EN	

(1) All voltages are with respect to the potential at the GND pins.

6.4 Thermal Information

THERMAL METRIC(1)		LP8861-Q1 PWP (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	44.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics(1)(2)

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Standby supply current	Device disabled, $V_{VDDIO/EN}$ = 0 V, V_{IN} = 12 V		4.5	20	µA
	Active supply current	V_{IN} = 12 V, V_{BOOST}=26 V, output current 80 mA/channel, f_{SW}= 300 kHz		5	12	mA
V_{POR_R}	Power-on reset rising threshold	LDO pin voltage. Output of the internal LDO or an external supply input (V_{DD}).			2.7	V
V_{POR_F}	Power-on reset falling threshold	LDO pin voltage. Output of the internal LDO or an external supply input (V_{DD}).	1.5			V
T_{TSD}	Thermal shutdown threshold		150	165	175	°C
T_{TSD_THR}	Thermal shutdown hysteresis			20		°C

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis.

6.6 Internal LDO Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO}	Output voltage	V_{IN} = 12 V	4.15	4.3	4.45	V
V_{DR}	Dropout voltage	External current load 5mA	120	220	430	mV
I_{SHORT}	Short circuit current			50		mA
I_{EXT_MAX}	Maximum current for external load			5		mA

6.7 Protection Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	VIN OVP threshold voltage		41	42	44	V
I_{OCP}	VIN OCP current	R_{SENSE} = 50 mΩ	2.7	3.2	3.7	A
V_{UVLO}	VIN UVLO			4.0		V
V_{UVLO_HYST}	VIN UVLO hysteresis			100		mV
	LED short detection threshold		5.6	6	7	V

6.8 Power Line FET Control Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSENSE_N pin leakage current	V_{VSENSE_N} = 45 V		0.1	3	µA
SD leakage current	V_{SD} = 45 V		0.1	3	µA
SD pulldown current		185	230	283	µA

6.9 Current Sinks Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT4, V_{OUTx} = 45 V		0.1	5	µA
I_{MAX}	Maximum current	OUT1 to OUT4		100		mA
I_{OUT}	Output current accuracy	I_{OUT} = 100 mA	−5%		5%	
I_{MATCH}	Output current matching (1)	I_{OUT} = 100 mA, PWM duty =100%		1%	3.5%	
V_{SAT}	Saturation voltage (2)	I_{OUT} = 100 mA, V_{LDO} = 4.3 V		0.4	0.7	V

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT4), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

6.10 PWM Brightness Control Electrical Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	Recommended PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time	I_{OUT} = 100 mA. No external load from LDO			0.5	µs

6.11 Boost/SEPIC Converter Characteristics

T_J = −40°C to +125°C (unless otherwise noted).
Unless otherwise specified: V_{IN} = 12 V, $V_{VDDIO/EN}$ = 3.3 V, L = 22 µH, C_{IN} = 2 × 10-µF ceramic and 33-µF electrolytic, C_{OUT} = 2 × 10-µF ceramic and 33-µF electrolytic, D = NRVB460MFS, f_{SW} = 300 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		10		45	V
f_{SW_MIN}	Minimum switching frequency (central frequency if spread spectrum is enabled)	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency (central frequency if spread spectrum is enabled)			2200		kHz
V_{OUT}/V_{IN}	Conversion ratio				10	
T_{OFF}	Minimum switch OFF time	f_{SW} ≥ 1.15 MHz			55	ns
I_{SW_MAX}	SW current limit		1.8	2	2.2	A
R_{DSon}	FET R_{DSon}	Pin-to-pin		240	400	mΩ
f_{SYNC}	External SYNC frequency		300		2200	kHz
$t_{SYNC\_ON\_MIN}$	External SYNC minimum on time			150		ns
$t_{SYNC\_OFF\_MIN}$	External SYNC minimum off time			150		ns

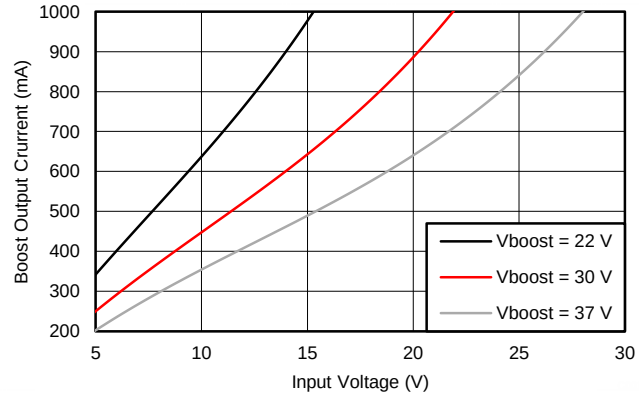
6.12 Logic Interface Characteristics

T_J = −40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			V
I_I	Input current		−1	5	30	µA
LOGIC INPUTS SYNC, PWM						
V_{IL}	Input low level				$0.2 \times V_{VDDIO/EN}$	V
V_{IH}	Input high level		$0.8 \times V_{VDDIO/EN}$			
I_I	Input current		−1		1	µA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5 V			1	µA

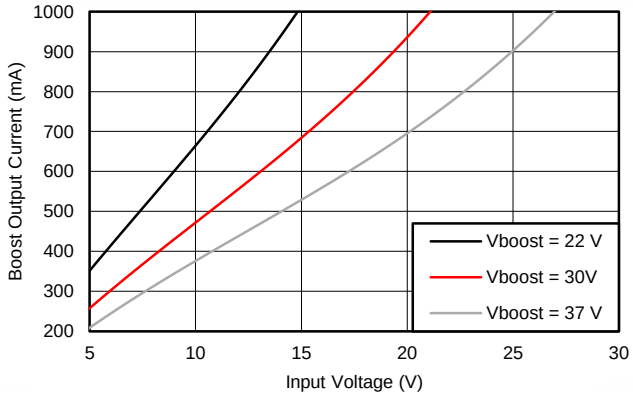
6.13 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, T = 25°C.



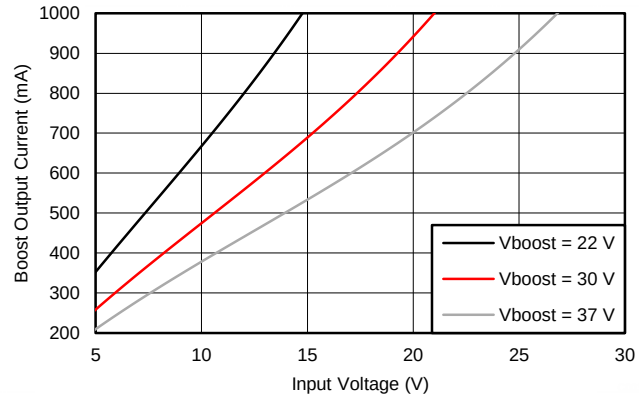
f_{SW} = 300 kHz L = 33 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF + 2 × 10 µF (ceramic)

Figure 1. Maximum Boost Output Current



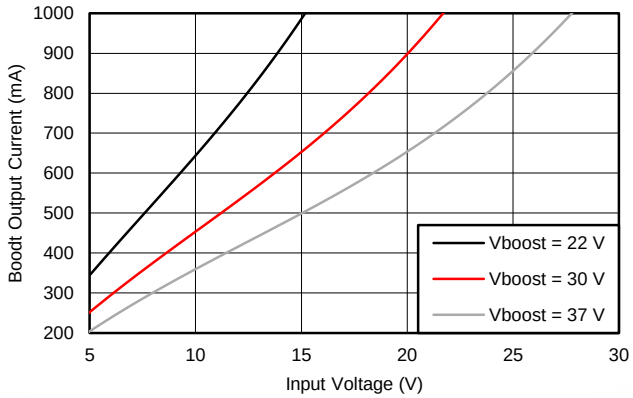
f_{SW} = 800 kHz L = 15 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 2. Maximum Boost Output Current



f_{SW} = 1.5 MHz L = 8.2 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 3. Maximum Boost Output Current



f_{SW} = 2.2 MHz L = 4.7 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 4. Maximum Boost Output Current

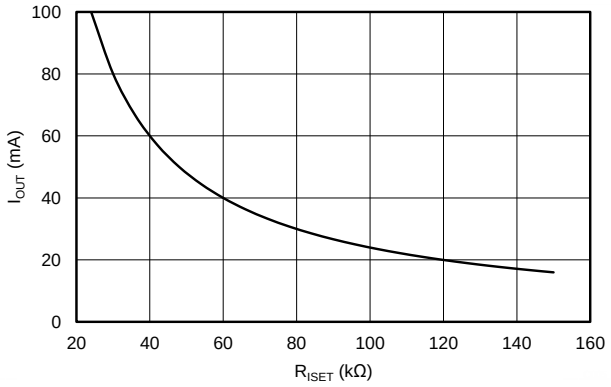


Figure 5. LED Current vs R_{ISET}

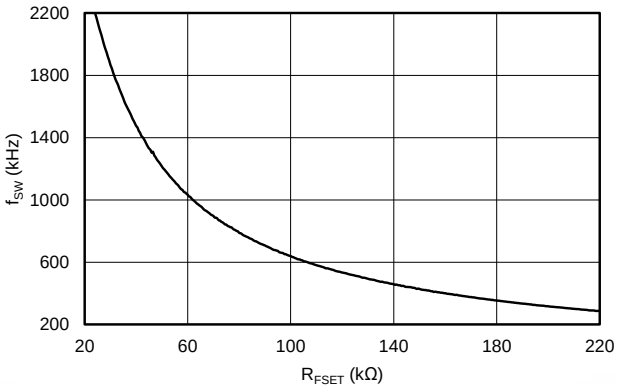


Figure 6. Boost Switching Frequency f_{SW} vs R_{FSET}

Typical Characteristics (continued)

Unless otherwise specified: D = NRVB460MFS, T = 25°C.

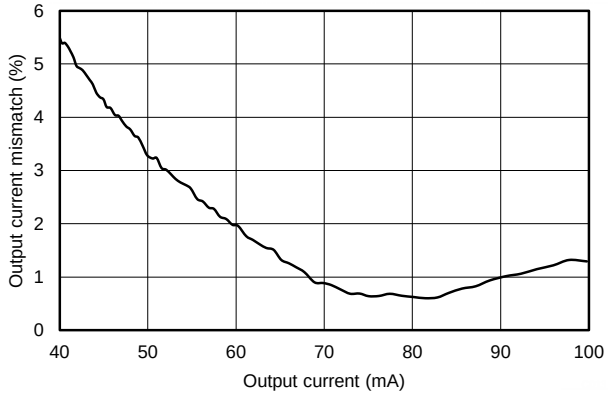


Figure 7. LED Current Sink Matching

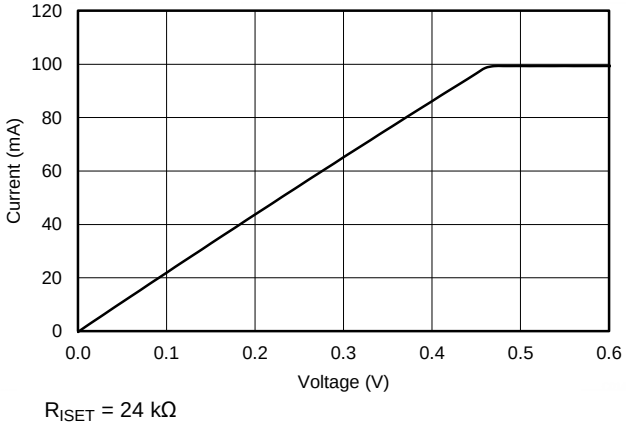


Figure 8. LED Current Sink Saturation Voltage

7 Detailed Description

7.1 Overview

The LP8861-Q1 is a highly integrated LED driver for automotive infotainment, lighting systems, and medium-sized LCD backlight applications. It includes a boost/SEPIC converter with an integrated FET, an internal LDO, and four LED current sinks. A VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the boost/SEPIC regulator is set by a resistor connected to the FSET pin. The maximum voltage is set by a resistive divider connected to the FB pin. For the best efficiency the voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LED output voltage in real time. For EMI reduction and control two optional features are available:

- Spread spectrum, which reduces EMI noise spikes at the switching frequency and its harmonic frequencies.
- Boost/SEPIC can be synchronized to an external clock frequency connected to the SYNC pin.

The four constant current sinks for driving the LEDs provide current up to 100 mA per sink and can be tied together to get a higher current. Value for the current value is set with a resistor connected to the ISET pin. Current sinks that are not used must be connected to the ground. Grounded current sinks are disabled and excluded from the adaptive voltage and open/short LED fault detection loop.

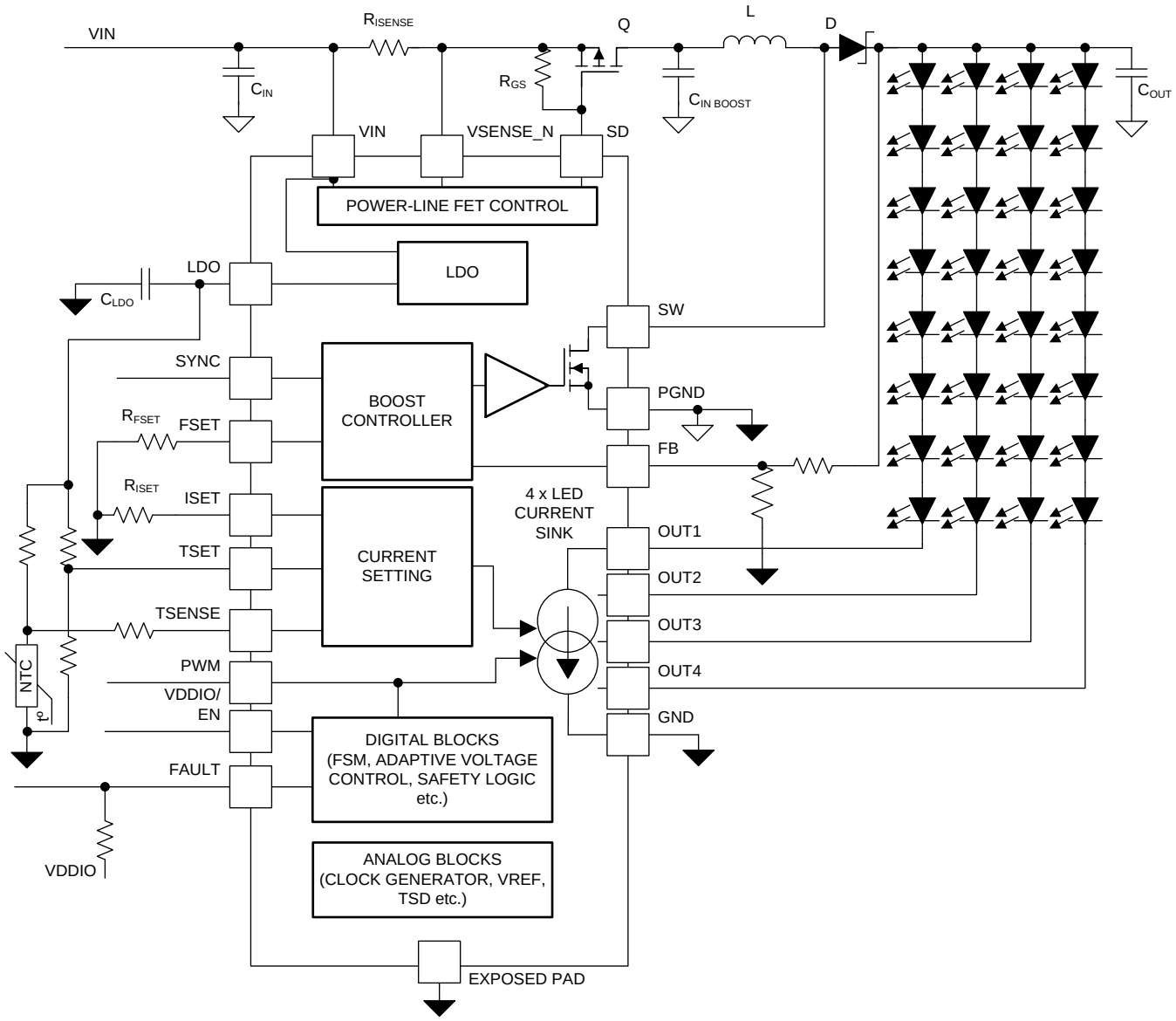
Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM follows the input PWM so the output frequency is equal to the input frequency.

The LP8861-Q1 has extensive fault detection features:

- Open-string and shorted LED detections
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- V_{IN} input-overvoltage protection
  - Threshold sensing from VIN pin
- V_{IN} input undervoltage protection
  - Threshold sensing from VIN pin
- V_{IN} input overcurrent protection
  - Threshold sensing across R_{ISENSE} resistor
- Thermal shutdown in case of die overtemperature
- LED thermal protection with a external NTC (optional feature)

Fault condition is indicated with the FAULT output pin. Additionally, the LP8861-Q1 supports control for an optional power-line FET allowing further protection in boost/SEPIC overcurrent state by disconnecting the device from power-line in fault condition. With the power-line FET control it is possible to protect device, boost components, and LEDs in case of shorted V_{BOOST} and too-high V_{IN} voltage. Power-line FET control also features soft-start which reduces the peak current from the power line during start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Boost/SEPIC Converter

The LP8861-Q1 boost/SEPIC DC-DC converter generates supply voltage for the LEDs. The maximum output voltage $V_{MAX\ BOOST}$ is defined by an external resistive divider (R1, R2).

Maximum voltage must be chosen based on the maximum voltage required for LED strings. Recommended $V_{MAX\ BOOST}$ is about 30% higher than maximum LED string voltage. Initial DC-DC voltage is about 88% of $V_{MAX\ BOOST}$. DC-DC output voltage is adjusted automatically based on LED current sink headroom voltage. Maximum voltage can be calculated with Equation 1:

$$V_{MAX\,BOOST} = \left(\frac{V_{BG}}{R2} + 0.0387\right) \times R1 + V_{BG} \quad (1)$$

where

- V_{BG} = 1.2 V
- R2 recommended value is 130 kΩ
- Resistors values are in kΩ

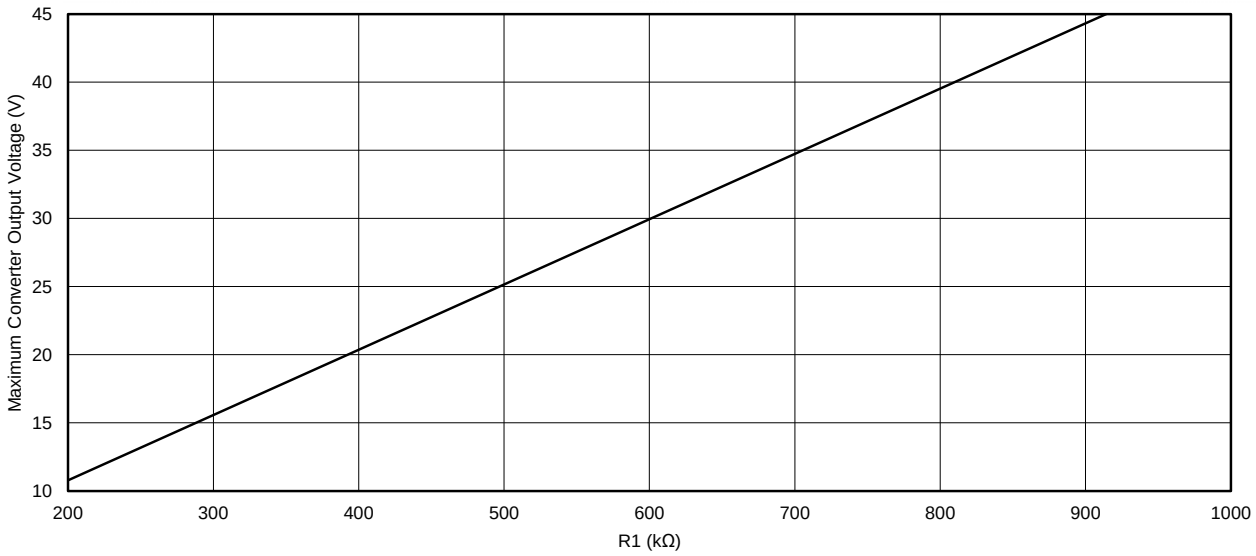


Figure 9. Maximum Converter Output Voltage vs R1 Resistance

The converter is a current mode DC-DC converter, where the inductor current is measured and controlled with the feedback. Switching frequency is adjustable between 300 kHz and 2.2 MHz with R_{FSET} resistor as Equation 2 in Equation 2:

$$f_{SW} = 67600 / (R_{FSET} + 6.4) \quad (2)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, kΩ

In most cases lower frequency has higher system efficiency. Boost parameters are chosen automatically during start-up according to the selected switching frequency (see Table 2). In boost mode a 15-pF capacitor C_{FB} must be placed across resistor R1 when operating in 300 kHz ... 500 kHz range (see Figure 24). When operating in the 1.8-MHz...2.2-MHz range, C_{FB} = 4.7 pF (see Figure 29).

Feature Description (continued)

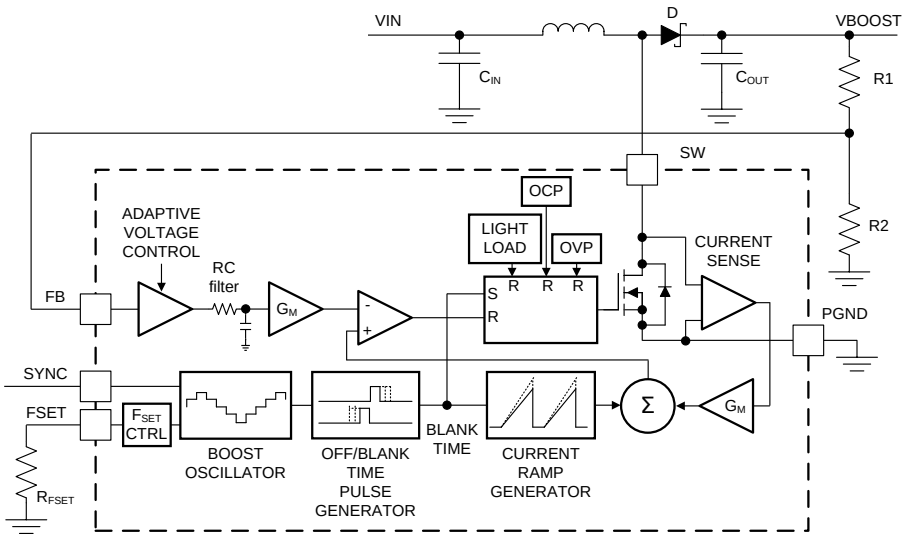


Figure 10. Boost Block Diagram

Boost clock can be driven by an external SYNC signal between 300 kHz…2.2 MHz. If the external synchronization input disappears, boost continues operation at the frequency defined by R_{FSET} resistor. When external frequency disappears and SYNC pin level is low, boost continues operation without spread spectrum immediately. If SYNC remains high, boost continues switching with spread spectrum enabled after 256 µs.

External SYNC frequency must be 1.2…1.5 times higher than the frequency defined by the R_{FSET} resistor. Minimum frequency setting with R_{FSET} is 250 kHz to support minimum switching frequency with external clock frequency 300 kHz.

The optional spread-spectrum feature (±3% from central frequency, 1-kHz modulation frequency) reduces EMI noise spikes at the switching frequency and its harmonic frequencies. When external synchronization is used, spread spectrum is not available.

Table 1. Boost Synchronization Mode

SYNC PIN STATUS	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300...2200 kHz frequency	Spread spectrum disabled, external synchronization mode

Table 2. Boost Parameters(1)

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (µH)	TYPICAL BOOST INPUT AND OUTPUT CAPACITORS (µF)	MIN SWITCH OFF TIME (ns)(2)	BLANK TIME (ns)	CURRENT RAMP (A/s)	CURRENT RAMP DELAY (ns)
1	300...480	33	2 × 10 (cer.) + 33 (electr.)	150	95	24	550
2	480...1150	15	10 (cer.) +33 (electr.)	60	95	43	300
3	1150...1650	10	3 × 10 (cer.)	40	95	79	0
4	1650...2200	4.7	3 × 10 (cer.)	40	70	145	0

(1) Parameters are for reference only.
(2) Due to current sensing comparator delay the actual minimum off time is 6ns (typ.) longer than in the table.

Boost SW pin DC current is limited to 2 A (typical). To support warm start transient condition the current limit is automatically increased to 2.5 A for a short period of 1.5 seconds when a 2-A limit is reached.

NOTE

Application condition where the 2-A limit is exceeded continuously is not allowed. In this case the current limit would be 2 A for 1.5 seconds followed by 2.5-A limit for 1.5 seconds, and this 3-second period repeats.

7.3.2 Internal LDO

The internal LDO regulator converts the input voltage at V_{IN} to a 4.3-V output voltage. The LDO regulator supplies internal and external circuitry. The maximum external load is 5 mA. Connect LDO output with a minimum of 1-µF ceramic capacitor to ground as close to the LDO pin as possible. If an external voltage higher than 4.5 V is connected to LDO pin, the internal LDO is disabled, and the internal circuitry is powered from the external power supply. VIN and VSENSE_N pins must be connected to the same external voltage as LDO pin. See Figure 29 for application schematic example.

7.3.3 LED Current Sinks

7.3.3.1 Current Sink Configuration

The LP8861-Q1 detects LED current sinks configuration during start-up. Any sink connected to the ground is disabled and excluded from the adaptive boost control and fault detection.

7.3.3.2 Current Setting

Maximum current for the LED current sinks is controlled with external R_{ISET} resistor. R_{ISET} value for target maximum current can be calculated using Equation 3:

$$R_{ISET} = 2342 / (I_{OUT} – 2.5) \quad (3)$$

where

- R_{ISET} is current setting resistor, kΩ
- I_{OUT} is output current per output, mA

7.3.3.3 Brightness Control

The LP8861-Q1 controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz. Dimming ratio is calculated as ratio between the input PWM period and minimum on/off time (0.5 µs).

7.3.4 Power Line FET Control

The LP8861-Q1 has a control pin (SD) for driving the gate of an external power-line FET. Power-line FET is an optional feature; an example schematic is shown in Figure 24. Power-line FET limits inrush current by turning on gradually when the device is enabled (VDDIO/EN = high, $V_{IN} > V_{GS}$). Inrush current is controlled by increasing sink current for the FET gradually to 230 µA.

In shutdown the LP8861-Q1 turns off the power-line FET and prevents the possible boost and LEDs leakage. The power switch also turns off in case of any fault which causes the device to enter FAULT RECOVERY state.

7.3.5 LED Current Dimming with External Temperature Sensor

The LP8861-Q1 has an optional feature to decrease automatically LED current when LED overheating is detected with an external NTC sensor. An example of the behavior is shown in Figure 11. When the NTC temperature reaches T1, the LP8861-Q1 starts to decrease the LED current. When the LED current has reduced to 17.5% of the nominal value, current turns off until temperature returns to the operation range. When TSET pin is grounded this feature is disabled. Temperature T1 and de-rate slope are defined by external resistors as explained below.

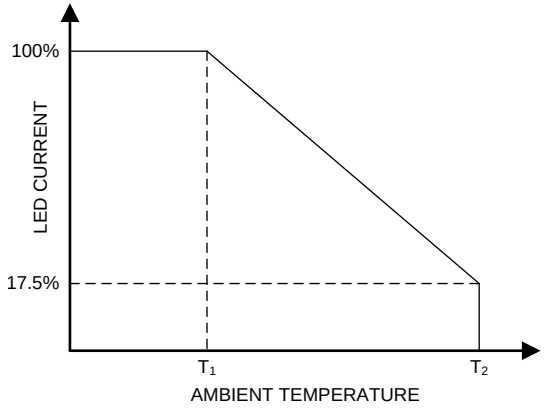


Figure 11. Temperature-Based LED Current Dimming Functionality

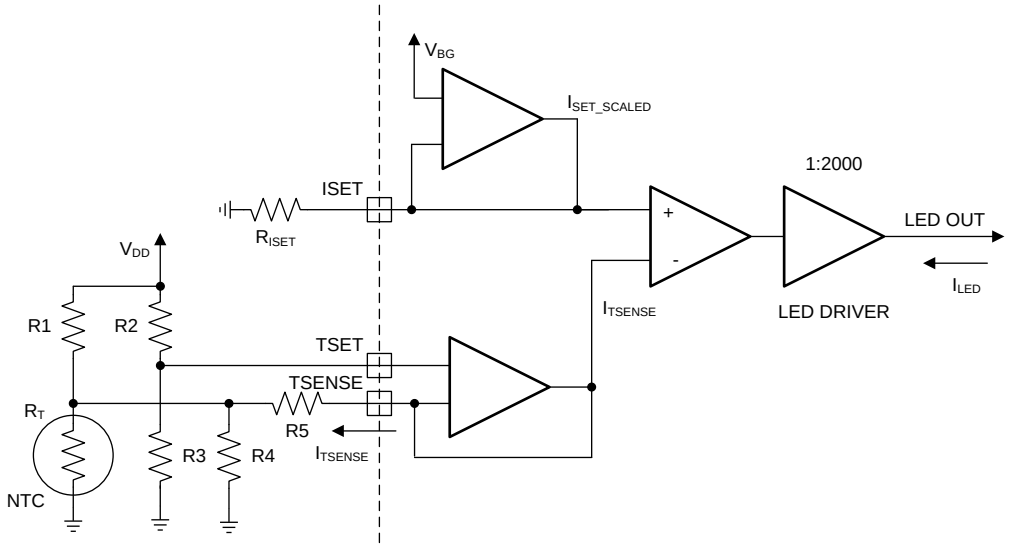


Figure 12. Temperature-Based LED Current Dimming Implementation

When the TSET pin is grounded LED current is set by R_{ISET} resistor:

$$R_{ISET} = 2342 / (I_{OUT} - 2.5) \quad (4)$$

When external NTC is connected, the TSENSE pin current decreases LED output current. The following steps describe how to calculate LED output current.

Parallel resistance of the NTC sensor RT and resistor R4 is calculated by formula:

$$R_{II} = \frac{R_T \times R4}{R_T + R4} \quad (5)$$

TSET voltage can be calculated with Equation 6:

$$V_{TSET} = V_{DD} \times \frac{R3}{R2 + R3} \quad (6)$$

TSENSE pin current is calculated by Equation 7:

$$I_{TSENSE} = \frac{V_{TSET} - V_{DD} \times \frac{R_{II}}{R_{II} + R1}}{R_{II} + R5 - \frac{R_{II}^2}{R_{II} + R1}} \quad (7)$$

ISET pin current defined by R_{ISET} is:

$$I_{SET\_SCALED} = \frac{V_{BG}}{R_{ISET}} \quad (8)$$

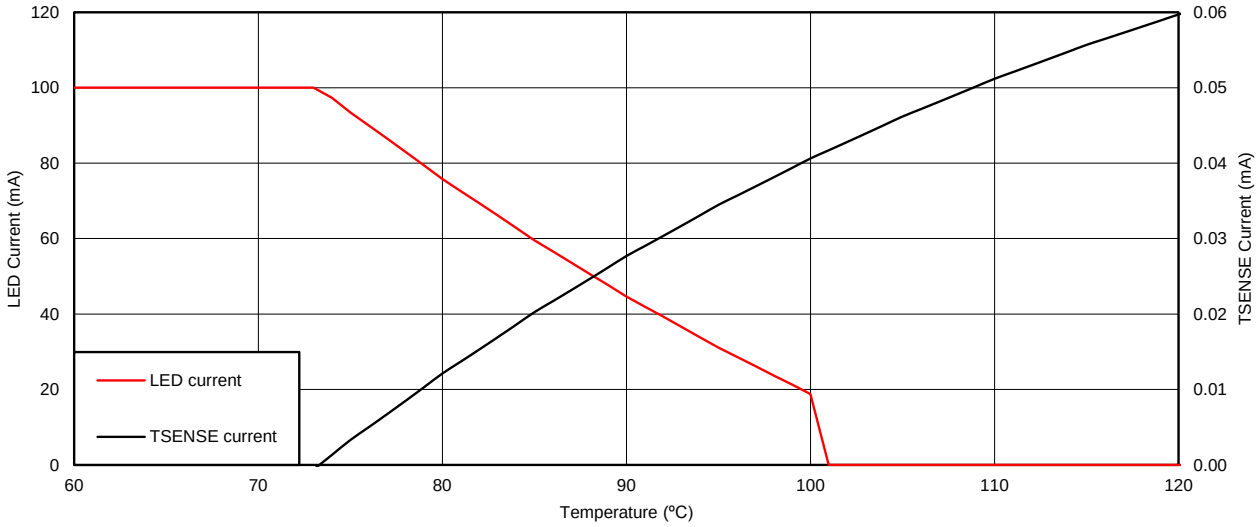
For Equation 9, I_{TSENSE} current must be limited between 0 and I_{SET_SCALED}. If $I_{TSENSE} > I_{SET\_SCALED}$ then set $I_{TSENSE} = I_{SET\_SCALED}$. If $I_{TSENSE} < 0$ then set $I_{TSENSE} = 0$.

LED driver output current is:

$$I_{LED} = (I_{SET\_SCALED} - I_{TSENSE}) \times 2\,000 \quad (9)$$

When current is lower than 17.5% of the nominal value, the current is set to 0 (so called cut-off point).

An Excel® calculator is available for calculating the component values for a specific NTC and target thermal profile (contact your local TI representative). Figure 13 shows an example thermal profile implementation.



NTC – 10 kΩ at 25ºC	R_{ISET} = 24 kΩ	R2 = 10 kΩ	R4 = 100 kΩ
VDD = 4.3V	R1 = 10 kΩ	R3 = 2 kΩ	R5 = 7.5 kΩ

Figure 13. Calculation Example

7.3.6 Protection and Fault Detection

The LP8861-Q1 has fault detection for LED open and short, VIN input overvoltage (VIN_OVP), VIN undervoltage lockout (VIN_UVLO), power line overcurrent (VIN_OCP), and thermal shutdown (TSD).

7.3.6.1 Adaptive Boost Control and Functionality of LED Fault Comparators

Adaptive boost control function adjusts the boost output voltage to the minimum sufficient voltage for proper LED current sink operation. The output with highest V_F LED string is detected and boost output voltage adjusted accordingly. Boost adaptive control voltage step size is defined by maximum boost voltage settings, V_{STEP} = ($V_{MAX\ BOOST}$ - $V_{MIN\ BOOST}$) / 256. Periodic down pressure is applied to the target boost voltage to achieve better system efficiency.

Every LED current sink has 3 comparators for an adaptive boost control and fault detection. Comparator outputs are filtered, filtering time is 1 µs.

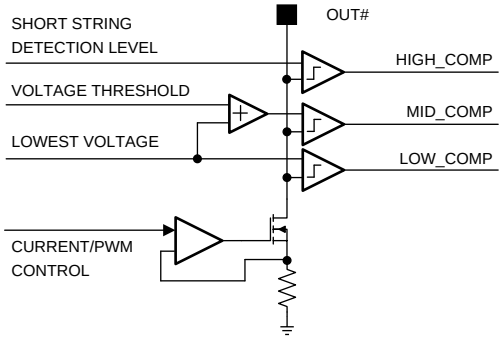


Figure 14. Comparators for Adaptive Voltage Control and LED Fault Detection

Figure 15 illustrates different cases which cause boost voltage increase, decrease, or generate faults. In normal operation, voltage at all the OUT# pins is between LOW_COMP and MID_COMP levels and boost voltage stays constant. LOW_COMP level is the minimum for proper LED current sink operation, 1.1 × V_{SAT} + 0.2 V (typical). MID_COMP level is 1.1 × V_{SAT} + 1.2 V (typical) — that is, typical headroom window is 1 V.

When voltage at all the OUT# pins increases above MID_COMP level, boost voltage adapts downwards.

When voltage at any of the OUT# pins falls below LOW_COMP threshold, boost voltage adapts upwards. In the condition where boost voltage reaches the maximum and there are one or more outputs still below LOW_COMP level, an open LED fault is detected.

HIGH_COMP level, 6 V typical, is the threshold for shorted LED detection. When the voltage of one or more of the OUT# pins increases above HIGH_COMP level and at least one of the other outputs is within the normal headroom window, shorted LED fault is detected.

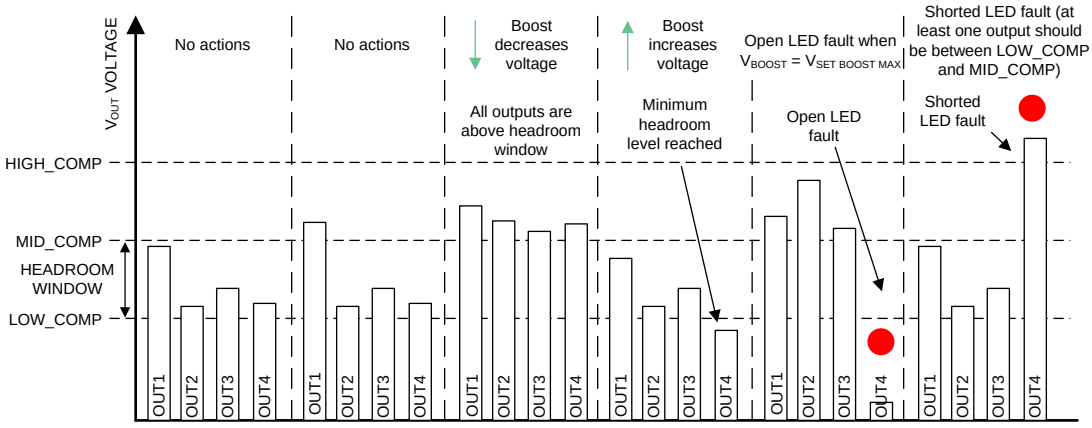


Figure 15. Boost Adaptation and LED Protection Algorithms

7.3.6.2 Overview of the Fault/Protection Schemes

The LP8861-Q1 fault detection behavior is described in Table 3. Detected faults (excluding LED faults) cause the device to enter FAULT_RECOVERY state. In FAULT_RECOVERY the boost and LED outputs of LP8861-Q1 are disabled, power-line FET is turned off, and the FAULT pin is pulled low. Device recovers automatically and enters normal operating mode (ACTIVE) after a recovery time of 100 ms if the fault condition has disappeared. When recovery is successful, the FAULT pin is released.

In case a LED fault is detected, device continues normal operation and only the faulty string is disabled. Fault is indicated via FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2…20 µs. LEDs are turned off for this period but device stays in ACTIVE mode. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.

Table 3. Fault/Protection Schemes

FAULT/ PROTECTION	FAULT NAME	THRESHOLD	CONNECTED TO FAULT PIN	FAULT_ RECOVERY STATE	ACTION
VIN overvoltage protection	VIN_OVP	1. V_{IN} > 42 V 2. V_{BOOST} > V_{SET_BOOST} + (6...10) V V_{SET_BOOST} is voltage value defined by logic during adaptation	Yes	Yes	1. Overvoltage is monitored from the beginning of soft start. Fault is detected if the duration of overvoltage condition is 100 µs minimum. 2. Overvoltage is monitored from the beginning of normal operation (ACTIVE mode). Fault is detected if overvoltage condition duration is 560 ms minimum (t_{filter}). After the first fault detection filter time is reduced to 50 ms for following recovery cycles. When device recovers and has been in ACTIVE mode for 160 ms, filter is increased back to 560 ms.
VIN undervoltage lockout	VIN_UVLO	Falling 3.9 V Rising 4 V	Yes	Yes	Detects undervoltage condition at VIN pin. Sensed from the beginning of soft start. Fault is detected if undervoltage condition duration is 100 µs minimum.
VIN overcurrent protection	VIN_OCP	3 A (50-mΩ current sensor resistor)	Yes	Yes	Detects overcurrent by measuring voltage of the SENSE resistor connected between VIN and VSENSE_N pins. Sensed from the beginning of soft start. Fault is detected if undervoltage condition duration is 10 µs minimum.
Open LED fault	OPEN_LED	LOW_COMP threshold	Yes	No	Detected if one or more outputs are below threshold level, and boost adaptive control has reached maximum voltage. Open string(s) is removed from voltage control loop and PWM is disabled. Fault pin is cleaned by toggling VDDIO/EN pin. If VDDIO/EN is low for a short period of 2…20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Shorted LED fault	SHORT_LED	Shorted string detection level 6 V	Yes	No	Detected if one or more outputs voltages are above shorted string detection level and at least one LED output voltage is within headroom window. Shorted string(s) are removed from the boost voltage control loop and outputs PWM(s) are disabled. Fault pin is cleaned by toggling VDDIO/EN pin. If VDDIO/EN is low for a short period of 2…20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Thermal protection	TSD	165ºC Thermal Shutdown Hysteresis 20ºC	Yes	Yes	Thermal shutdown is monitored from the beginning of soft start. Die temperature must decrease by 20ºC for device to recover.

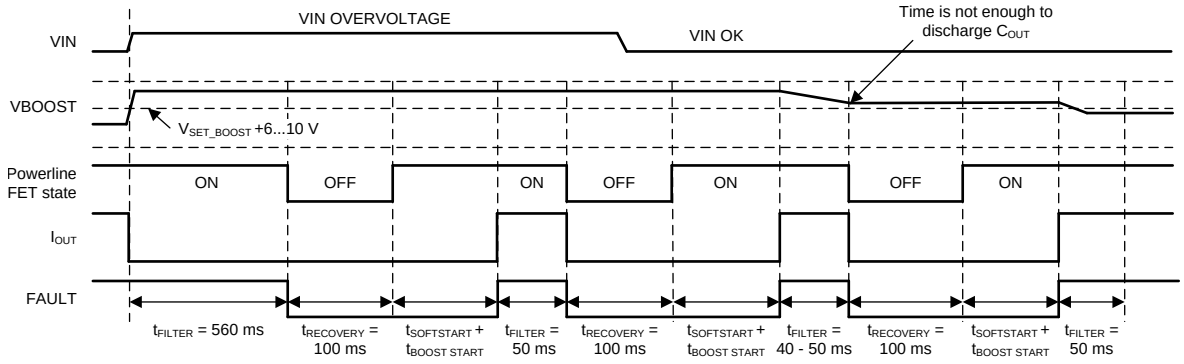


Figure 16. VIN Overvoltage Protection (Boost OVP)

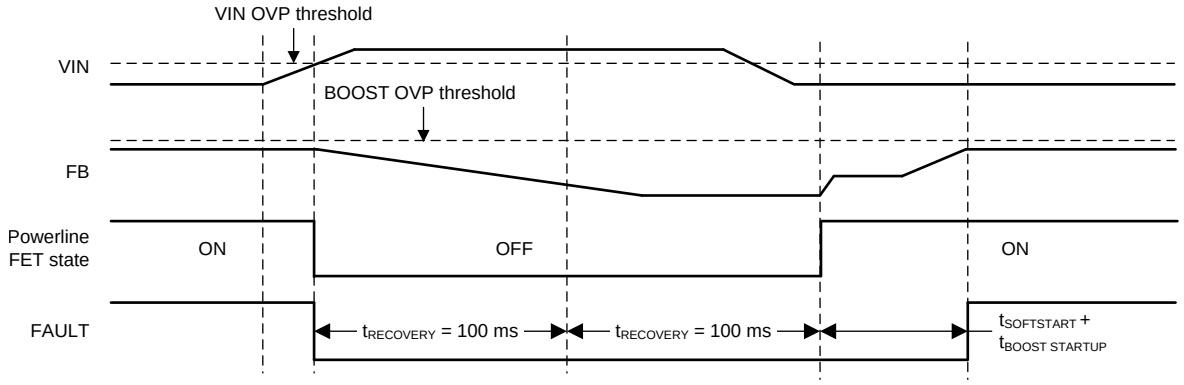


Figure 17. VIN Overvoltage Protection (VIN OVP)

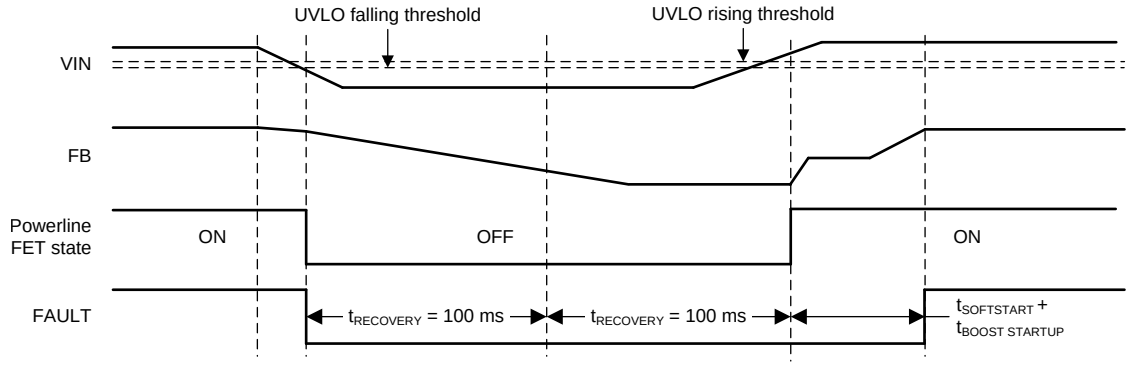


Figure 18. VIN Undervoltage Lockout

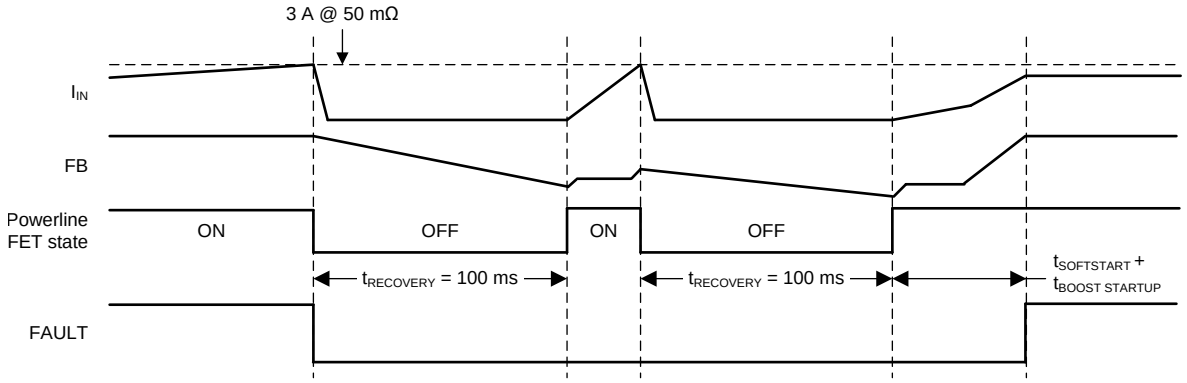


Figure 19. Input Voltage Overcurrent Protection

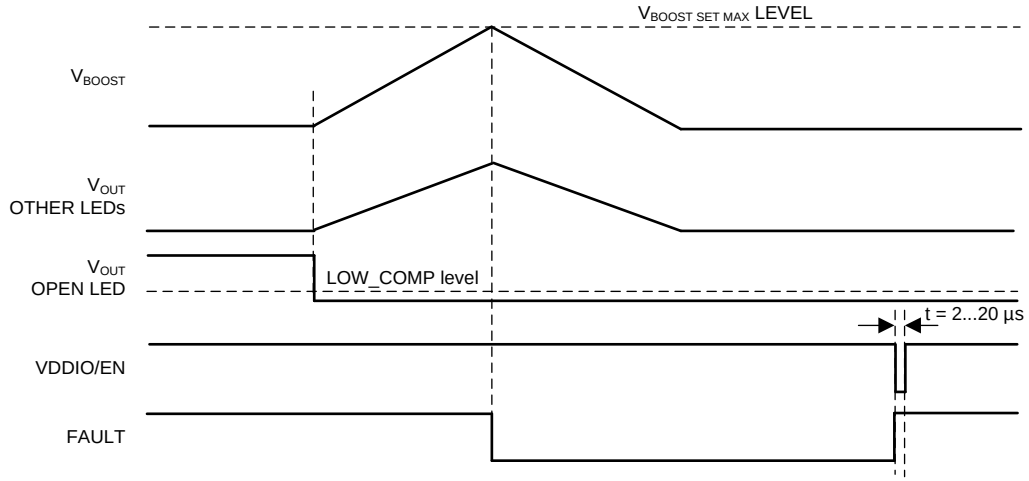


Figure 20. LED Open Fault

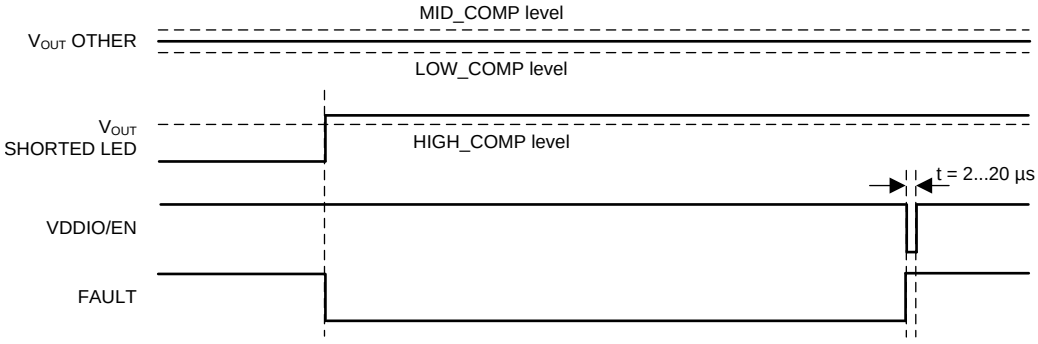


Figure 21. LED Short Fault

7.4 Device Functional Modes

7.4.1 Device States

The LP8861-Q1 enters STANDBY mode when the internal LDO output rises above the power-on reset level, $V_{LDO} > V_{POR\_R}$. In STANDBY mode device is able to detect the VDDIO/EN signal. When VDDIO/EN is pulled high, device powers up. During soft start the external power line FET is opened gradually to limit inrush current. Soft start is followed by boost start, during which time boost voltage is ramped to the initial value. After boost start LED outputs are sensed to detect grounded current sinks. Grounded current sinks are disabled and excluded from the boost voltage control loop.

If a fault condition is detected, the LP8861-Q1 enters FAULT_RECOVERY state. In this state power line FET is switched off and both the boost and LED current sinks are disabled. Fault that cause the device to enter FAULT_RECOVERY are listed in Figure 22. When LED open or short is detected, faulty string is disabled but LP8861-Q1 stays in ACTIVE mode.

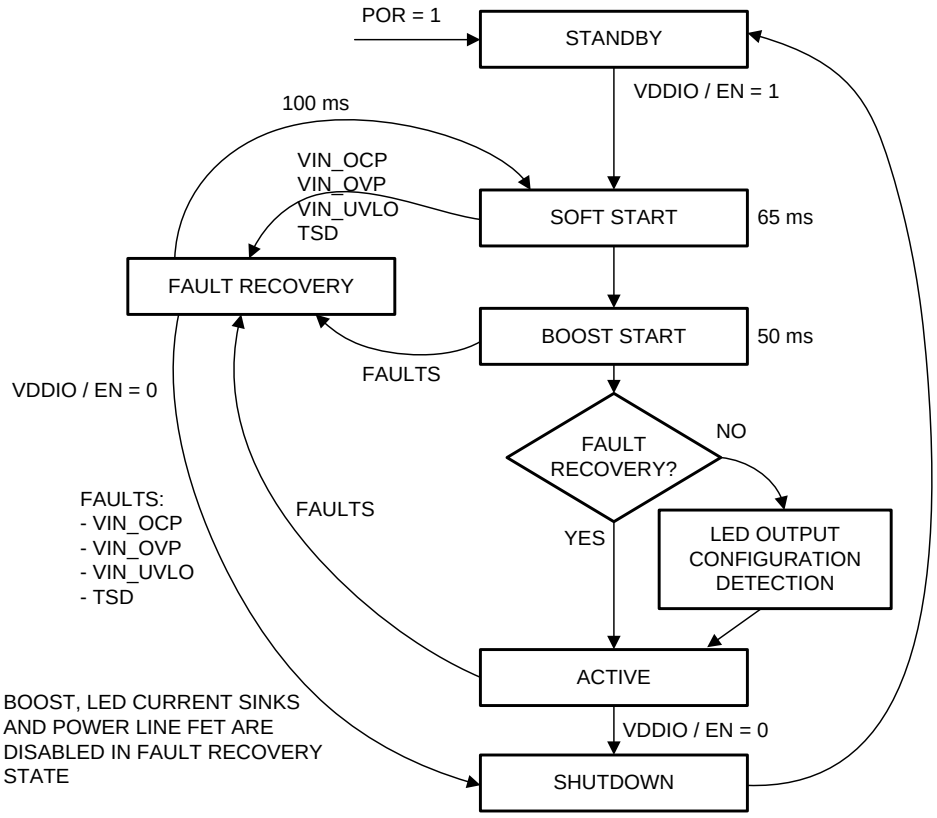


Figure 22. State Diagram

Device Functional Modes (continued)

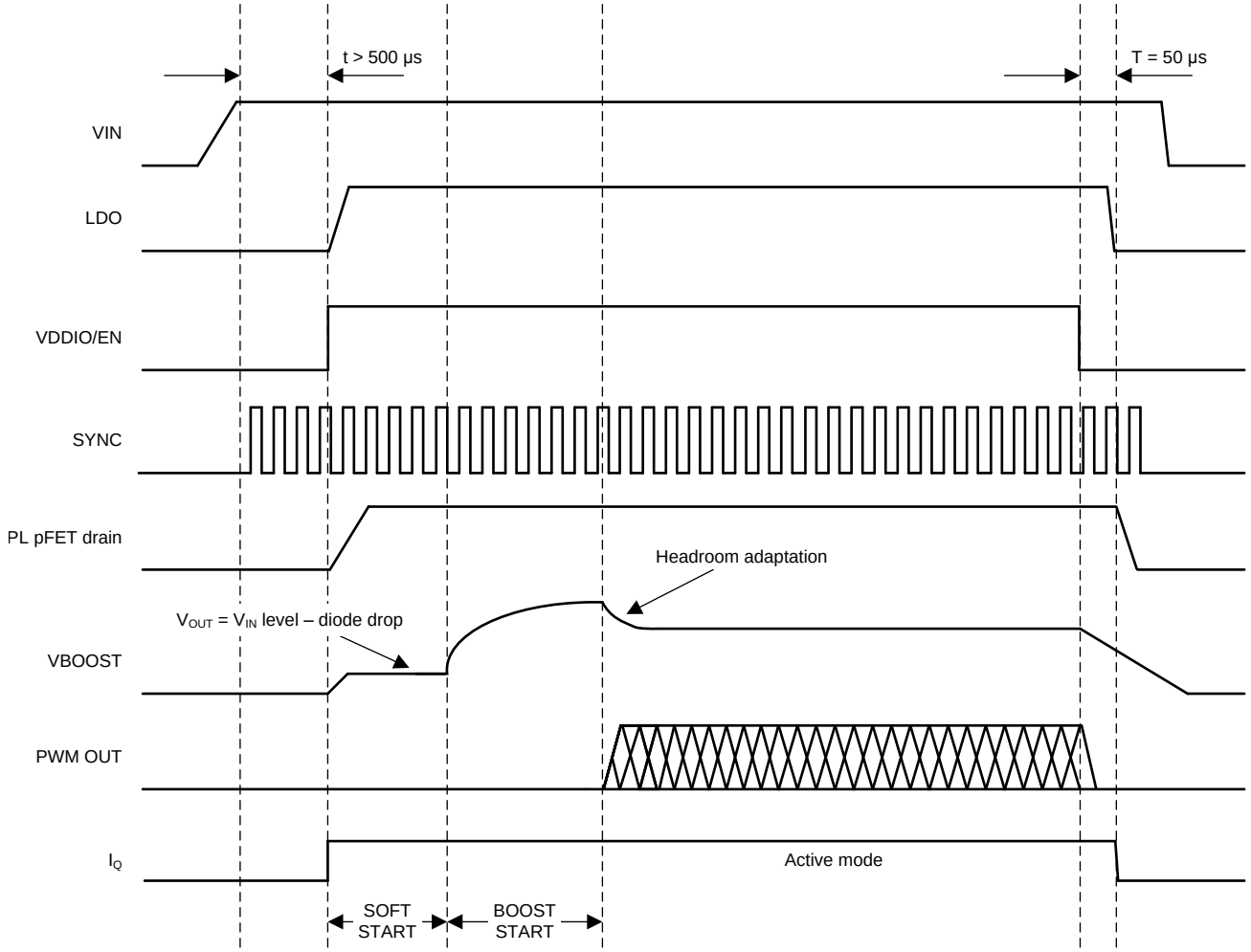


Figure 23. Timing Diagram for the Typical Start-Up and Shutdown

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8861-Q1 is designed for automotive applications, and an input voltage V_{IN} is intended to be connected to the car battery. Device circuitry is powered from the internal LDO which, alternatively, can be used as external VDD voltage — in that case, external voltage must be in the 4.5-V to 5.5-V range.

The LP8861-Q1 uses a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- SYNC pin for boost synchronisation (optional)
- FAULT output to indicate fault condition (optional)

8.2 Typical Applications

8.2.1 Typical Application for 4 LED Strings

Figure 24 shows the typical application for LP8861-Q1 which supports 4 LED strings with maximum current 100 mA and boost switching frequency of 300 kHz.

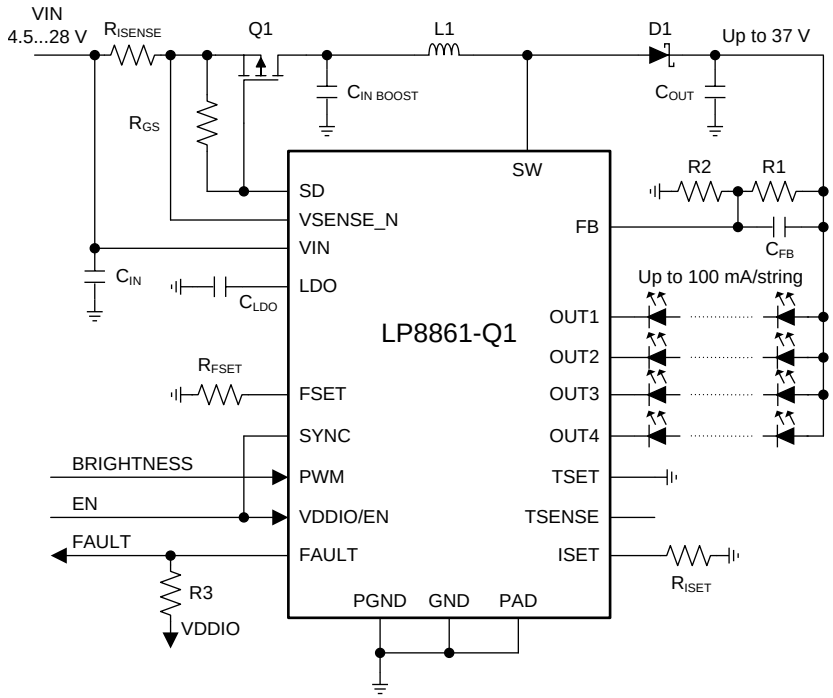


Figure 24. Typical Application for Four Strings 100 mA/String Configuration

Typical Applications (continued)

8.2.1.1 Design Requirements

DESIGN PARAMETER	VALUE
VIN voltage range	4.5…28 V
LED string	4 x 8 LEDs (30 V)
LED string current	100 mA
Max boost voltage	37 V
Boost switching frequency	300 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 µH
C_{IN}	10 µF 50 V
$C_{IN\ BOOST}$	2 × 10-µF, 50-V ceramic + 33-µF, 50-V electrolytic
C_{OUT}	2 × 10-µF, 50-V ceramic + 33-µF, 50-V electrolytic
C_{LDO}	1 µF 10 V
C_{FB}	15 pF
R_{ISET}	24 kΩ
R_{FSET}	210 kΩ
R_{ISENSE}	50 mΩ
R1	750 kΩ
R2	130 kΩ
R3	10 kΩ
R_{GS}	20 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current and the worst-case average to peak inductor current. Equation 10 shows the worst-case conditions:

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation
- V_{OUT} - Output Voltage

(10)

As a result the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating at least 3 A is recommended for most applications. See Table 2 for inductance recommendation for the different switch frequency ranges. The inductor's resistance should be less than 300 mΩ for good efficiency.

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies* (SLVA061). Power Stage Designer™ Tools can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

8.2.1.2.2 Output Capacitor Selection

A ceramic and electrolytic capacitors should have sufficient voltage rating. The DC-bias effect in ceramic capacitors can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendation for different switching frequency range is shown in Table 2. To minimize audible of noise ceramic capacitors their geometric size is usually minimized.

8.2.1.2.3 Input Capacitor Selection

A ceramic and electrolytic capacitors should have sufficient voltage rating. The DC-bias effect in ceramic capacitors can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendation for different switching frequency range is shown in Table 2. To minimize audible of noise ceramic capacitors their geometric size is usually minimized.

8.2.1.2.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect in ceramic capacitors can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-µF capacitor is sufficient.

8.2.1.2.5 Diode

A Schottky diode should be used for the boost output diode. Ordinary rectifier diodes should not be used, because slow switching speeds and long recovery times degrade the efficiency and the load regulation. Diode rating for peak repetitive current should be greater than inductor peak current (up to 3 A) to ensure reliable operation. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage.

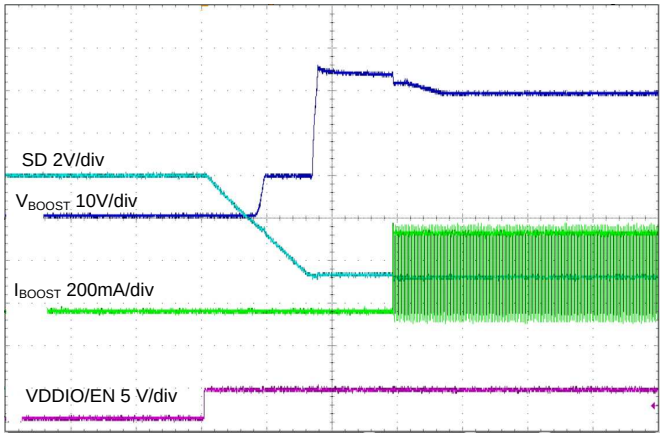
8.2.1.2.6 Power Line Transistor

A pFET transistor with necessary voltage rating (V_{DS} at least 5 V higher than max input voltage) should be used. Current rating for the FET should be the same as input peak current or greater. Transfer characteristic is very important for pFET. V_{GS} for open transistor should be less then V_{IN}. A 20-kΩ resistor between pFET gate and source is sufficient.

8.2.1.2.7 Input Current Sense Resistor

A high-power 50-mΩ resistor should be used for sensing the boost input current. Power rating can be calculated from the input current and sense resistor resistance value. Increasing R_{ISENSE} decreases VIN OCP current proportionally.

8.2.1.3 Application Curves



f_{SW} = 300 kHz V_{IN} = 10 V
Brightness PWM 50% 100 Hz

Figure 25. Typical Start-up

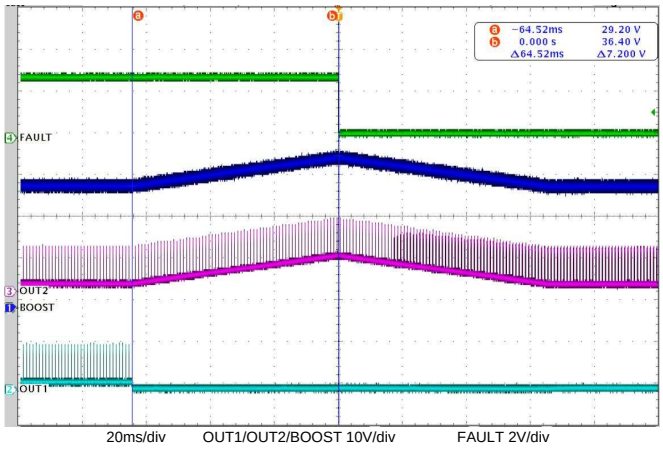
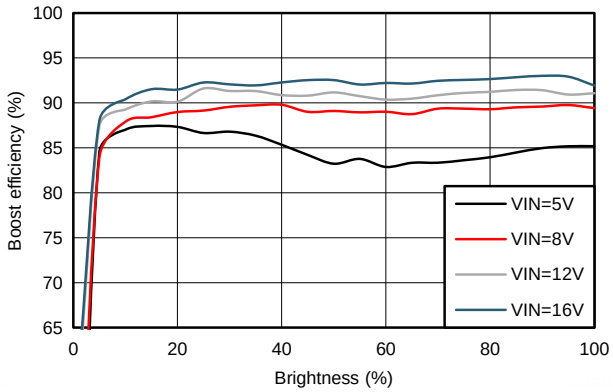
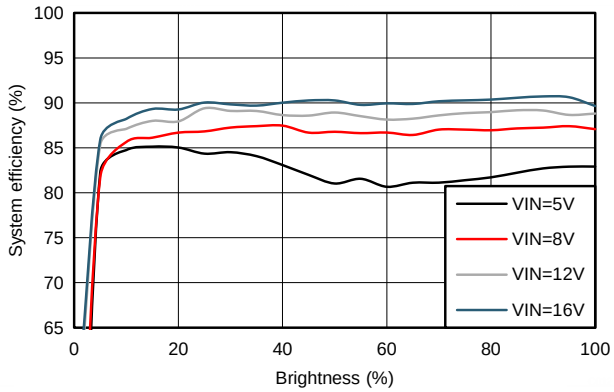


Figure 26. Open LED Fault



Load 4 strings, 8 LED per string f_{SW}= 300 kHz
I = 100 mA/string for V_{IN} = 12 V and 16 V
I = 60 mA/sting for V_{IN} = 8 V
I = 50 mA/string for V_{IN} = 5 V

Figure 27. Boost Efficiency



Load 4 strings, 8 LED per string f_{SW} = 300 kHz
I = 100 mA/string for V_{IN} = 12 V and V_{IN} = 16 V
I = 60 mA/sting for V_{IN} = 8 V
I = 50 mA/string for V_{IN} = 5 V

Figure 28. System Efficiency

8.2.2 High Output Current Application

The LP8861-Q1 current sinks can be tied together to drive LED with higher current. To drive 200 mA per string 2 outputs can be connected together. All 4 outputs connected together can drive an up to 400-mA LED string. Device circuitry is powered from external VDD voltage.

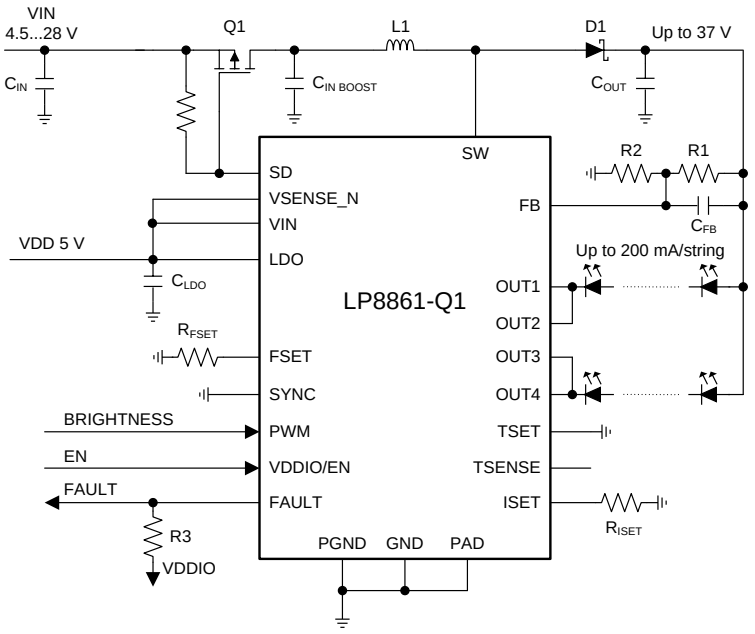


Figure 29. Two Strings 200 mA/String Configuration

8.2.2.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5…28 V
LED string	2 x 8 LEDs (30 V)
LED string current	200 mA
Max boost voltage	37 V
Boost switching frequency	2.2 MHz
External boost sync	not used
Boost spread spectrum	disabled
L1	4.7 µH
C_{IN}	10 µF 50 V
$C_{IN\ BOOST}$	2 × 10-µF, 50-V ceramic
C_{OUT}	3 × 10-µF, 50-V ceramic
C_{LDO}	1 µF 10 V
C_{FB}	4.7 pF
R_{ISET}	24 kΩ
R_{FSET}	24 kΩ
R1	750 kΩ
R2	130 kΩ
R3	10 kΩ
R_{GS}	20 kΩ

8.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.2.3 Application Curves

See *Application Curves*.

8.2.3 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. The SW pin voltage is equal to the sum of the input voltage and output voltage in SEPIC mode — this fact limits the maximum input voltage in this mode. LED current sinks not used should be connected to ground. External frequency can be used to synchronize boost/SEPIC switching frequency, and external frequency can be modulated to spread switching frequency spectrum.

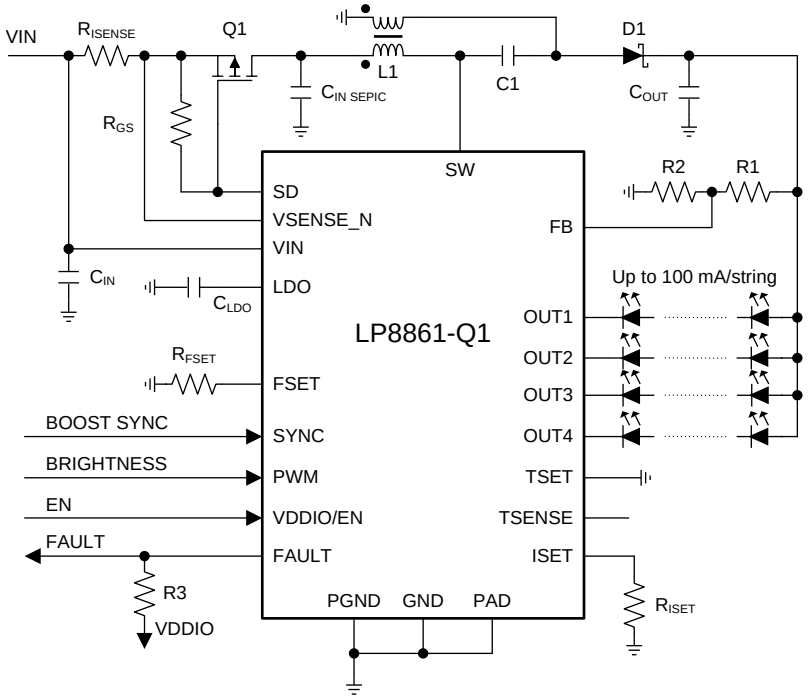


Figure 30. SEPIC Mode, 4 Strings 100 mA/String Configuration

8.2.3.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5…30 V
LED string	4 x 4 LEDs (14.5 V)
LED string current	100 mA
Max boost voltage	17.5 V
Boost switching frequency	300 kHz
External boost sync	used
Boost spread spectrum	not available with external sync
L1	33 µH
C_{IN}	10 µF 50 V
$C_{IN\ SEPIC}$	2 × 10-µF, 50-V ceramic + 33-µF 50-V electrolytic
C1	10-µF 50-V ceramic
C_{OUT}	2 × 10-µF, 50-V ceramic +33-µF 50-V electrolytic
C_{LDO}	1 µF 10 V
R_{ISET}	24 kΩ
R_{FSET}	210 kΩ
R_{ISENSE}	50 mΩ
R1	390 kΩ
R2	130 kΩ
R3	10 kΩ
R_{GS}	20 kΩ

8.2.3.2 Detailed Design Procedure

See *Detailed Design Procedure* for external component recommendations. The *Power Stage Designer™ Tools* can be use for defining SEPIC component current and voltage ratings according to application: http://www.ti.com/tool/powerstage-designer

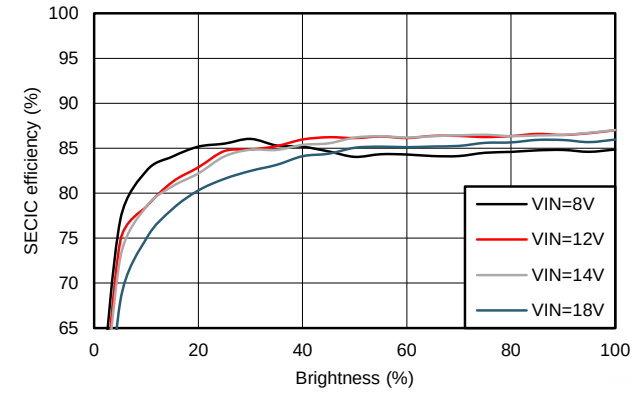
8.2.3.2.1 Diode

A Schottky diode with a low forward drop and fast switching speed should be used for the SEPIC output diode. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times degrade the efficiency and load regulation. The diode must be able to handle peak repetitive current greater than the integrated FET peak current (SW pin limit), thus 3 A or higher must be used to ensure reliable operation. Average current rating should be greater than the maximum output current. Choose a diode with reverse breakdown larger than the sum of input voltage and output voltage.

8.2.3.2.2 Inductor

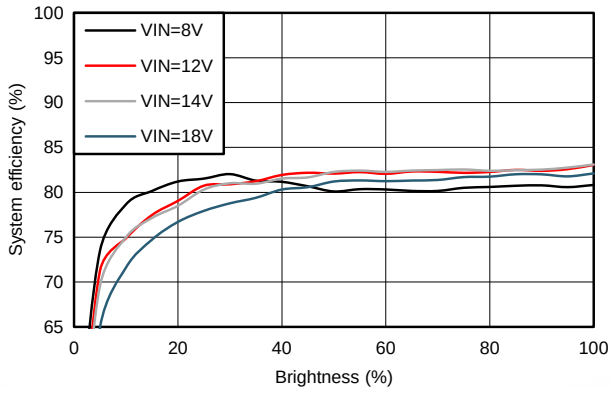
Coupled or uncoupled inductors can be used in SEPIC mode. Coupled inductor typically provides better efficiency. *Power Stage Designer™* Tools can be used for the SEPIC inductance calculation: http://www.ti.com/tool/powerstage-designer.

8.2.3.3 Application Curves



Load 4 strings, 4 LED per string
I = 100 mA/string
f_{SW}= 300 kHz

Figure 31. SEPIC Efficiency



Load 4 strings, 4 LED per string
I = 100 mA/string
f_{SW}= 300 kHz

Figure 32. System Efficiency

8.2.4 Application with Temperature Based LED Current De-rating

The LP8881-Q1 is able to protect connected LED strings from overheating. LED current versus temperature behavior can be adjusted with external resistor as described in *LED Current Dimming with External Temperature Sensor*.

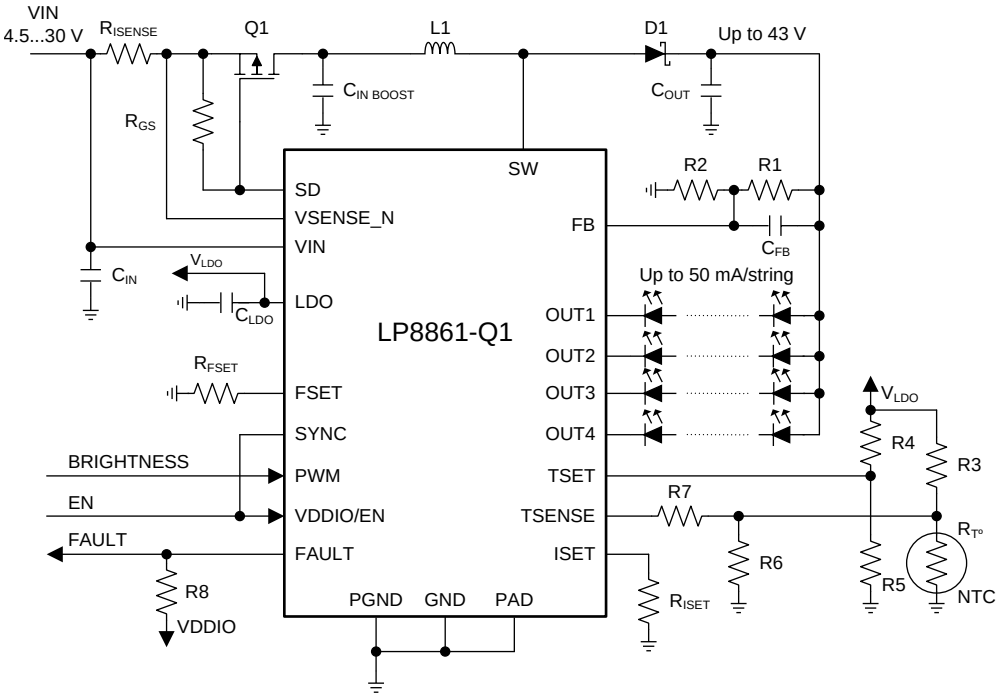


Figure 33. Temperature Based LED Current De-rating

8.2.4.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5…30 V
LED string	4 x 9 LEDs (33 V)
LED string current	50 mA
Max boost voltage	43 V
Boost switching frequency	400 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 µH
C_{IN}	10-µF 50-V ceramic
$C_{IN\ BOOST}$	2 × 10-µF, 50-V ceramic + 33-µF, 50-V electrolytic
C_{OUT}	2 × 10-µF, 50-V ceramic + 33-µF, 50-V electrolytic
C_{LDO}	1 µF 10 V
C_{FB}	15 pF
R_{ISET}	48 kΩ
R_{FSET}	160 kΩ
R_{ISENSE}	50 mΩ
R1	866 kΩ
R2	130 kΩ
R3	12 kΩ
R4	10 kΩ
R5	1.8 kΩ
R6	82 kΩ
R7	16 kΩ
R8	10 kΩ
RT	10 kΩ @ 25ºC
R_{GS}	20 kΩ

8.2.4.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.4.3 Application Curve

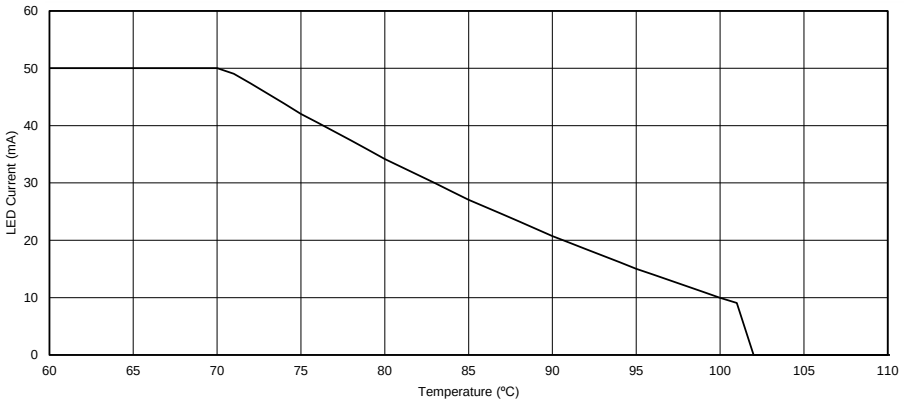


Figure 34. LED Current vs Temperature

9 Power Supply Recommendations

The LP8861-Q1 device is designed to operate from a car battery. The device should be protected from reverse voltage polarity and voltage dump over 50 V. The resistance of the input supply rail must be low enough so that the input current transient does not cause too high drop at the LP8861-Q1 VIN pin. If the input supply is connected by using long wires additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the V_{IN} line.

10 Layout

10.1 Layout Guidelines

Figure 35 is a layout recommendation for the LP8861-Q1 used to demonstrate the principles of good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Bypass LDO capacitor must as close as possible to the device.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds need to be close to each other to minimize current loop size
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High-frequency return currents try to find route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the “positive” current route in the ground plane, if the ground plane is intact under the route
- GND plane needs to be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting need to be on the same direction in optimal case.
- Inductors must be placed so that the current flows in the same direction as in the current loops. Rotating inductor 180° changes current direction.
- Use separate power and noise-free grounds. Power ground is used for boost converter return current and noise-free ground for more sensitive signals, like LDO bypass capacitor grounding as well as grounding the GND pin of the device itself.
- Boost output feedback voltage to LEDs need to be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1-µF bypass capacitor as close as possible to the LDO pin.
- Input and output capacitors need strong grounding (wide traces, many vias to GND plane).
- If two output capacitors are used they need symmetrical layout to get both capacitors working ideally.
- Output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads; this increases EMI. DC bias characteristics need to be obtained from the component manufacturer; DC bias is not taken into account on component tolerance. X5R/X7R capacitors are recommended.

10.2 Layout Example

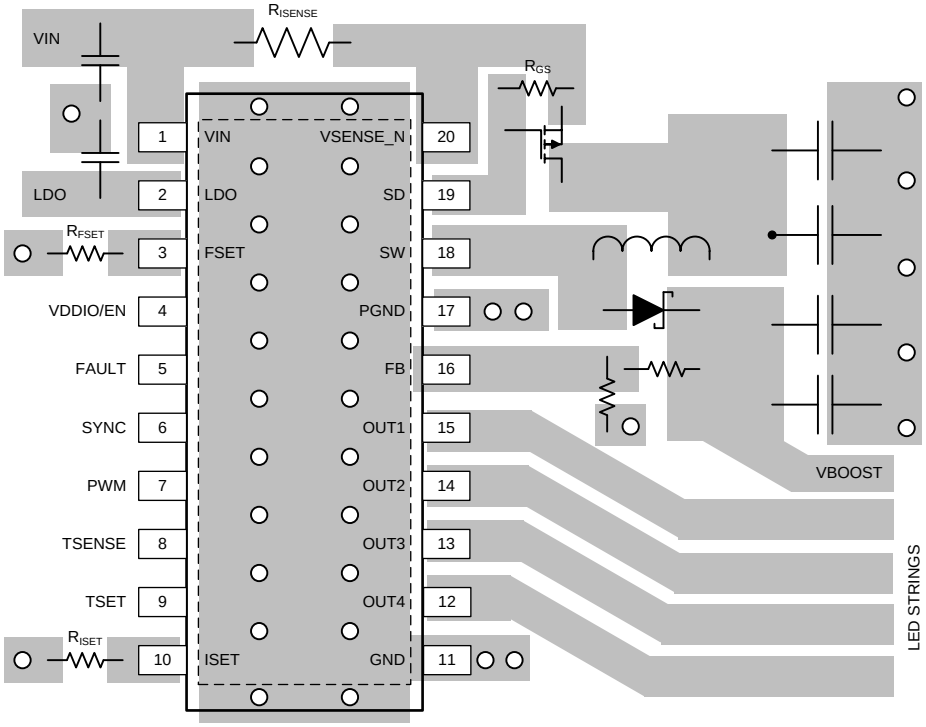


Figure 35. LP8861-Q1 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

- *Using the LP8861-Q1EVM Evaluation Module* (SNVU456)
- *PowerPAD™ Thermally Enhanced Package Application Note* (SLMA002)
- TI Application Note *Understanding Boost Power Stages in Switch Mode Power Supplies* (SLVA061)
- *Power Stage Designer™ Tools*, http://www.ti.com/tool/powerstage-designer

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
Excel is a registered trademark of Microsoft Corporation.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8861QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8861Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

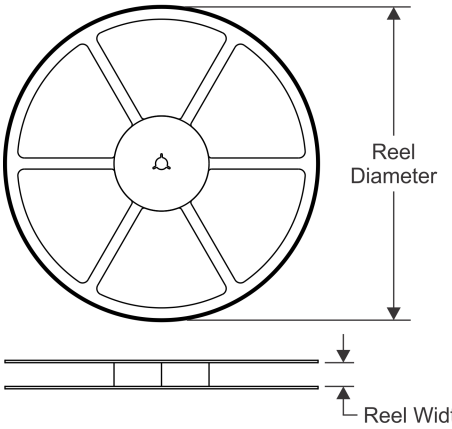
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

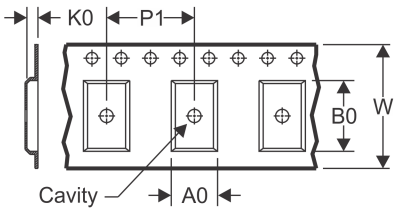
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

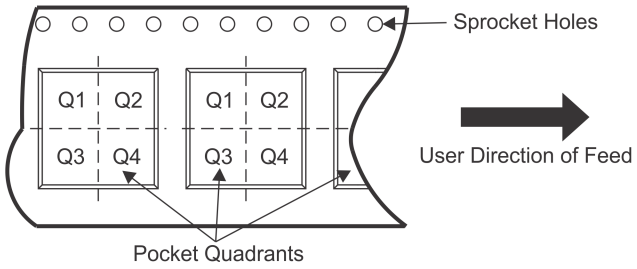


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

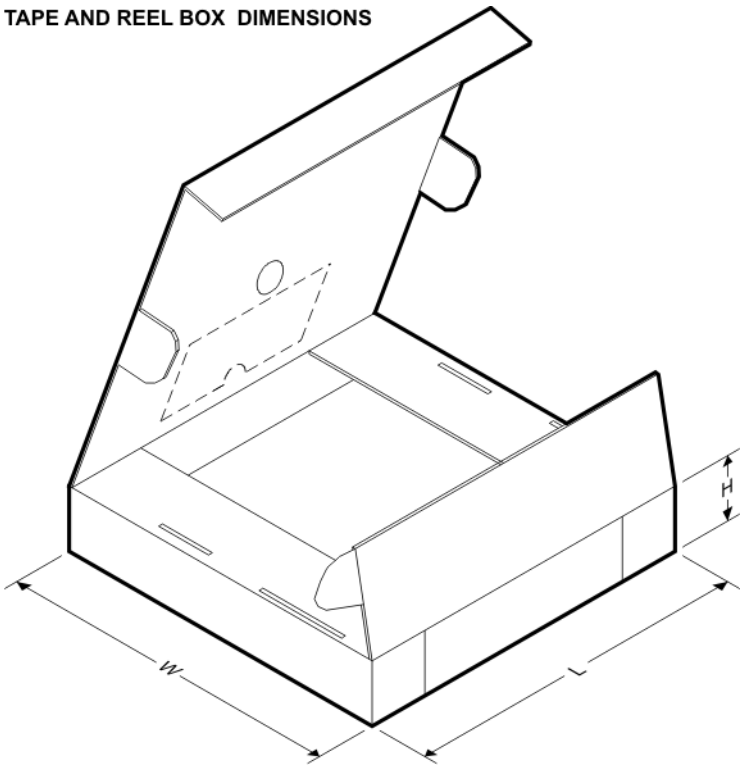
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8861QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8861QPWPRQ1	HTSSOP	PWP	20	2000	367.0	367.0	38.0

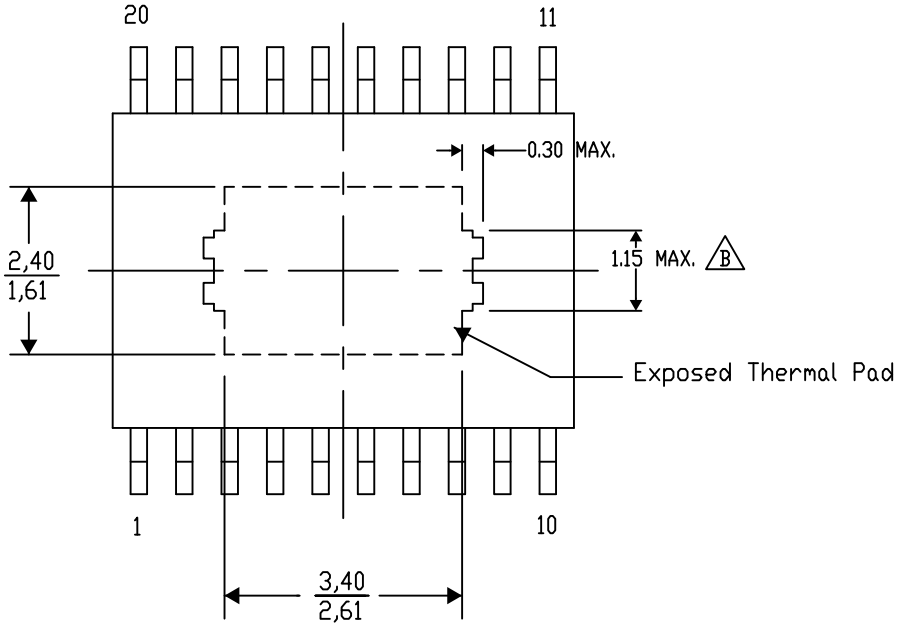
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

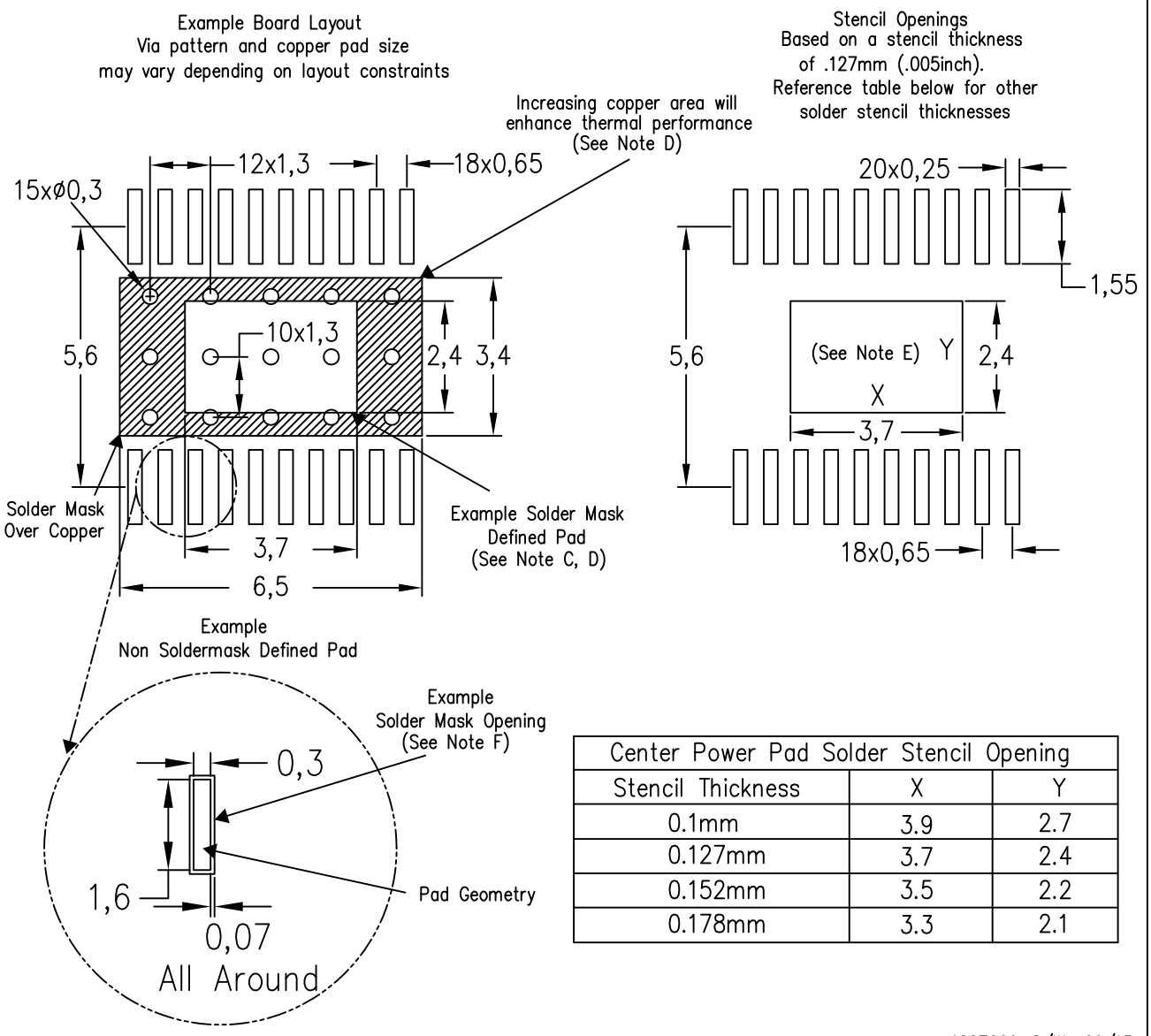
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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