

## P-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD25401Q3](#)

### FEATURES

- Ultra Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Low  $R_{DS(on)}$
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

### APPLICATIONS

- DC-DC Converters
- Battery Management
- Load Switch
- Battery Protection

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion load management applications. The SON 3x3 package offers excellent thermal performance for the size of the package.

**Table 1. PRODUCT SUMMARY**

V <sub>DS</sub>	Drain to Source Voltage	–20		V
Q <sub>g</sub>	Gate Charge Total (4.5V)	8.8		nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	2.1		nC
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = –2.5V	13.5	mΩ
		V <sub>GS</sub> = –4.5V	8.8	mΩ
V <sub>th</sub>	Threshold Voltage	–0.85		V

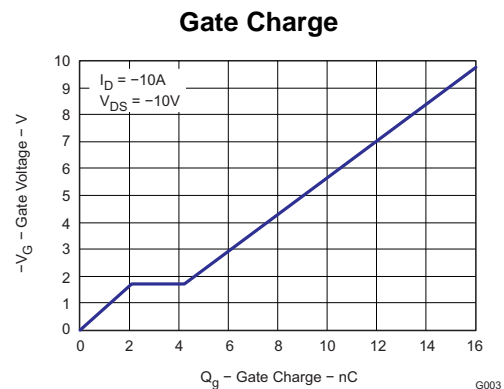
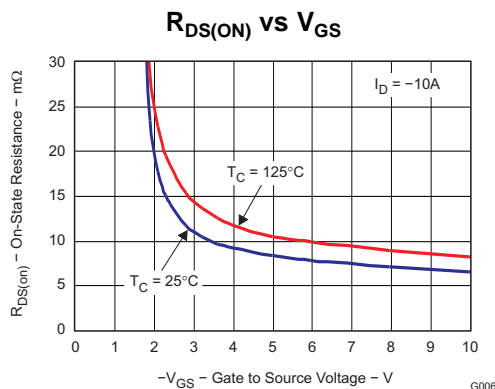
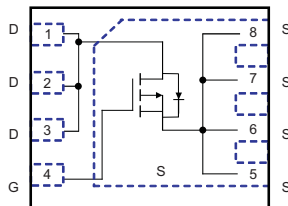
### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25401Q3	SON 3 x 3 Plastic Package	13-inch reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	–20	V
$V_{GS}$	Gate to Source Voltage	+12 / –12	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	–60	A
	Continuous Drain Current <sup>(1)</sup>	–14	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	–82	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.8	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	–55 to 150	$^\circ\text{C}$

- (1)  $R_{\theta JA} = 45^\circ\text{C/W}$  on 1inch<sup>2</sup> Cu (2 oz.) on 0.060" thick FR4 PCB.  
 (2) Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

**Figure 1. Top View**


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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## ELECTRICAL CHARACTERISTICS

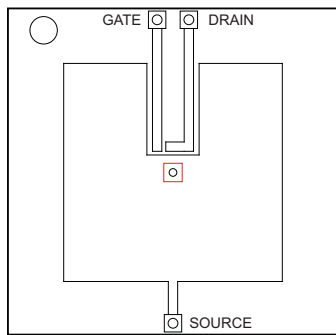
(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV <sub>DSS</sub>	Drain to Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = −250μA	−20			V	
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = −20V to −16V	−1			μA	
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V	−100			nA	
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250μA	−0.6	−0.85	−1.2	V	
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = −2.5V, I <sub>D</sub> = −10A	13.5			18.2	mΩ
		V <sub>GS</sub> = −4.5V, I <sub>D</sub> = −10A	8.8			11.7	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = −15V, I <sub>D</sub> = −10A	43			S	
Dynamic Characteristics							
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = −10V, f = 1MHz	1070			1400	pF
C <sub>OSS</sub>	Output Capacitance		560			730	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance		180			230	pF
Q <sub>g</sub>	Gate Charge Total (4.5V)	V <sub>DS</sub> = −10V, I <sub>D</sub> = −10A	8.8			12.3	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain		2.1				nC
Q <sub>gs</sub>	Gate Charge Gate to Source		2.1				nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>		0.9				nC
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = −10V, V <sub>GS</sub> = 0V	8.2				nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = −10V, V <sub>GS</sub> = −4.5V, I <sub>D</sub> = −10A , R <sub>G</sub> = 5.1Ω	8.1				ns
t <sub>r</sub>	Rise Time		3.9				ns
t <sub>d(off)</sub>	Turn Off Delay Time		13.5				ns
t <sub>f</sub>	Fall Time		12.6				ns
Diode Characteristics							
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = −10A, V <sub>GS</sub> = 0V	−0.7			−1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = −12.5V, I <sub>F</sub> = −10A, di/dt = 300A/μs	17.4				nC
t <sub>rr</sub>	Reverse Recovery Time		21				ns

## THERMAL INFORMATION

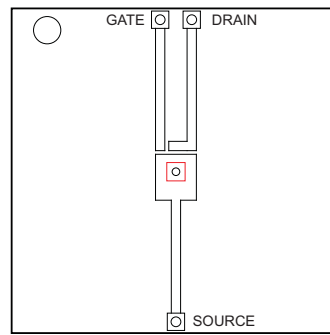
THERMAL METRIC <sup>(1)(2)</sup>		CSD25401Q3	UNITS
		8 PIN	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	42.0	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	20.6	
θ <sub>JB</sub>	Junction-to-board thermal resistance	8.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.7	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



M0137-01

Max  $R_{\theta JA} = 57^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> of 2 oz. Cu.

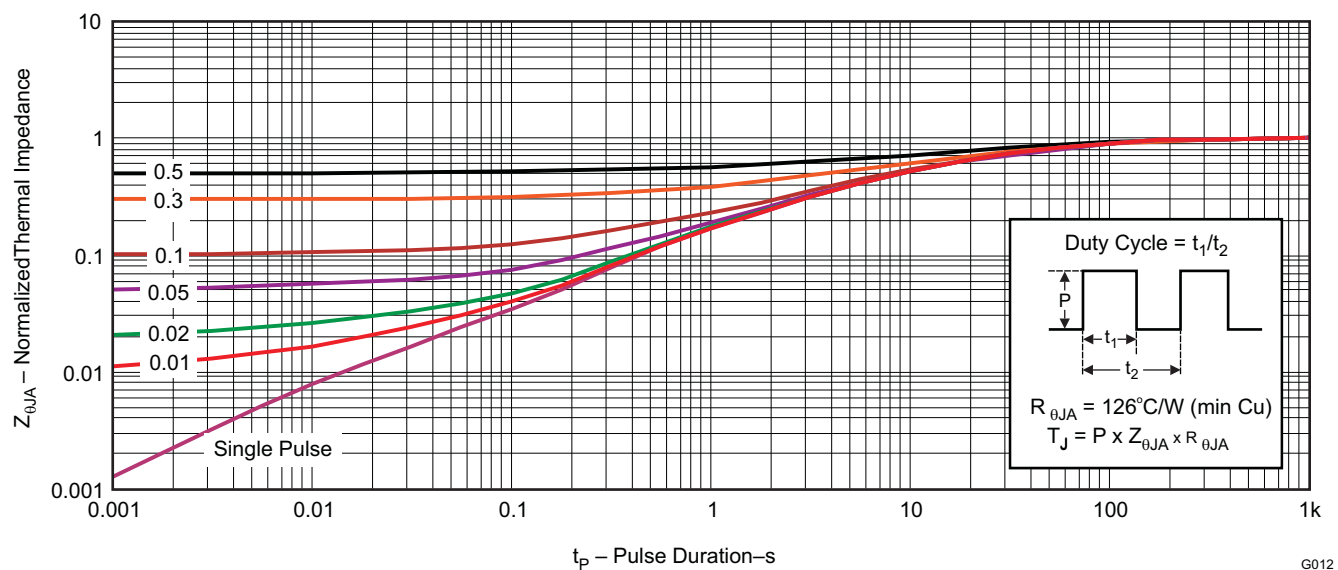


M0137-02

Max  $R_{\theta JA} = 158^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

## TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

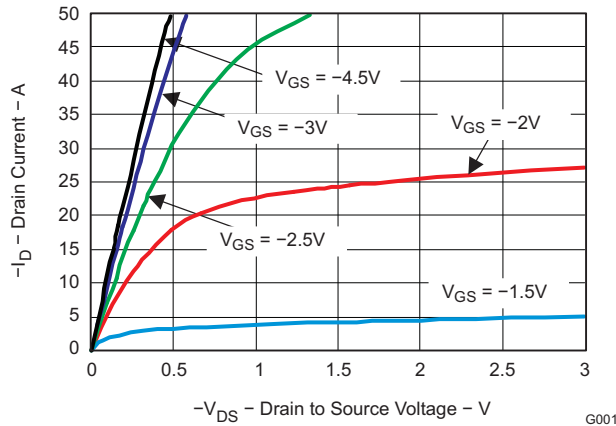


G012

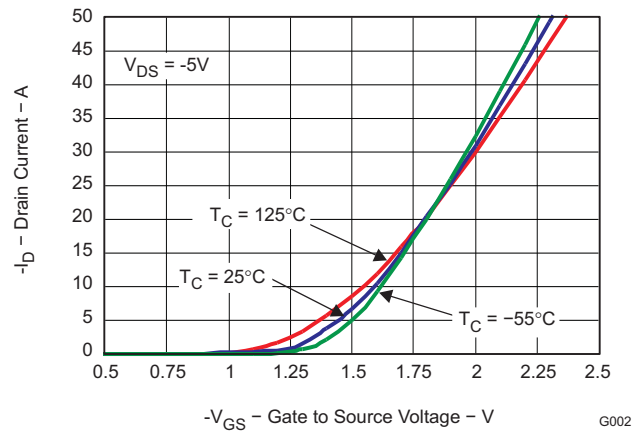
Figure 2. Transient Thermal Impedance

## TYPICAL MOSFET CHARACTERISTICS (continued)

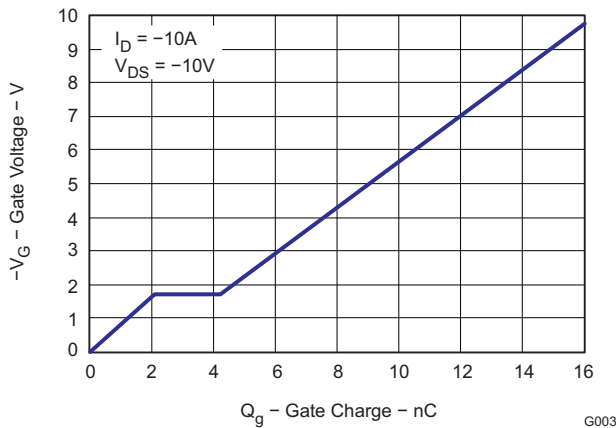
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



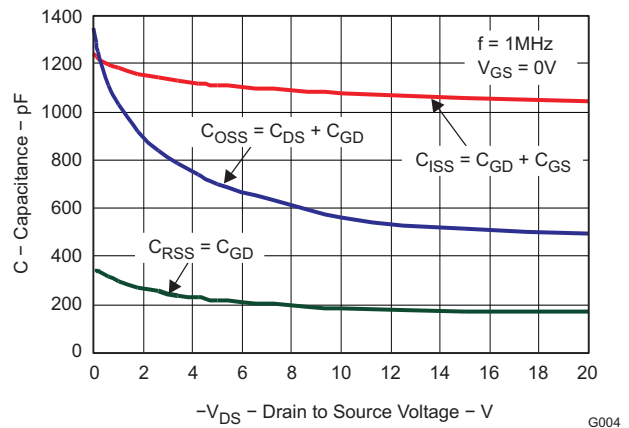
**Figure 3. Saturation Characteristics**



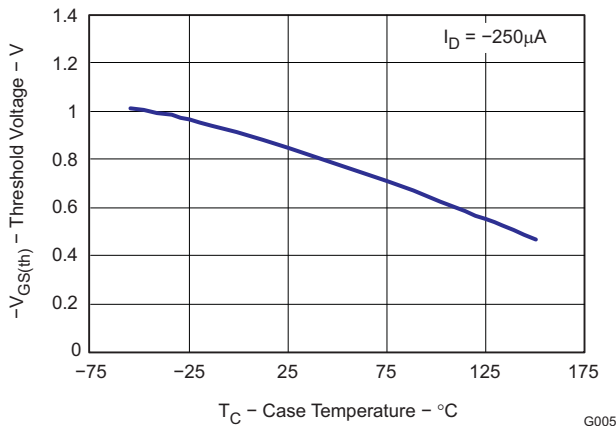
**Figure 4. Transfer Characteristics**



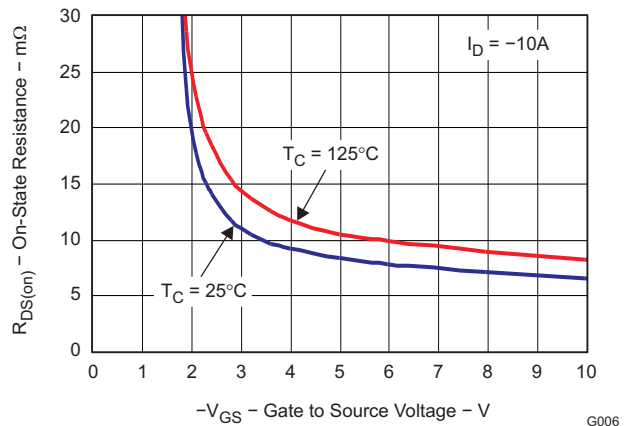
**Figure 5. Gate Charge**



**Figure 6. Capacitance**



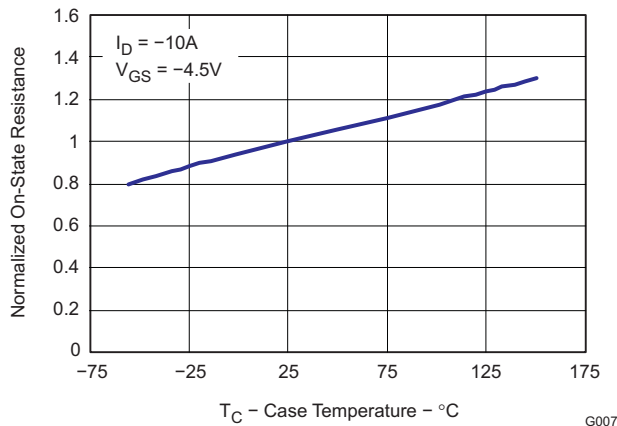
**Figure 7. Threshold Voltage vs. Temperature**



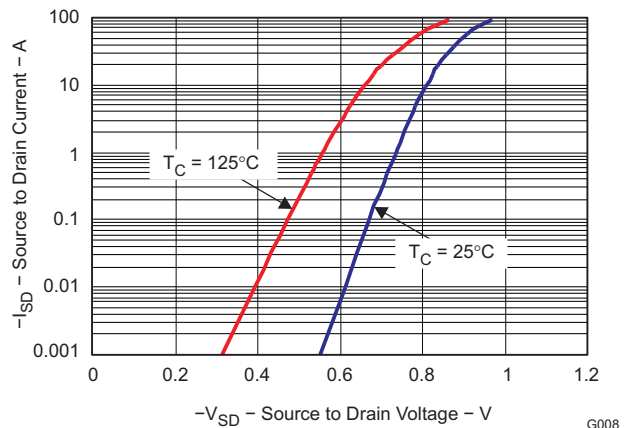
**Figure 8. On Resistance vs. Gate Voltage**

## TYPICAL MOSFET CHARACTERISTICS (continued)

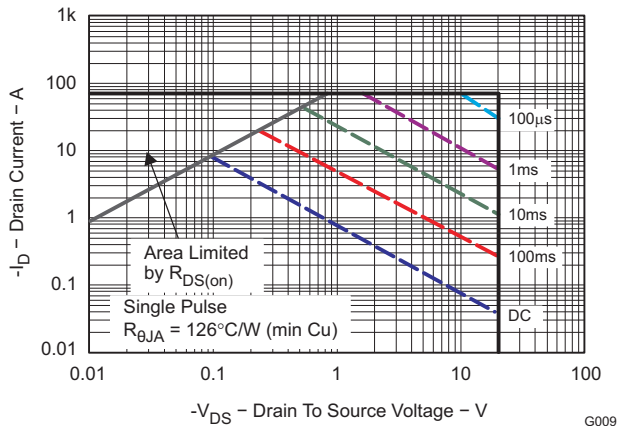
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



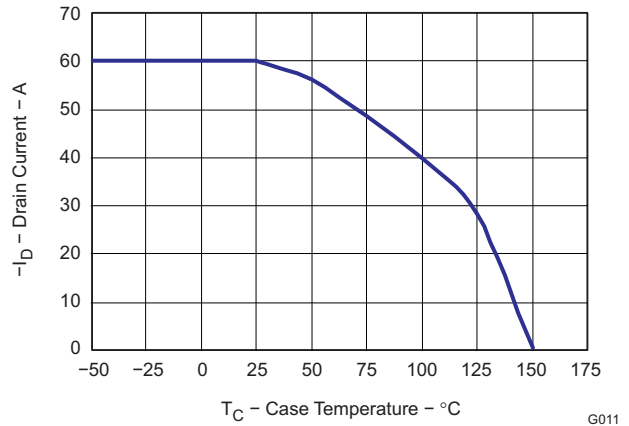
**Figure 9. On Resistance vs. Temperature**



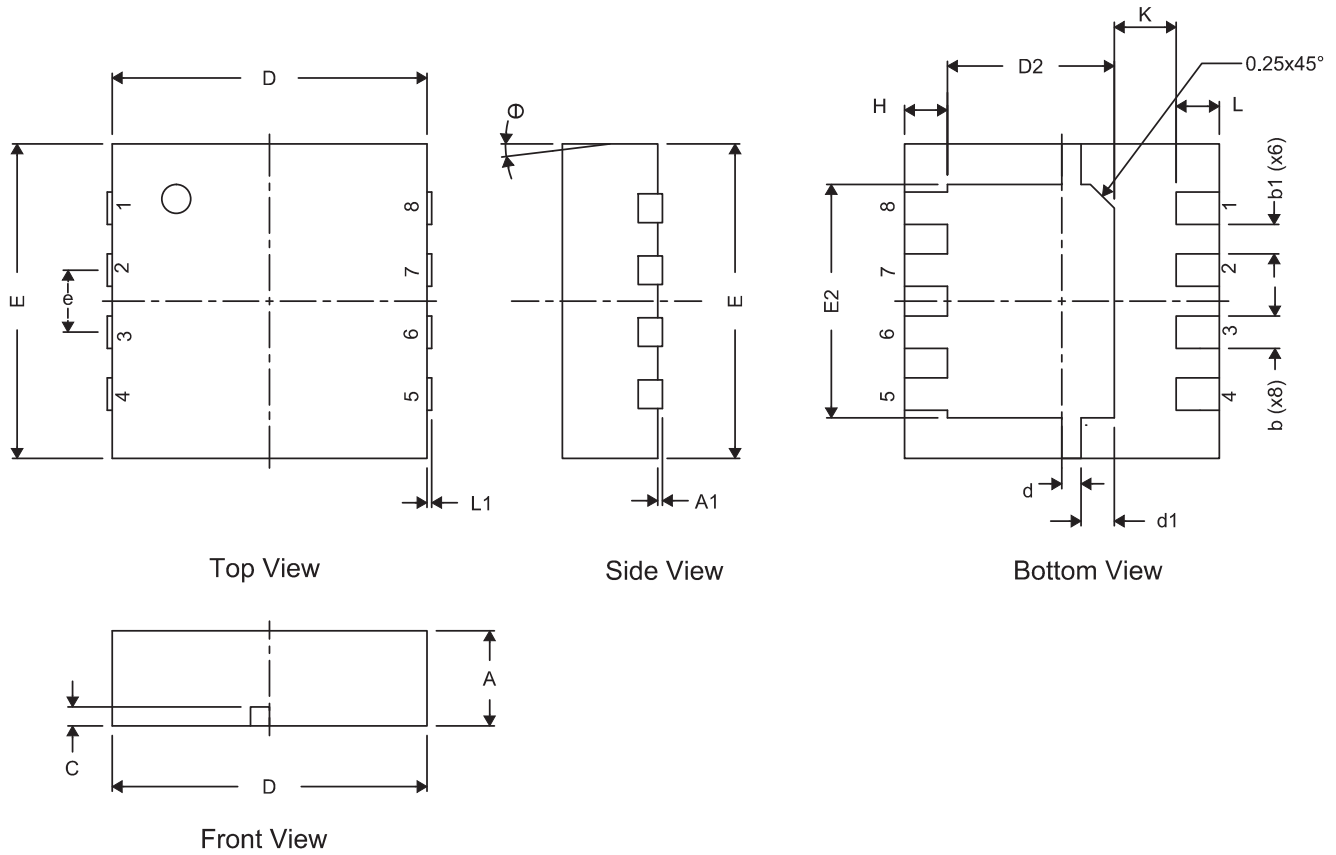
**Figure 10. Typical Diode Forward Voltage**



**Figure 11. Maximum Safe Operating Area**

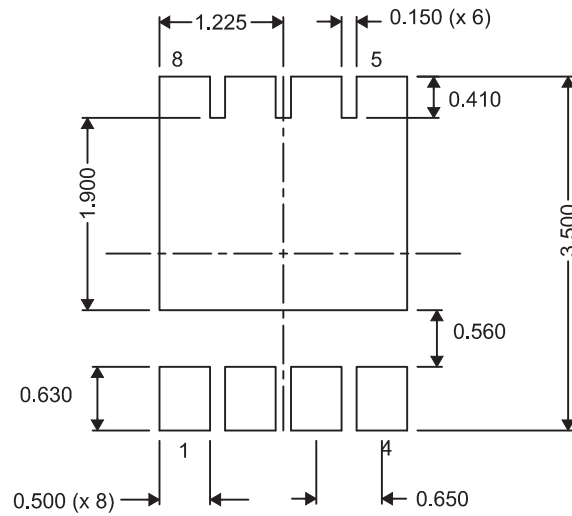


**Figure 12. Maximum Drain Current vs. Temperature**

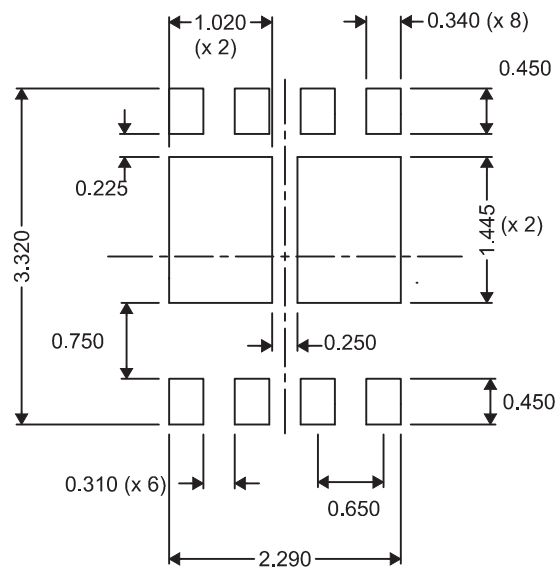
**MECHANICAL DATA****CSD25401Q3 Package Dimensions**

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0		0	0		0
$\theta$	0		0	0		0

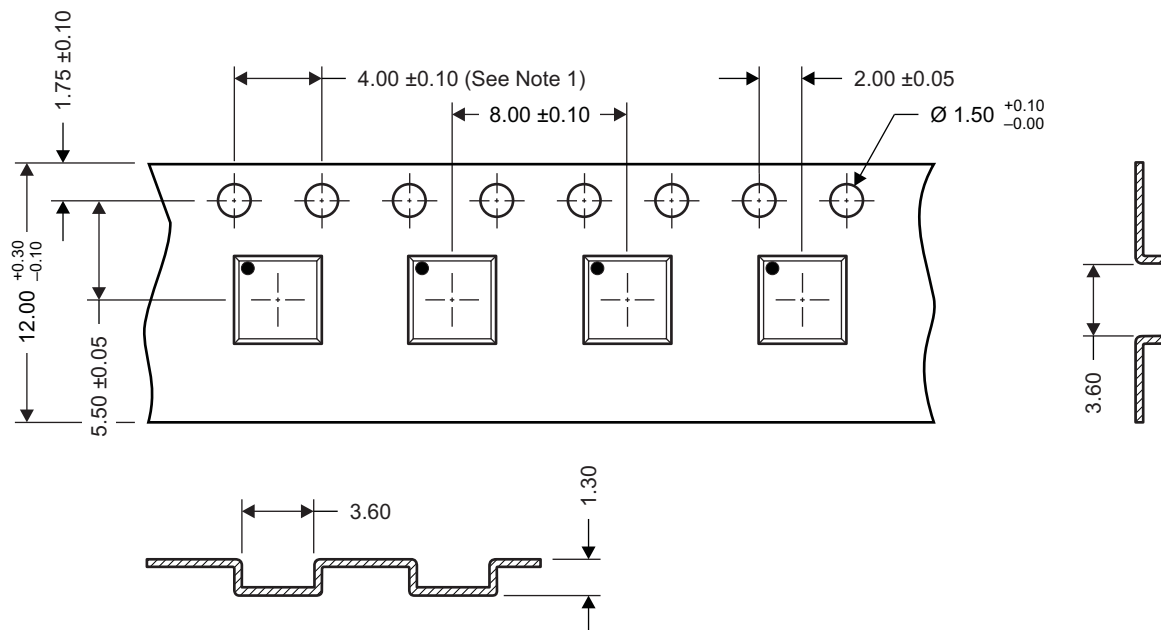
## Recommended PCB Pattern



## Recommended Stencil Opening



## Tape and Reel Information



M0144-01

### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness:  $0.30 \pm 0.05$ mm
6. MSL1 260°C (IR and Conection) PbF Reflow Compatible

## REVISION HISTORY

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### Changes from Original (August 2009) to Revision A Page

- Changed 300s to 300μs in Note 2 of the Abs Max Ratings table ..... [1](#)
  - Changed Q<sub>g</sub> Gate Charge Total (4.5V) - max value From: 2.3 To: 12.3 ..... [2](#)
- 

### Changes from Revision A (October 2009) to Revision B Page

- Deleted the Package Marking Information section ..... [8](#)
- 

### Changes from Revision B (October 2010) to Revision C Page

- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table ..... [2](#)
  - Changed the CSD25401Q3 Package Dimensions section ..... [6](#)
  - Changed the Recommended PCB Pattern section ..... [7](#)
-

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25401Q3	OBSOLETE	VSON-CLIP	DQG	8		TBD	Call TI	Call TI	-55 to 150	CSD25401	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### Applications

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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