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GreenChip III TEA1751: integrated PFC and flyback controller

Rev. 1.1 — 4 September 2013 **Application note**

Document information

Info	Content
Keywords	GreenChip III, TEA1751, PFC, flyback, high efficiency, adaptor, notebook, PC Power
Abstract	The TEA1751 is a member of the new generation of PFC and flyback controller combination ICs, used for efficient switched mode power supplies. It has a high level of integration which allows the design of a cost effective power supply with a very low number of external components. The TEA1751 is fabricated in a Silicon-On-Insulator (SOI) process. The NXP SOI process makes a wide voltage range possible.

Revision history

Rev	Date	Description
v.1.1	20130904	updated issue
Modifications:		• Section 7 “PCB layout considerations” has been updated.
v.1	20090210	first issue

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1. Introduction

The TEA1751 is a combination controller with a PFC and flyback controller integrated in to an SO-16 package. Both controllers operate in Quasi Resonant (QR) / Discontinuous Conduction Mode (DCM) mode with valley detection. The switching is independent for each controller.

The PFC output power is on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage. The flyback output power is Current mode controlled for good suppression of input voltage ripple.

The communication circuitry between both controllers is integrated and no adjustment is needed.

The voltage and current levels mentioned in this application note are typical values. A detailed description of the pin level spreading can be found in the *TEA1751 data sheet*.

1.1 Scope

This application note describes the functionality and the control functions of TEA1751 and the adjustments needed within the power converter application.

For the large signal parts of the PFC and flyback power stages, the design and data for the coil and transformer are dealt with in a separate application note.

1.2 The TEA1751 GreenChip III controller

The features of the GreenChip III allow the power supply engineer to design a reliable and cost-effective and efficient switched mode power supply with the minimum number of external components.

1.2.1 Key features

- PFC and flyback controller integrated in one SO-16 package
- Switching frequency of PFC and flyback are independent of each other
- No external hardware required for communication between the two controllers
- High level of integration, resulting in a very low external component count
- Mains voltage enable and brownout protection integrated
- Fast latch reset function implemented

1.2.2 System features

- Safe Restart mode for system fault conditions
- High-voltage start-up current source (5.4 mA)
- Reduction of HV current source (1 mA) in Safe restart mode
- Wide V_{CC} range (38 V)
- MOSFET driver voltage limited
- Easy controlled start-up behavior and V_{CC} circuit
- General-purpose input for latched protection
- Internal IC overtemperature protection

- Two high-voltage spacers between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL and FBAUX pins

1.2.3 PFC features

- Dual output voltage boost converter
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- T_{on} controlled
- Mains input voltage compensation for control loop for good transient response
- Over current protection (OCP)
- Soft start and soft stop
- Open / short detection for PFC feedback loop: no external OVP circuit necessary

1.2.4 Flyback features

- QR / DCM operation with valley switching
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- Current mode controlled
- Overcurrent protection (OCP)
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels without audible noise
- Soft start
- Accurate OverVoltage Protection (OVP) through auxiliary winding
- Time-out protection for output overloads and open flyback feedback loop, available as safe restart (TEA1751T) or latched (TEA1751LT) protection

1.3 Application schematic

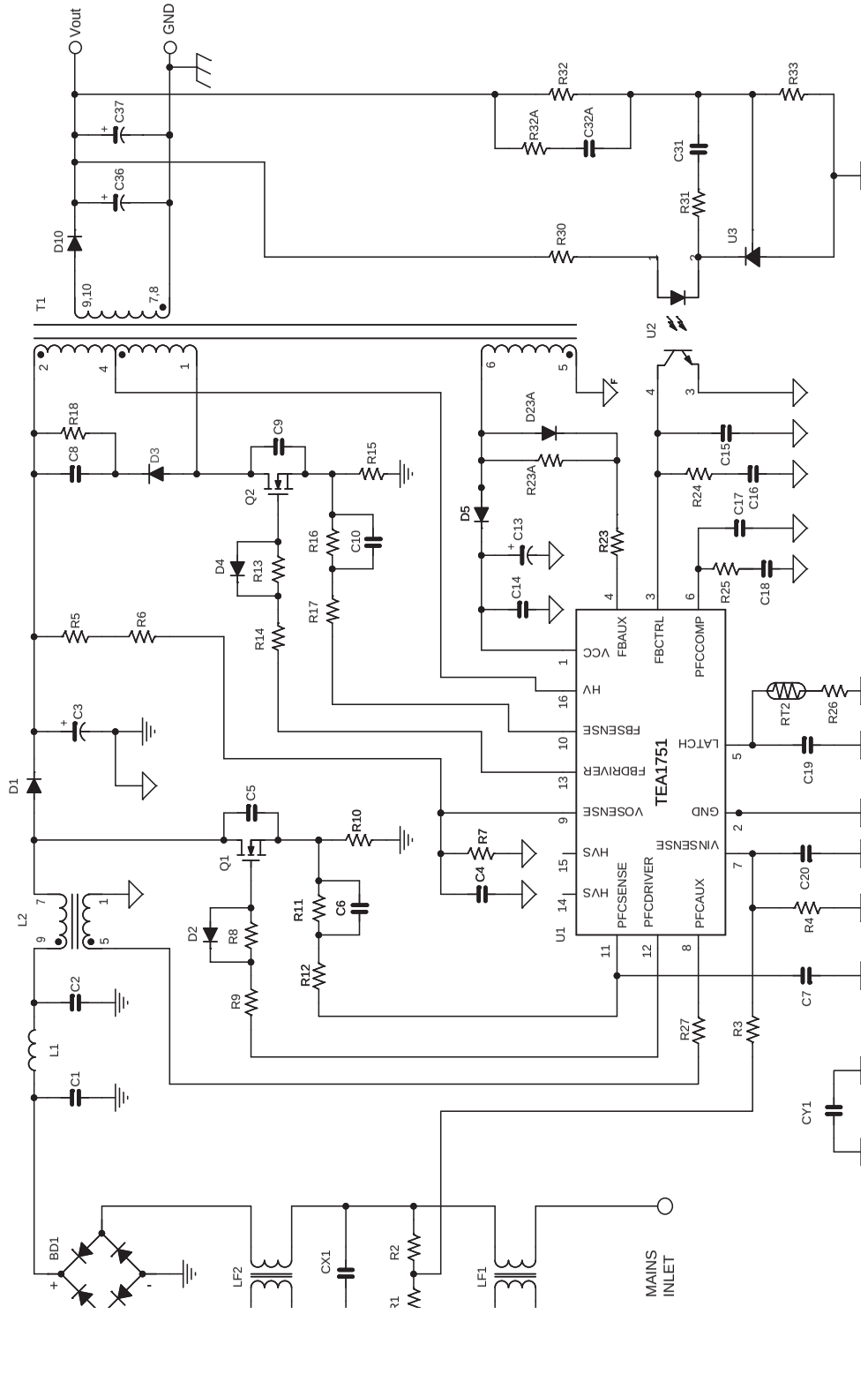


Fig 1. Application schematic

2. Pin description

Table 1. Pin descriptions

Pin	Name	Functional description
1	V_{CC}	Supply voltage: $V_{startup}$ = 22 V, $V_{th(UVLO)}$ = 15 V. At mains switch-on, the capacitor connected to this pin is charged to V_{CC} start by the internal HV current source. When the pin voltage is lower than 0.65 V, the charge current is limited to 1 mA, this to prevent overheating of the IC if the V_{CC} pin is short circuited. When the pin voltage is between 0.65 V and $V_{th(UVLO)}$, the charge current is 5.4 mA to enable a fast start-up. Between $V_{th(UVLO)}$) and $V_{startup}$, the charge current is again limited to 1 mA, this to reduce the safe restart duty cycle and as a result the input power during fault conditions. At the moment $V_{startup}$ is reached the current source is pinched-off, and V_{CC} is regulated to $V_{startup}$ until the flyback starts. See Section 3.2 for a complete description of the start-up sequence.
2	GND	Ground connection.
3	FBCTRL	Control input for flyback for direct connection of the optocoupler. At a control voltage of 2 V the flyback delivers maximum power. At a control voltage of 1.5 V the flyback enters the frequency reduction mode and the PFC is switched off. At 1.4 V the flyback stops switching. Internal there is a 30 mA current source connected to the pin, which is controlled by the internal logic. This current source can be used to implement a time-out function to detect an open control-loop or a short circuit of the output-voltage. The time-out function can be disabled with a resistor of 100 kΩ between this pin and ground.
4	FBAUX	Input from auxiliary winding for transformer demagnetization detection, mains dependent overpower protection (OPP) overvoltage protection (OVP) of the flyback. The combination of the demagnetization detection and the valley detection at pin HV is determining the switch-on moment of the flyback in the valley. A flyback OVP is detected at a current > 300 μA into the FBAUX pin. Internal filtering is present to prevent false detection of an OVP. The flyback OPP starts at a current < −100 μA out of the FBAUX pin.
5	LATCH	General purpose latched protection input. When $V_{startup}$ (pin 1) is reached, this pin is charged to a voltage of 1.35 V first before the PFC is enabled. To trigger the latched protection, the pin must be pulled down to below 1.25 V. An internal 80 μA current source is connected to the pin, which is controlled by the internal logic. Because of this current source, an NTC resistor for temperature protection can be directly connected to this pin.
6	PFCCOMP	Frequency compensation pin for the PFC control loop.

Table 1. Pin descriptions *…continued*

Pin	Name	Functional description
7	VINSENSE	Sense input for mains voltage. This pin has 5 functions: • mains enable level: $V_{start(VINSENSE)}$ = 1.15 V • mains stop level (brownout): $V_{stop(VINSENSE)}$ = 0.9 V • mains voltage compensation for the PFC control-loop gain bandwidth • fast latch reset: V_{flr} = 0.75 V • dual boost switch-over point: $V_{bst(DUAL)}$ = 2.2 V The mains enable and mains stop level enable and disable the PFC. The voltage at the VINSENSE pin must be an averaged DC value, representing the AC line voltage. The pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. The auxiliary winding must be connected by a 5 kΩ series resistor to prevent damage of the input due to lightning surges.
9	VOSENSE	Sense input for output voltage of the PFC. VOSENSE pin, open loop and short detection: $V_{th(ol)(VOSENSE)}$ =1.15 V Regulation of PFC output voltage: $V_{reg(VOSENSE)}$ = 2.5 V PFC soft OVP (cycle-by-cycle): $V_{ovp(VOSENSE)}$ = 2.63 V Control output for output voltage of the PFC, - dual boost current: $I_{bst(DUAL)}$ = −15 μA
10	FBSENSE	Current sense input for flyback. At this pin, the voltage across the flyback current sense resistor is measured. The setting of the sense level is determined by the FBCTRL voltage, using the equation: $V_{FBSENSE} = 0.75 \times V_{FBCTRL} - 1\ V$ The maximum setting level for $V_{FBSENSE}$ = 0.5 V. Internal there is a 60 μA current source connected to the pin, which is controlled by the internal logic. The current source is used to implement a soft start function for the flyback and to enable the flyback. The flyback only starts when the internal current source is able to charge the soft start capacitor to a voltage of more than 0.5 V. Therefore a minimum soft start resistor of 12 kΩ is required to guarantee the enabling of the flyback.
11	PFCSENSE	Overcurrent protection input for PFC. This input is used to limit the maximum peak current in the PFC core. The PFCSENSE is a cycle-by-cycle protection, at 0.5 V the PFC MOSFET is switched off. There is an internal 60 μA current-source connected to the pin, which is controlled by the internal logic. This current source is used to implement a soft start and soft stop function for the PFC, this to prevent audible noise in PFC burst mode. This pin is also used for enabling of the PFC. The PFC only starts when the internal current source is able to charge the soft start capacitor to a voltage of more than 0.5 V. Therefore a minimum soft start resistor of 12 kΩ is required to guarantee the enabling of the PFC.
12	PFCDRIVER	Gate driver output for PFC MOSFET.
13	FBDRIVER	Gate driver output for flyback MOSFET.

Table 1. Pin descriptions *…continued*

Pin	Name	Functional description
14	HVS	High-voltage safety spacer, not connected
15	HVS	High-voltage safety spacer, not connected
16	HV	High-voltage input for internal start-up current source (output at pin 1), and valley sensing of the flyback. The combination of the demagnetization detection at the FBAUX pin and the valley detection at the HV pin determine the switch-on moment of the flyback in the valley.

3. System description and calculation

3.1 PFC and flyback start conditions

Figure 2 and Figure 3 show the conditions for enabling of the PFC and flyback are given. If start-up problems occur these conditions can be checked to find the cause of the problem. Some of the conditions are dynamic signals (see Figure 4) and should be checked with an oscilloscope.

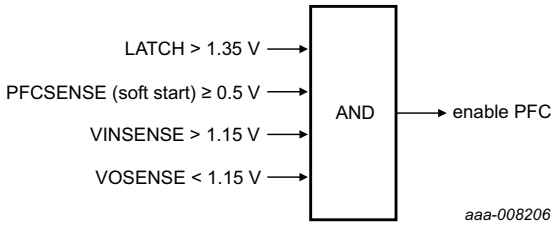


Fig 2. PFC start condition

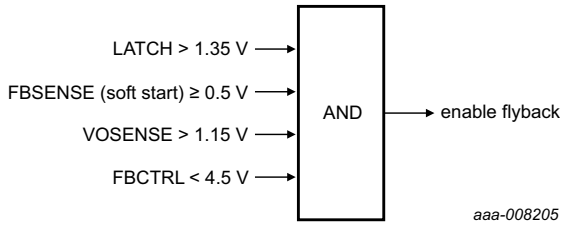


Fig 3. Flyback start condition

3.2 Start-up sequence

At switch-on with a low mains voltage, the TEA1751(L)T power supply has the following start-up sequence (see Figure 4):

1. The HV current source is set to 0.9 mA and the V_{CC} electrolytic capacitor is charged to 0.65 V; this to detect a possible short circuit at pin V_{CC}.
2. At V_{CC} = 0.65 V, the HV current source is set to 5.4 mA and the V_{CC} electrolytic capacitor is fast charged to $V_{TH(UVLO)}$.
3. At $V_{CC} = V_{TH(UVLO)}$, the HV current source is set to 0.9 mA again and the V_{CC} electrolytic capacitor is charged further to $V_{startup}$.
4. At $V_{startup}$, the HV current source is switched off and the 80 μA LATCH pin current source is switched on to charge the LATCH pin capacitor. At the same time, the PFCSENSE and FBSENSE soft start current sources are switched on.
5. When the LATCH pin is charged up to 1.35 V the PFC and flyback can start switching, but only when the VINSENSE pin has reached a level of 1.15 V.
6. For the PFC also the soft start capacitor at pin PFCSENSE must be charged up to 0.5 V. The voltage at the VOSENSE pin must be greater than 1.15 V.

7. For the flyback also the soft start capacitor at pin FBSENSE must be charged up to 0.5 V and the voltage at the FBCTRL pin must be less than 4.5 V. Normally, the voltage at the FBCTRL pin is always less than 4.5 V at the first flyback switching cycle, unless the FBCTRL pin is open. At the moment that the flyback starts, the FBCTRL time-out current source is switched on.
8. When the flyback has reached its nominal output voltage, the V_{CC} supply of the IC is taken over by the auxiliary winding. If, for any reason, the flyback feedback loop signal is missing, then the time-out protection at the FBCTRL pin is triggered and both converters the PFC and the flyback are switched off, VCC drops to $V_{TH(UVLO)}$, and the IC continues with step 3 of the start-up cycle. This is the safe restart cycle.

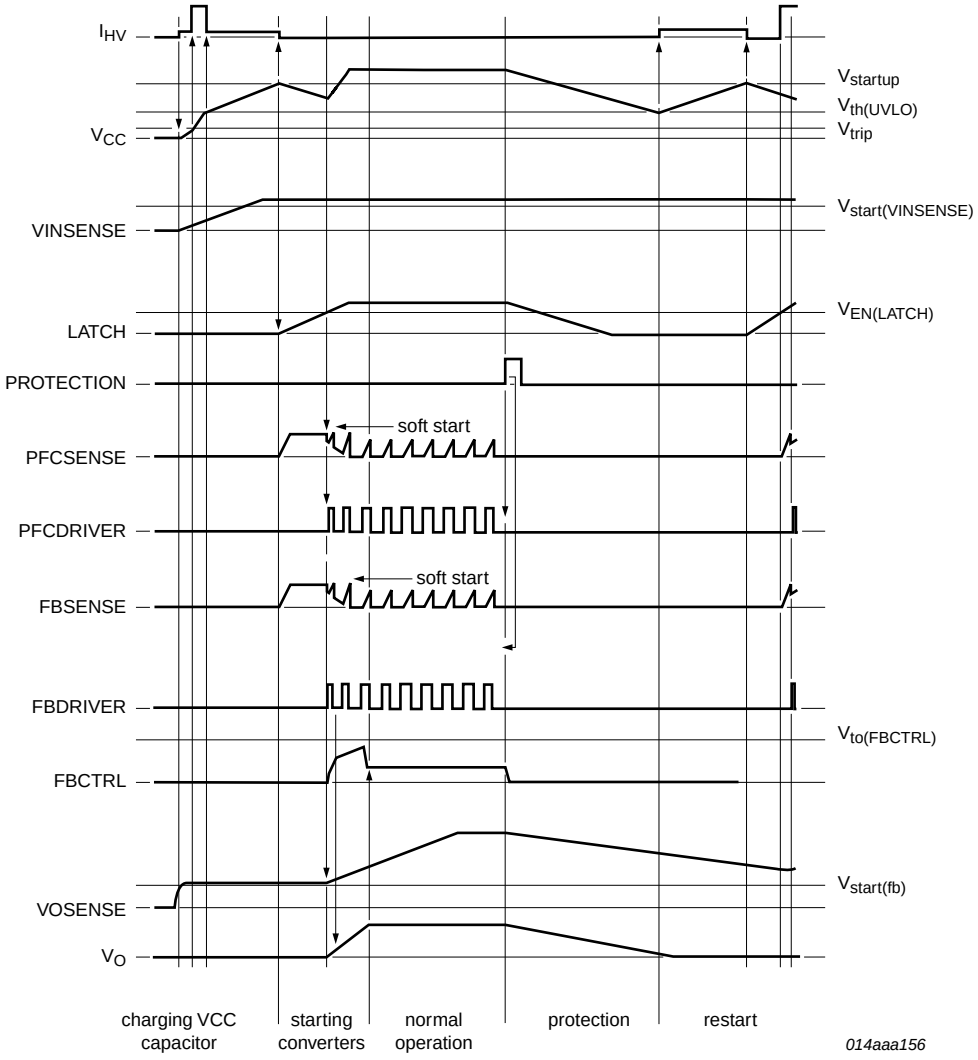


Fig 4. Start-up sequence at low mains voltage

The charge time of the soft start capacitors can be chosen by their values independently for the PFC and the flyback. This way it can be realized that the PFC starts before the flyback.

3.3 V_{CC} cycle at safe restart protections

In Safe restart mode, the controller goes through the steps 3 to 8 as described in Section 3.2.

3.4 Mains voltage sensing and brownout

The mains input voltage is measured through the VINSENSE pin. When the VINSENSE pin has reached the $V_{start(VINSENSE)}$ level of 1.15 V the PFC can start switching, but only if the other start conditions are met as well, see Section 3.1. As soon as the voltage at pin VINSENSE drops below the $V_{stop(VINSENSE)}$ level of 0.89 V, the PFC stops switching. The flyback however, continues switching until the flyback maximum on-time protection, $t_{on(fb)max}$ (40 μs) is triggered. When this protection is triggered, the IC stops switching and enters the safe restart mode.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimal with a time constant of approximately 150 ms at the VINSENSE pin. The long time constant at the VINSENSE pin prevents a fast restart of the PFC after a mains drop-out, therefore the voltage at the VINSENSE pin is clamped to a level of 100 mV below the $V_{start(VINSENSE)}$ level, this to guarantee a fast PFC restart after recovery of the mains input voltage.

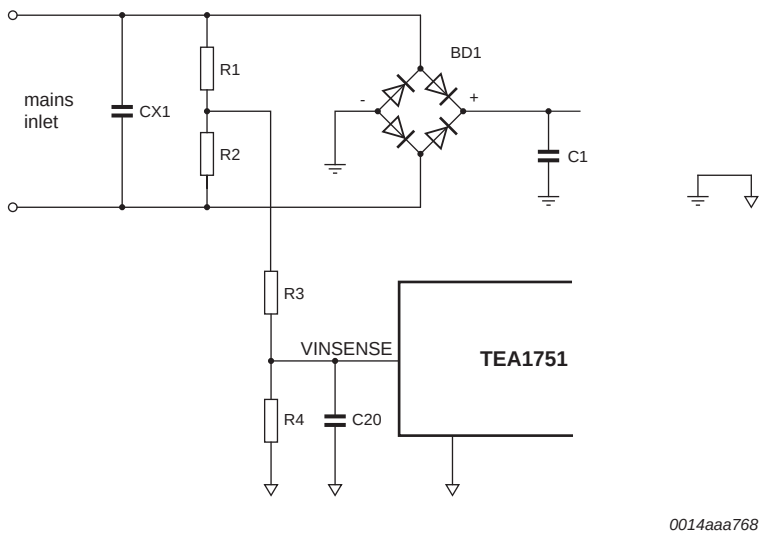


Fig 5. VINSENSE circuitry

3.4.1 Discharge of mains input capacitor

For safety, according to Ref. 1, the X-capacitors in the EMC input filtering must be discharged with a time constant $\tau < 1$ s.

The R to discharge the X-cap in the input filtering, is determined by the replacement value of R1+ R2.

In a typical 90 W adapter application with CX1 = 220 nF, the replacement value of R1 + R2 must be smaller than or equal to the following:

$$R_V \leq \frac{\tau}{C} = \frac{1}{220\ nF} = 4.55\ M\Omega \quad (1)$$

3.4.2 Brownout voltage adjustment

The rectified AC input voltage is measured via R1 and R2. Each resistor alternately senses half the sine wave, so both resistors must have the same value. The average voltage sensed at the connection of R1 and R2 is as follows:

$$V_{avg} = \frac{2\sqrt{2}}{\pi} \cdot V_{acrms} \quad (2)$$

The V (AC) brownout RMS level is calculated as follows:

$$V_{acbrownout} = \frac{\pi}{2\sqrt{2}} \cdot V_{stop(VINSENSE)} \cdot 2 \cdot \frac{R1 \cdot R2}{\left(\frac{R1 + R2}{R4} + 1\right)} + R3 \quad (3)$$

For a brownout threshold of 68 V (AC) and compliance with Ref. 1. Example values are shown in Table 2.

Table 2. VINSENSE component values

CX1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A value of 3.3 μF for capacitor C20, with 47 kΩ at R4, gives the recommended time constant of ~150 ms at the VINSENSE pin.

3.5 Internal OTP

The IC has an internal temperature protection to protect the IC from overheating by overloads at the V_{CC} pin. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching. As long as the OTP is active, the V_{CC} capacitor is not recharged from the HV mains. The OTP circuit is supplied from the HV pin if the V_{CC} supply voltage is not sufficient. The OTP is a latched protection.

3.6 LATCH pin

The LATCH pin is a general-purpose input pin, which can be used to latch off both converters. The pin sources a bias current $I_{o(LATCH)}$ of 80 μA for the direct connection of an NTC. When the voltage on this pin is pulled below 1.25 V, switching of both converters is immediately stopped. V_{CC} starts cycling between the $V_{TH(UVLO)}$ and $V_{startup}$, without a restart. Switching off and then switching on the mains input voltage trigger the fast latch reset circuit, and reset the latch.

At start-up, the latch pin first must be charged above 1.35 V, before both converters are enabled. Charging of the LATCH pin starts at $V_{startup}$.

No internal filtering is present at the LATCH pin. A 10 nF capacitor must be placed between this pin and IC GROUND pin to prevent false triggering, also when the LATCH pin function is not used.

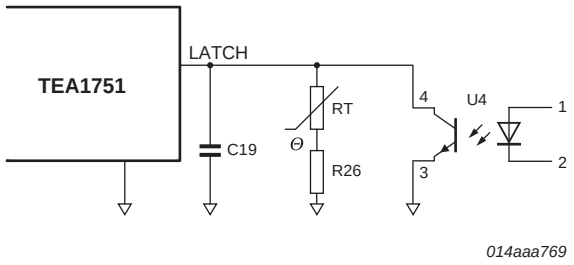


Fig 6. Usage of the LATCH pin protection

Latching on application over temperature occurs when the total resistance value of the NTC and its series resistor drops below the following:

$$R_{OTP} = \frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = \frac{1.25\ V}{80\ \mu A} = 15.6\ k\Omega \quad (4)$$

The optocoupler triggers the latch if the driven optotransistor conducts more than 80 μA.

3.7 Fast latch reset

Switching off and then switching on the mains input voltage, can reset the latched protection. After the mains input is switched off, the voltage at the VINSENSE pin will drop below V_{FLR} (0.75 V). This triggers the fast latch reset circuit, but does not reset the latched protection. After the mains input is switched on, the voltage at the VINSENSE pin will rise again, and when the level has passed 0.85 V, the latch will be reset. The system restarts again when the V_{CC} pin is charged to $V_{startup}$. See step 4 of Section 3.2.

4. PFC description and calculation

The PFC operates in Quasi Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 125 kHz to reduce the switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

The PFC of the TEA1751(L)T is designed as a dual boost converter with two output voltage levels that are dependent on the mains input voltage range. The advantage of such a dual boost is that the overall system efficiency at low mains can be improved due to reduction of the PFC switching losses. In low and medium power adapters (< 120 W) the contribution of PFC switching losses to the total losses are relative high.

The dual output voltage is controlled through an internal current source of 15 μA at pin VOSENSE. As shown in Figure 7, the mains input voltage measured at pin VINSENSE is used to control the internal current source. This current-source in combination with the resistors at pin VOSENSE sets the lower PFC output voltage. At high mains, the current-source is switched off. Therefore, the maximum PFC output voltage is not effected by the accuracy of the current-source. In a typical adapter with a PFC output voltage of

385 V (DC) at high mains, the PFC output voltage is 250 V (DC) at low mains. A voltage of 2.2 V at pin VINSENSE corresponds with a mains input voltage of approximately 180 V (AC). The small slope at the transfer function ensures stable switch over of the PFC output voltage without hiccups.

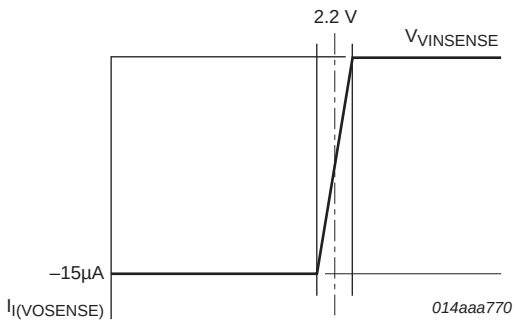


Fig 7. Transfer function of VINSENSE voltage to dual boost current at VOSENSE

At low output loads, the PFC is switched off to ensure a high efficiency, and a low no-load standby input power. After switch off, the bulk electrolytic capacitor voltage drops to Vac × √2.

4.1 PFC output power and voltage control

The PFC of the TEA1751(L)T is on-time controlled, therefore it is not necessary to measure the mains phase angle. The on-time is kept constant during the half sine wave to obtain a good power factor (PF), and a class-D Mains Harmonics Reduction (MHR) (see Ref. 2).

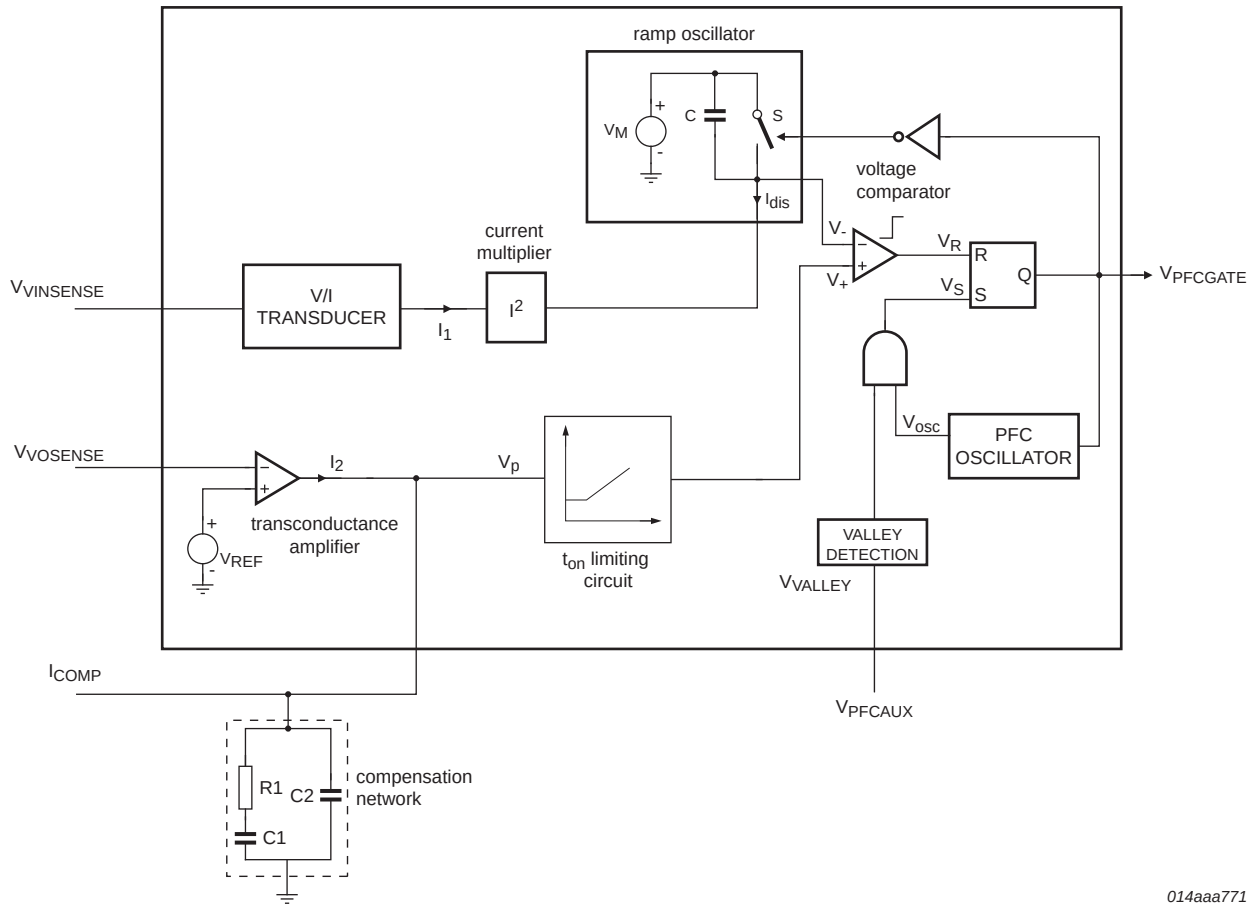


Fig 8. PFC on-time control

To stabilize the PFC control loop, a network with one resistor and two capacitors at the PFCCOMP pin is used. The mathematical equation for the transfer function of a boost converter contains the square of the mains input voltage. In a typical application this results in a low regulation bandwidth for low mains input voltages and a high regulation bandwidth at high input voltage, while at high mains input voltages it can be difficult to meet the MHR requirements. The TEA1751(L)T uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as function of the mains input voltage. As a result the gain is constant over the entire mains input voltage range.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimal with a time constant of approximately 150 ms at the VINSENSE pin.

4.1.1 Setting the PFC output voltage

The PFC output voltage is set with a resistor divider between the PFC output voltage and the VOSENSE pin. In PFC Normal mode, the PFC output voltage is regulated so that the voltage on the VOSENSE pin is equal to $V_{reg(VOSENSE)}$ = 2.5 V.

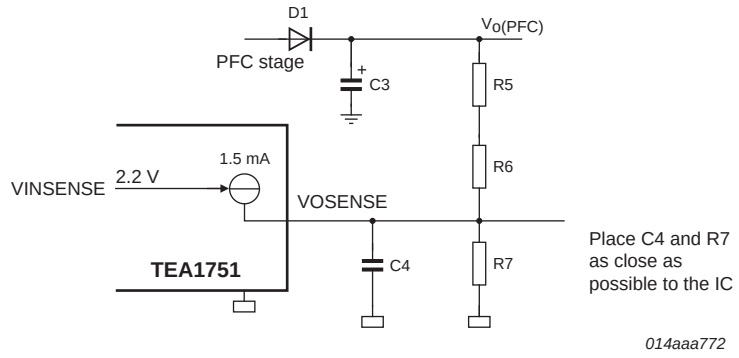


Fig 9. PFC output voltage setting

For low no-load input power two resistors of 4.7 MΩ (1 %) can be used between the bulk electrolytic capacitor and the VOSENSE pin. The dimensioning of the $I_{bst(DUAL)}$ current source (−15 μA) has been adapted to the usage of these resistor values. With a resistor value of 4.7 MΩ for R5 and R6 and 60 kΩ to 62 kΩ for R7, a universal mains adapter has a PFC output voltage of approximately 380 V to 390 V at high mains and 240 V to 250 V at low mains.

The resistor R7 (1 %) between the VOSENSE pin and ground can be calculated with equation:

$$R7 = \frac{(R5 + R6) \times V_{reg(VOSENSE)}}{(V_{O(PFC)} - V_{reg(VOSENSE)})} \quad (5)$$

Suppose that the regulated PFC output voltage is 382 V, then:

$$R7 = \frac{(4.7\ M\Omega + 4.7\ M\Omega) \times 2.5\ V}{(382\ V - 2.5\ V)} = 62\ k\Omega\ (1\ \%)$$

At low mains, the 15 μA current source $I_{bst(DUAL)}$ is active. The lower PFC output voltage can be calculated with Equation 6:

$$V_{O(PFC)LOW} = \frac{R5 + R6 + R7}{R7} \cdot (V_{reg(VOSENSE)} - I_{bst(DUAL)} \cdot R7) \quad (6)$$

With 4.7 MΩ for R5 and R6 and 62 kΩ for R7 the lower PFC output voltage is calculated as follows:

$$V_{O(PFC)LOW} = \frac{4.7\ M\Omega + 4.7\ M\Omega + 62\ k\Omega}{62\ k\Omega} \cdot (2.5\ V - 15\ \mu A \cdot 62\ k\Omega) = 240\ V$$

The function of the capacitor C4 at the VOSENSE pin is to filter noise and to prevent false triggering of the protections, due to MOSFET switching noise, mains surge events or ESD events. False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current. False triggering of the $V_{th(ol)(VOSENSE)}$ protection causes a safe restart cycle. A time constant of 500 ns to 1 ms, at the VOSENSE pin should be sufficient, which results in a value of 10 nF for capacitor C4.

Place R7 and C4 as close as possible to the IC between the VOSENSE pin and the IC ground pin.

4.1.2 Calculation of the PFC soft start and stop components

The soft start and stop are implemented through the RC network at the PFCSENSE pin.

Rss1 must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the PFC. See Section 3.1 for start-up description.

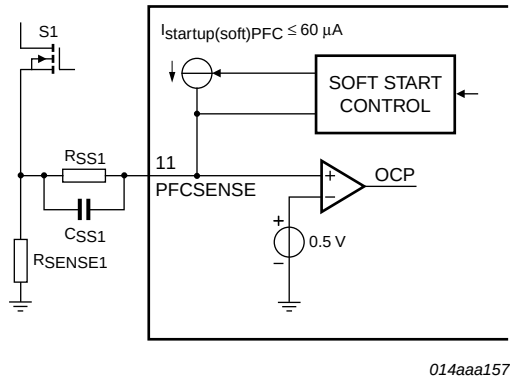


Fig 10. PFC soft start

The total soft start or soft stop time is equal to: $t_{softstart} = 3Rss1 \cdot Css1$

Keep the soft start time of the PFC smaller than the soft start time of the flyback to ensure that the PFC starts before the flyback at initial start-up. It is also advised that the soft start time is kept within a range of 2 ms to 5 ms.

With C8 = 100 nF and R11 = 12 kΩ, the total soft start time is 3.6 ms.

4.2 PFC demagnetizing and valley detection

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. To reduce switching losses and electromagnetic interference (EMI) (valley switching) the next stroke is started if the voltage across the PFC MOSFET is at its minimum.

The maximum switching frequency of the PFC is limited to 125 kHz to reduce the switching losses. One or more valleys are skipped, when necessary, to keep the frequency below 125 kHz.

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 ms after the last PFC gate signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal 4 µs after demagnetization was detected.

In some applications, the PI filter before the PFC inductor can start oscillating when the PFC switching frequency is close to the third harmonic of the PI filter resonance frequency. This can lead to false PFC valley detection. As a result, the PFC can run in Continuous conduction mode. False detection can be suppressed by placing a diode between the IC ground and the PFCAUX pin.

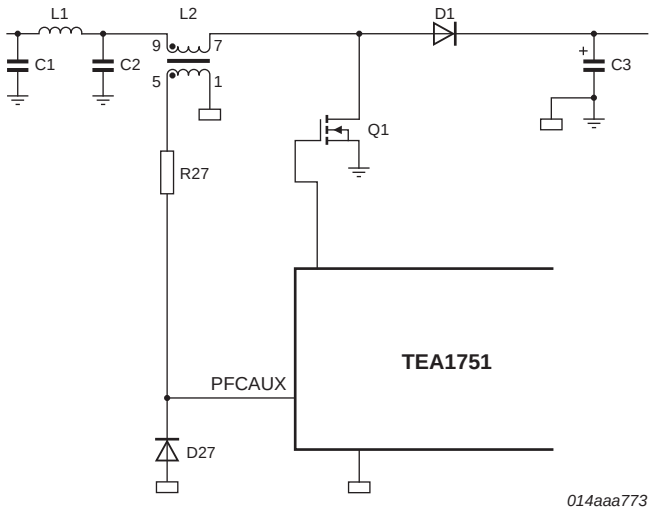


Fig 11. PFCAUX circuitry

4.2.1 Design of the PFCAUX winding and circuit

To guarantee valley detection at low ringing amplitudes, the voltage at the PFCAUX pin must be set as high as possible, taking into account its absolute maximum rating of ±25 V.

The number of turns of the PFCAUX winding can be calculated as follows:

$$N_{a(max)} = \frac{V_{PFC(AUX))}}{V_{L(max)}} \times N_p = \frac{25\ V}{V_{L(max)}} \times N_p \quad (7)$$

Where: VPFCAUX is the absolute maximum rating of the PFCAUX pin, and $V_{L(max)}$ is the maximum voltage across the PFC primary winding. The PFC output voltage at the PFCOVP level determines the maximum voltage across the PFC primary winding and can be calculated with equation:

$$V_{L(max)} = \frac{V_{OVP(VOSENSE)}}{V_{reg(VOSENSE)}} \times V_{O(PFC)} = \frac{2.63\ V}{2.5\ V} \times V_{O(PFC)} \quad (8)$$

When a PFC coil with a higher number of auxiliary turns is used, then a resistor voltage divider can be placed between the auxiliary winding and pin PFCAUX. The total resistive value of the divider should be less than 10 kΩ to prevent delay of the valley detection by parasitic capacitance.

The polarity of the signal at the PFCAUX pin must be reversed compared to the PFC MOSFET drain signal.

To protect the PFCAUX pin against electrical overstress, for example during lighting surge events, put a 5 kΩ resistor between the PFC auxiliary winding and this pin. To prevent incorrect valley switching of the PFC due to external disturbance, the resistor should be placed close to the IC.

4.3 PFC protections

4.3.1 VOSENSE OverVoltage Protection (OVP)

At start-up or at the transition from PFC Burst mode to PFC Normal mode, a voltage overshoot can occur at the boost electrolytic capacitor. This overshoot is caused by the relative slow response of the PFC control loop. The PFC control loop response must be relatively slow to guarantee a good power factor and meet the MHR requirements. The OverVoltage Protection (OVP) at the VOSENSE pin limits the overshoot. At the moment that the $V_{OVP(VOSENSE)}$ level of 2.63 V is detected, the PFC MOSFET is switched off immediately, regardless of the on-time setting. The switching of the MOSFET remains blocked until the voltage at the VOSENSE pin drops below 2.63 V again.

When the resistor between the VOSENSE pin and ground is open, the OVP is also triggered.

The peak voltage at the boost electrolytic capacitor generated by the PFC due to an overshoot and limited by the PFC OVP can be calculated with the equation:

$$V_{O(PFC\_peak)} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot V_{O(PFC\_nominal)} = \frac{2.63\ V}{2.5\ V} \cdot V_{O(PFC\_nominal)} \quad (9)$$

4.3.2 VOSENSE open and short pin detection

The VOSENSE pin, which is sensing the PFC output voltage, has integrated protection circuitry to detect an open and short-circuited pin. This pin can also sense if one of the resistors in the voltage divider is open. Therefore the VOSENSE pin is fail-safe. It is not necessary to add an external OVP circuit for the PFC. An internal current source pulls down the pin below the $V_{th(ol)(VOSENSE)}$ detection level of 1.15 V, when the pin is open. At detection of the $V_{th(ol)(VOSENSE)}$ level switching of the PFC MOSFET is blocked until the voltage at the VOSENSE pin rises above 1.15 V again.

4.3.3 VINSENSE open pin detection

The VINSENSE pin, which senses the mains input voltage, has an integrated protection circuit to detect an open pin. An internal current source pulls down the pin below the $V_{stop(VINSENSE)}$ level of 0.9 V, when the pin is open.

4.3.4 OverCurrent Protection (OCP)

An OverCurrent Protection (OCP) limits the maximum current through the PFC MOSFET and PFC coil. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET is switched off immediately when the voltage at pin PFCSENSE exceeds the $V_{sense(PFC)max}$ level of 0.52 V. The OCP is a switching cycle-by-switching cycle protection.

To avoid false triggering of the PFC OCP by switching of the flyback, keep a margin of 0.1 V into account. False triggering of the $V_{OVP(VOSENSE)}$ protection can cause disturbance of the AC mains input current. It is also advised that a small capacitor of 100 pF to 220 pF is placed directly at the PFCSENSE pin to any suppress external disturbance.

The current sense resistor can be calculated as follows:

$$R_{OCP(PFC)} = \frac{V_{sense(PFC)max} - V_{margin}}{Ip_{QR(PFC)max}} = \frac{0.52\ V - 0.1\ V}{Ip_{QR(PFC)max}} \quad (10)$$

Where: $Ip_{QR(PFC)max}$ is the maximum PFC peak current at the high load and low mains.

For the PFC operating in Quasi Resonant mode the maximum peak current can be calculated with equation:

$$Ip_{QR(PFC)max} = \frac{2\sqrt{2} \cdot Pi_{max} \cdot 1.1}{Vac_{max}} = \frac{2\sqrt{2} \cdot \frac{Po_{max}}{\eta} \cdot 1.1}{Vac_{max}} \quad (11)$$

Where:

- Po_{max} is the maximum output power of the flyback
- 1.1 is a factor to compensate for the dead time between zero current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in QR mode
- η is the expected efficiency of the total converter at maximum output power
- Vac_{min} is minimum mains input voltage

5. Flyback description and calculation

The flyback of the TEA1751(L)T is a variable frequency controller that can operate in Quasi Resonant (QR) or Discontinuous Conduction mode with demagnetization detection and valley switching.

The setting of the primary peak current controls the output power; the switching frequency is a result. The primary peak current is set through the voltage at the FBCTRL pin and measured back at the FBSENSE pin with the following relationship:

$$V_{sense(FB)} \cong 0.75 \times V_{FBCTRL} - 1\ V \quad (12)$$

The flyback controls the operational mode of the PFC. At low output powers, when the primary peak current, $Ip \leq 0.25 \times Ip_{max}$ the PFC is switched off.

Demagnetization of the flyback transformer is detected through pin FBAUX, connected to the auxiliary winding. The valley is detected through the HV pin, which can be connected to the MOSFET drain or to the center tap of the primary winding.

The input voltage of the flyback is measured through pin FBAUX and used to implement and OverPower Protection (OPP). The OPP keeps the maximum output power of the flyback constant over the input voltage.

The flyback has an accurate OverVoltage Protection (OVP) circuit. The overvoltage is measured, through pin FBAUX. Both controllers are switched off in a latched protection when an overvoltage is detected.

5.1 Flyback output power control

An important aspect of the TEA1751(L)T flyback system is, that the setting of the primary peak current controls the output power. The switching frequency is a result of external application parameters and internal IC parameters.

External application parameters are the transformer turns ratio, the primary inductance, the drain source capacitance, the input voltage, the output voltage and the feedback signal from the control loop. Internal IC parameters are the oscillator setting, the setting of the peak current and the detection of demagnetization and valley.

The output power of flyback can be described with the equation:

$$P_o = \frac{1}{2} \cdot L_p \cdot L_p{}^2 \cdot f_s \cdot \eta \quad (13)$$

At initial start-up, the flyback always starts at the maximum output power. From maximum to minimum output power, the flyback goes through the three operation modes as shown Figure 12.

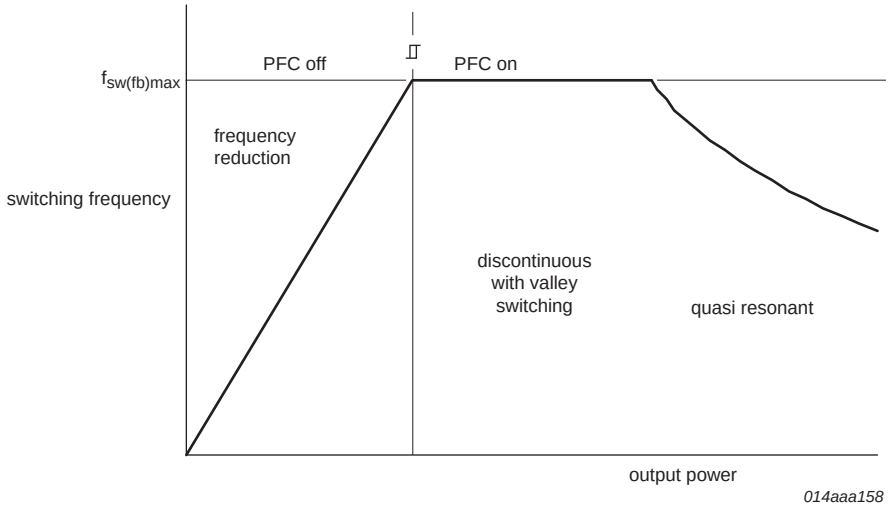


Fig 12. Operation modes flyback

At maximum output power, limited by the flyback current sense resistor, the flyback operates in Quasi Resonant (QR) mode. The next primary switching cycle starts at detection of the first valley.

By reducing the peak current, the output power is reduced and as a result the switching frequency goes up. When the maximum flyback switching frequency is reached and the output power still must be reduced, the flyback goes from QR into Discontinuous mode (DCM) with valley switching.

In DCM, the output power is reduced by further reduction of the peak current and at the same time skipping of one or more valleys. In this mode, the switching frequency is kept constant. The exact switching frequency however, depends on the detection of the valley but is never higher as the maximum frequency.

The minimum flyback peak current: $Ip_{min} = 0.25 \times Ip_{max}$. At this point, the flyback enters the Frequency Reduction mode and the PFC is set in Burst mode. In the Frequency Reduction mode, the peak current is kept constant. Increasing the off time reduces the output power.

Place a 10 nF noise filter capacitor (C15) as close as possible to the FBTRL pin to avoid disturbance of the flyback by switching of the PFC MOSFET.

5.1.1 Calculation of the flyback current sense resistor

The current sense resistor $R_{OCP(fb)}$ can be calculated with Equation 14:

$$R_{OCP(fb)} = \frac{V_{sense(fb)max}}{Ip_{QR(fb)max}} = \frac{0.52\ V}{Ip_{QR(fb)max}} \quad (14)$$

For the flyback operating in Quasi Resonant mode the peak current can be calculated with Equation 15:

$$Ip_{QR(fb)max} = \frac{2Po_{max} \cdot 1.1}{\eta \times Vdc_{min}} \times \frac{Vdc_{min} + \frac{N_p}{N_s} \cdot V_o}{\frac{N_p}{N_s} \cdot V_o} \quad (15)$$

Where:

- Po_{max} is the maximum output power of the flyback
- 1.1 is a factor that compensates for the dead time between zero current in the flyback transformer at the end of the secondary stroke and the detection of the first valley in QR mode
- η is the expected efficiency of the flyback at maximum output power

  Vdc_{min} is minimum bulk electrolytic capacitor voltage in PFC Burst mode as follows:

  $$Vdc_{min} = Vo_{PFC} \times \left(\frac{V_{burst(L)}}{V_{reg(VOSENSE)}} = Vo_{PFC} \right) \times \frac{1.92\ V}{2.5\ V}$$

- V_o is the output voltage
- N_p is the number of primary turns of the flyback transformer
- N_s is the number of secondary turns of the flyback transformer.

5.1.2 Calculation of the flyback soft start components

The soft start is implemented through the RC network at pin FBSENSE.

Rss1 must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the flyback. See Section 3.1 for start-up description.

The total soft start or soft stop time is equal to: $t_{softstart} = 3Rss \cdot Css$.

Make the soft start time for the flyback larger than the soft start time of the PFC, to ensure that the PFC starts before the flyback at initial start-up. It is also advisable to keep the soft start time in a range of 5 ms to 10 ms.

With C10 = 220 nF and R16 = 12 kΩ the total soft start time is 8 ms.

5.2 Flyback control of PFC Burst mode

The flyback controls the operation mode of the PFC. At low output powers, when the primary peak current $Ip \leq 0.25 \times Ip_{max}$, the PFC is switched off. This is the same point as when the flyback enters the Frequency Reduction mode, see Figure 12 and Section 4.1.

On the transition from PFC Normal mode to Burst mode and from Burst mode to Normal mode is a hysteresis of 60 mV on $V_{hys(FBCTRL)}$. This provides the possibility of smooth transitions for all applications. To guarantee a smooth transition from PFC off to PFC on and to avoid audible noise in flyback transformer, place the 10 nF noise filter capacitor C15 as close as possible to the FBTRL pin .

5.3 Flyback protections

5.3.1 Short circuit on the FBCTRL pin

If the pin is shorted to ground, switching of the flyback controller is inhibited. This situation is equal to the minimum, or a no output power situation.

5.3.2 Open the FBCTRL pin

As shown in Figure 13. the FBCTRL pin is connected to an internal voltage source of 3.5 V via an internal resistor of 3 kΩ. When the voltage on pin FBCTRL is above 2.5 V, this connection is disabled and the FBCTRL pin is biased with an internal 30 μA current source. When the voltage on the FBCTRL pin rises above $V_{to(FBCTRL)}$ of 4.5 V, a fault is assumed. Switching of the flyback (and also the PFC) is blocked and the controller enters the Safe Restart mode.

An internal switch pulls the FBCTRL pin down when the flyback is disabled.

5.3.3 Time-out flyback control-loop

A time-out function can be realized to protect for an output short circuit at initial start-up or for an open control loop situation. This can be done by placing a resistor in series with a capacitor between the FBCTRL pin and ground.

See Figure 13. Above 2.5 V the switch in series with the resistor of 3 kΩ is opened and pin FBCTRL and thus the RC combination is biased with a 30 μA current-source. When the voltage on FBCTRL pin rises above 4.5 V, switching of the flyback (and also the PFC) is blocked and the controller enters the Safe Restart mode. The capacitor can be used to set the time to reach 4.5 V at the FBCTRL pin. The resistor is necessary to separate the relative large time-out capacitor from the control loop response. Use a resistor of at least 30 kΩ. The resistor however, also influences the charge time of the capacitor.

The time-out time t_{to} can be calculated with Equation 16:

$$t_{to} = \frac{C_{to} \times (V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to}))}{I_{O(FBCTRL)}} \quad (16)$$

Otherwise the capacitor can be calculated with Equation 17:

$$C_{to} = \frac{I_{O(FBCTRL)} \cdot t_{to}}{V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to})} \quad (17)$$

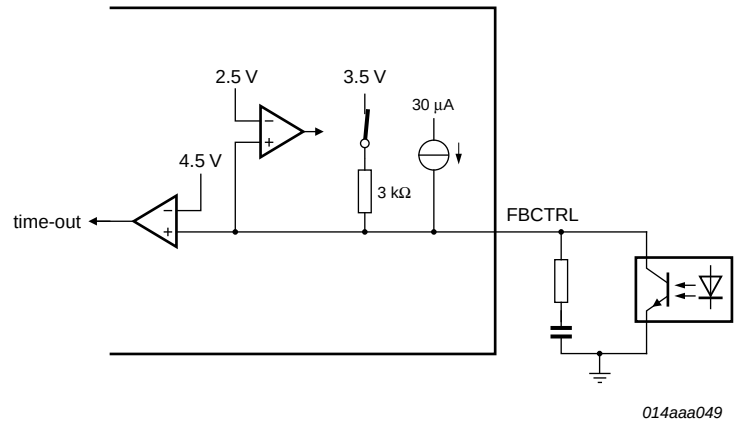
Or the resistor can be calculated with Equation 18:

$$R_{to} = \frac{v_{to(FBCTRL)}}{I_{O(FBCTRL)}} - \frac{t_{to}}{C_{to}} \quad (18)$$

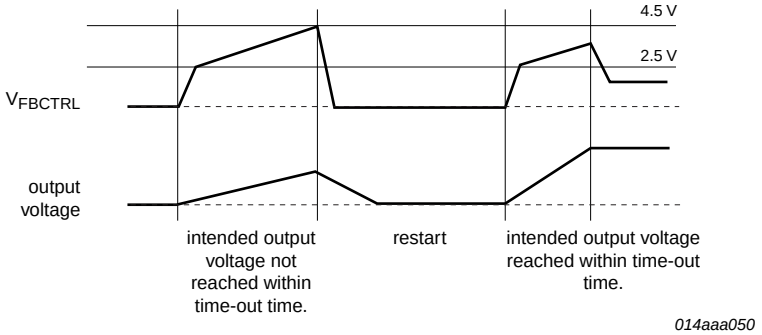
A t_{to} of 37 ms in combination with a C_{to} of 330 nF leads to a resistor value of:

$$R_{to} = \frac{4.5\ V}{30\ \mu A} - \frac{37\ ms}{330\ nF} = 37.9\ k\Omega \approx 39\ k\Omega$$

When the time-out protection is not required, placing a resistor of 100 kΩ between pin FBCTRL and ground can disable the time-out protection.



a. Circuit diagram



b. Timing diagram

Fig 13. Time-out protection

5.3.4 Overvoltage protection flyback

The IC has an internal OverVoltage Protection (OVP) circuit, which switches off both controllers when an overvoltage is detected at the output of the flyback, by a latched protection. The IC can detect an overvoltage at a secondary winding of the flyback by measuring the voltage at the auxiliary winding during the secondary stroke. A series resistor between the auxiliary winding and the FBAUX pin converts this voltage to a current on the FBAUX pin.

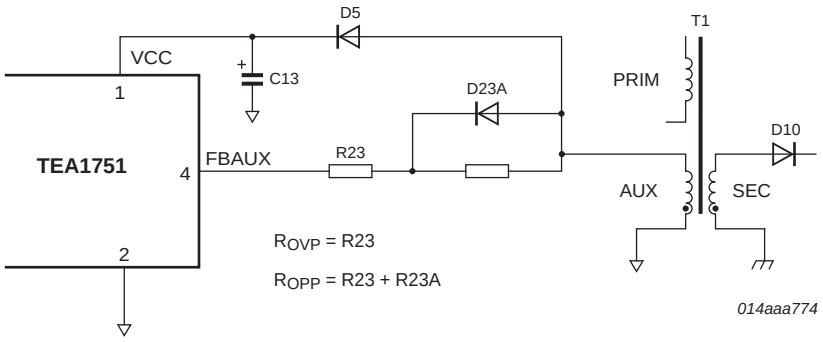


Fig 14. Flyback OVP and OPP circuit

At a current $I_{ovp(FBAUX)}$ of 300 μA into the FBAUX pin, the IC detects an overvoltage. An internal integrator filters noise and voltage spikes. The output of the integrator is used as an input for an up-down counter. The counter has been added as an extra filter to prevent false OVP detection, which might occur during ESD or lightning events.

If the integrator detects an overvoltage, the counter increases its value by one. If another overvoltage is detected during the next switching cycle, the counter increases its value by one again. If no overvoltage is detected during the next switching cycle, then the counter will subtract its value by two (the minimum value is 0). If the value reaches 8, the IC assumes a true overvoltage, and activates the latched protection. Both converters are switched off immediately and V_{CC} starts cycling between the $V_{th(UVLO)}$ and $V_{startup}$, without a restart.

Switching off and then switching on the mains input voltage, triggers the fast latch reset circuit, and reset the latch.

The OVP level can be set by the resistor R_{OVP}:

$$R_{OVP} = \frac{\left(\frac{N_{AUX}}{N_s} \times Vo_{OVP}\right) - V_{clamp(FBAUX)} - Vf_{D23A}}{I_{OVP(FBAUX)}} = \frac{\left(\frac{N_{AUX}}{N_s} \times Vo_{OVP}\right) - 0.7_{(typ)} - Vf_{D23A}}{300\ \mu A_{(typ)}} \quad (19)$$

Where:

- N_s is the number of turns on the secondary winding
- N_{aux} is the number of turns on the auxiliary winding of the flyback transformer
- $V_{clamp(FBAUX)}$ is the positive clamp voltage of the FBAUX pin
- Vf_{D23A} is the forward voltage of D23A at a current of 300 μA

For the calculation of the Vo_{OVP} level, the tolerances on $I_{ovp(FBAUX)}$ must be taken into account, this to avoid triggering of the OVP during normal operation.

5.3.5 OverPower Protection (OPP)

In a quasi-resonant flyback, the maximum output power is dependent on the (mains) input voltage. To compensate for this, an OPP is implemented. During the primary stroke of the flyback the mains voltage is sensed by measuring the current drawn from pin FBAUX. See Figure 14, with a resistor between the flyback auxiliary winding and pin FBAUX the voltage at the auxiliary winding is converted into a current IFBAUX. The IC is using the current information to reduce the setting of the maximum flyback peak current measured through pin FBSENSE. See Figure 15 for the limitation of the maximum $V_{FBSENSE}$ level as a function of I_{FBAUX}.

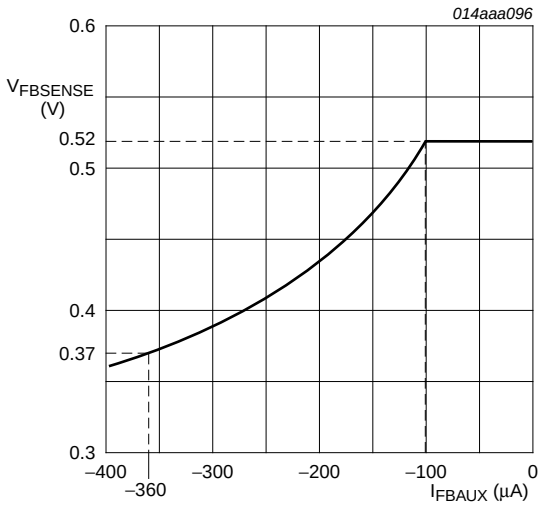


Fig 15. Operation modes flyback

See Figure 14, the total OPP resistance determining the I_{FBAUX} current during the primary stroke of the flyback exists of R23 + R23A. First, the OVP resistor R23 has to be calculated before the remaining part of the OPP resistor R23A can be calculated.

The value of R23A can be calculated with Equation 20:

$$R23A = \frac{\frac{N_a}{N_p} \cdot Vo_{PFC(LOW)} - V_{clamp(FBAUX)}}{I_{start(OPP)FBAUX}} = \frac{\frac{N_a}{N_p} \cdot 240\ V - 0.8\ V}{100\ \mu A} - R_{OVP} \quad (20)$$

6. Summary of calculations

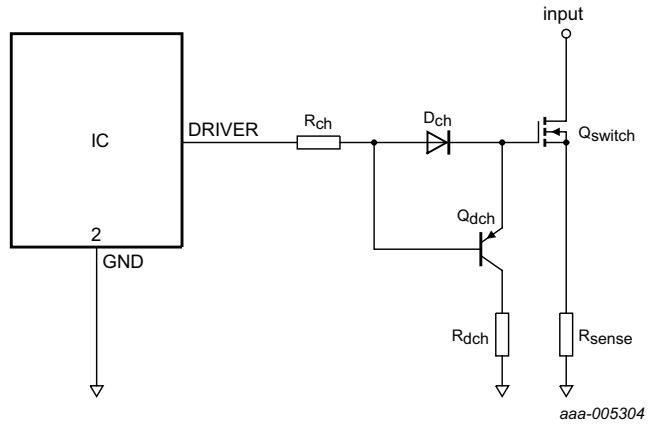
See Figure 1 “Application schematic” for component reference numbers.

7. PCB layout considerations

A good layout is an important part of the final design. It minimizes many kinds of disturbances and makes the overall performance more robust with less risk of EMI. Guidelines for the improvement of the layout of the PCB are as follows:

- Separate large signal grounds from small signal grounds (see Figure 17). A triangular symbol indicates small signal grounds. All other ground symbols are related to large signal grounds.
- Make the print area within the indicated large signal loops (see Figure 17) as small as possible. Each indicated large signal loop has its own color. Make the copper tracks as short and wide as possible.
- The connection between both MOSFETs (PFC and flyback) and the IC driver outputs must be as short as possible (green line in Figure 17). Use wide tracks. Increase the distance between the copper tracks and/or preferably use a separate guided ground track for both connections minimizing the coupling between the PFCDRIVER and FBDRIVER. A circuit diagram according to Figure 16 can be added if it is impossible to place the MOSFET and the IC close to each other.
- The power ground and small signal ground are only connected with one short copper track (make this track as short and as wide as possible). Preferably, it should become one spot (connection between ground 4a and ground 6a, shown as a blue line in Figure 17).
- Use a ground shield underneath the IC, connect this ground shield to the GND pin of the IC.
- Connect all series connected resistors that are fixed to an IC pin as close as possible to that pin.
- Connect heat sinks which are connected to the nearest corresponding ground signal component. Make this connection as short as possible. Connect the heat sink of diode bridge BD1 to ground 1, Q1 to 4, and Q2 to 4b. In typical applications, all three components are often mounted on a single heat sink. If so, make one wide copper track that connects all three grounds to each other. Also combine in this copper track ground 2.
- Connect the grounds of 6b to each other.
- Make a local "star ground" from grounds 6a, 6b, 6c, and 7. Ground 6a is the middle of the star and is connected to the GND pin (the ground of the IC).
- Grounds marked 7 do not have to be a star ground.
- Place the Y-capacitor across grounds 1 and 8. Use one copper track, separated from all others for this connection. Alternatively, in a typical application setup, use the heat sinks connection copper track for this purpose.
- Place C4, C15 and C7 (in order of priority) as close as possible to the IC. Reduce coupling between the PFC switching signals (PFC driver and PFCAUX) and the flyback sense signals (FBSENSE and FBCTRL) as much as possible. The coupling reduction minimizes the risk of electromagnetic interference and audible noise.
- Figure 17 shows an overview of the hierarchy of the different grounds at the bottom. Connect the anode of the TL431 (ground 8) to ground 9 using one special separately connecting copper track. Minimize all other currents in this special track. Make the connection as close as possible to the output.

Remark: Use the circuit shown in Figure 16 when the distance between the IC drive output and corresponding MOSFET are relatively large.



Transistor is mounted close to the MOSFET with wide and short tracks.

Fig 16. Switching off the MOSFET when the distance between IC and MOSFET is large

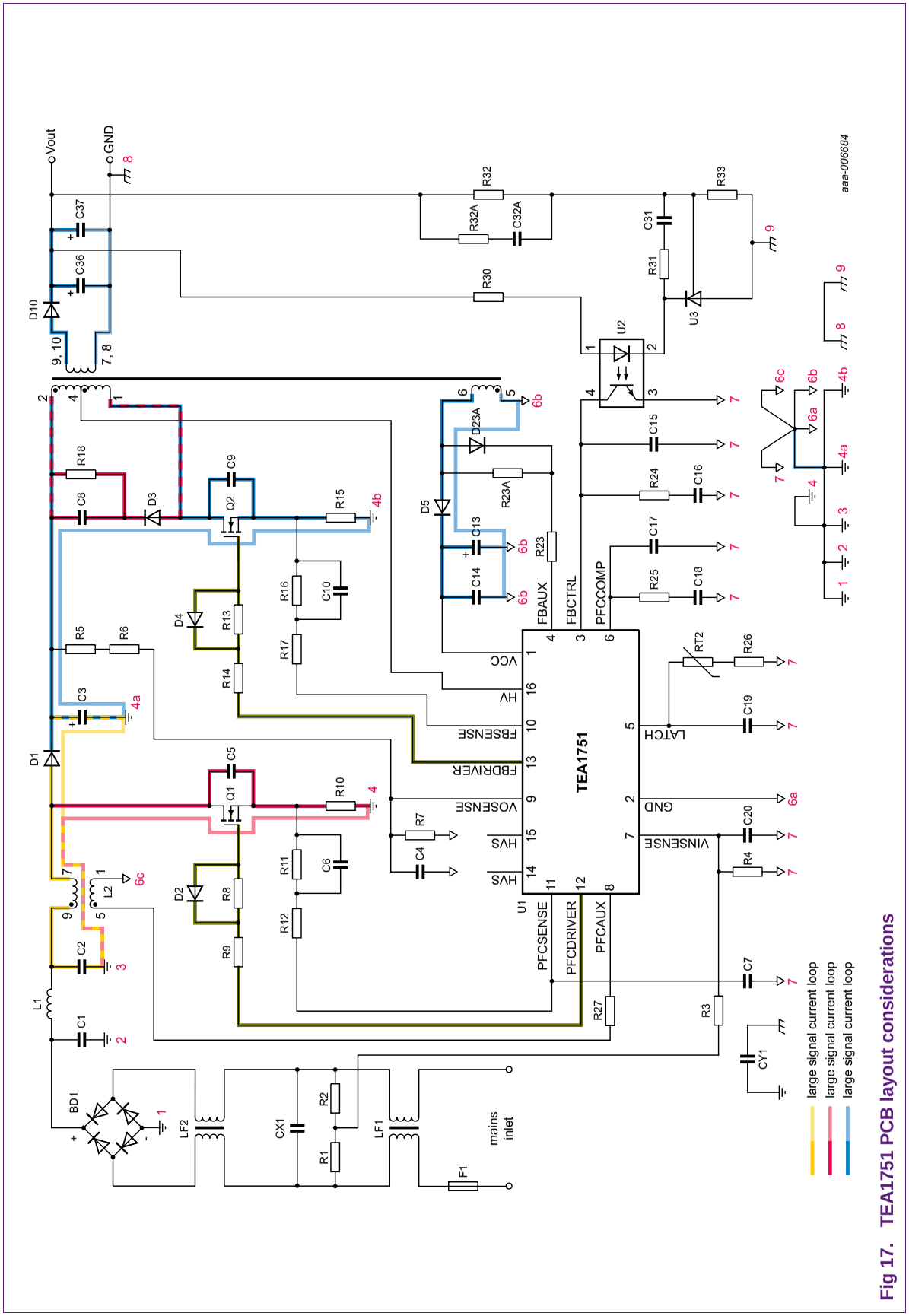


Fig 17. TEA1751 PCB layout considerations

8. References

[1] **IEC-60950 —** Chapter 2.1.1.7 “Discharge of capacitors in equipment”

[2] **IEC61000-3-2 —**

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10. Contents

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