Product Technical Specification

AirPrime WP8548

4116440
Rev 8

Important Notice

Due to the nature of wireless communications, transmission and reception of data can never be guaranteed. Data may be delayed, corrupted (i.e., have errors) or be totally lost. Although significant delays or losses of data are rare when wireless devices such as the Sierra Wireless modem are used in a normal manner with a well-constructed network, the Sierra Wireless modem should not be used in situations where failure to transmit or receive data could result in damage of any kind to the user or any other party, including but not limited to personal injury, death, or loss of property. Sierra Wireless accepts no responsibility for damages of any kind resulting from delays or errors in data transmitted or received using the Sierra Wireless modem, or for failure of the Sierra Wireless modem to transmit or receive such data.

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Do not operate the Sierra Wireless modem in areas where blasting is in progress, where explosive atmospheres may be present, near medical equipment, near life support equipment, or any equipment which may be susceptible to any form of radio interference. In such areas, the Sierra Wireless modem **MUST BE POWERED OFF**. The Sierra Wireless modem can transmit signals that could interfere with this equipment.

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The driver or operator of any vehicle should not operate the Sierra Wireless modem while in control of a vehicle. Doing so will detract from the driver or operator's control and operation of that vehicle. In some states and provinces, operating such communications devices while in control of a vehicle is an offence.

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Revision History

Revision number	Release date	Changes
1	October 2014	Creation (limited release)
2	January 2015	Reorganized content extensively

Revision number	Release date	Changes
3	April 2015	Removed analog audio Removed diversity Changed signal names: 2G_TX_ON to TX_ON; LED1_N to WWAN_LED_N; 19M_CLKOUT to SYS_CLK; 32K_CLKOUT to SLEEP_CLK; TP1_N to TP1; TP2-TP10 to J1-J9 Updated test point dimensions, changed test point signal names Updated Table 1-1 on page 16: GNSS band ranges Updated Figure 2-1, AirPrime WP8548 Architecture Overview, on page 19 Updated Electrical description in Table 2-1 on page 20 Updated Table 3-2, Absolute Maximum Ratings, on page 25: Ripple value, footnotes Updated Figure 3-1, Power Supply Characteristics (capture enlarged), on page 27 Updated Power Consumption States on page 28 Updated Table 3-7, Current Consumption Values, on page 31 Updated Table 3-17, WP7500 Conducted Tx Max Output Power Tolerances—WCDMA, on page 37: Band 6 Updated Table 3-22, WP7502 Conducted Rx Sensitivity—WCDMA Bands,, on page 40: Band 6 Replaced Table 3-18, Absolute Maximum Ratings, on page 40 Updated Table 3-17, GNSS Standalone Antenna Recommendations, on page 38: frequency ranges, IIP2/3 descriptions Updated Mechanical Drawing on page 44 Updated descriptive info for Application Core on page 43 and Embedded Memory on page 44 Updated BAT_RTC on page 46 Updated Table 4-3, POWER_ON_N Electrical Characteristics, on page 47 and removed associated note Updated Table 4.3.1, Power-up Sequence, on page 47 sequence, timing parameters, USB enumeration description Updated Table 4-5, USB Pin Descriptions, on page 48 Updated Table 4-8, GPIO Pin Description, on page 52 Added WAKE_ON_WWAN on page 68 Updated I2C Interface on page 54 description Updated ADC on page 57 Updated Temperature Monitoring on page 65, added AT info for solicited/unsolicited notifications; updated functionality descriptions in table Added SAFE_PWR_REMOVE on page 69 and UIM1_DET/UIM2_DET on page 69 Updated Figure 5-1, Voltage Limiter Example, on page 68 Updated Figure 5-5, UIM Interface, on page 73 Added Figure 5-7, USB OTG Interface, on page 74 Updated Labeling on page 80 Updated Figure 9-1, Pin Configuration (bottom view), on page 89 core/extension/ground identifications Updated Table 9-1, Pin definitions, on page 90: core/extension/ground identifications; “if unused” values throughout table; USB_VBUS details; removed SPKR_N/SPKR_P/MIC_P/MIC_N; changed name SYS_CLK; changed name SLEEP_CLK; added DR_SYNC (was GPIO); updated GPIO numbers; changed name TP1; changed name TX_ON; updated UIM1_DET/UIM2_DET details; replaced LCD signals with Reserved; moved COEX pins; changed name WWAN_LED_N; moved W_DISABLE_N; changed name WAKE_ON_WWAN; replaced some GND/NC/GPIOs as reserved; removed SYSTEM_POWER_CTRL; updated ANT_CTL directions; replaced GPS_DISABLE_N with GPIO Updated supply voltage (3.4-4.3V) Updated Table 2-3, Supported GSM/GPRS/EDGE Specifications, on page 22: Removed R99 details; updated class values GPRS/EDGE
4	April 2015	Removed SPI2, GPIO34-37, COEX, and ADC2-3 content

Revision number	Release date	Changes
5	June 2015	Updated Power Consumption States on page 28 Updated Table 3-21, Internal Device Frequencies, on page 43 (PLL frequencies) Updated Figure 3-4, AirPrime WP8548 Mechanical Drawings, on page 45 Updated Figure 4-2, Recommended UIM Holder Implementation, on page 51 and sample part number Updated Figure 5-5, UIM Interface, on page 73 Corrected pin group field (pins 30,32,36,128) and function field (pins 110,136,139) in Table 9-1, Pin definitions, on page 90 Updated Table 3-11, Conducted Tx Max Output Power Tolerances—GSM, on page 45, Table 3-10, Conducted Rx Sensitivity—GSM/EDGE Bands, on page 33, Table 3-17, WP7500 Conducted Tx Max Output Power Tolerances—WCDMA, on page 37, Table 3-22, WP7502 Conducted Rx Sensitivity—WCDMA Bands,, on page 40. Added DR_SYNC on page 69. Changed GPIO6 to RESET_OUT_N.
6	October 2015	Updated Table 3-7, Current Consumption Values, on page 31. Removed references to “Antenna 1” (since only one antenna) in Table 3-14, Antenna recommendations,, on page 36. Added footnotes explaining signal direction in interface tables in Chapter 3. Noted that USB_VBUS should be connected by customers for future scalability, but is not currently connected internally. Updated Reset Timing (Trlen) parameter in Table 4-14, Reset Timing, on page 55. Added section W_DISABLE_N—Wireless Disable on page 70. Updated Figure 5-5, UIM Interface, on page 73. Updated Figure 5-6, USB Interface, on page 74. Cleanup—replaced “No connect” with “Leave open” throughout document. Updated Table 9-1 on page 90 “I/O” and/or “If unused” columns for pins 1, 16, 31, 55–58, 71–90, 91, 96, 97, 98, 99, 100–103, 107–108, 114–124, 129–135, 140–146, 160. Updated Table 2-3 on page 22 (GPRS—added MCS1-9).
7	February 2016	Updated Table 3-7, Current Consumption Values, on page 31 Updated Table 3-9, Conducted Tx Max Output Power Tolerances—GSM, on page 33 Updated Table 3-10, Conducted Rx Sensitivity—GSM/EDGE Bands, on page 33 Updated Table 3-11, Conducted Tx Max Output Power Tolerances—WCDMA, on page 34 Updated Table 3-12, Conducted Rx Sensitivity—WCDMA Bands, on page 35 Updated RF Circuit on page 73 Updated Important Compliance Information for North American Users on page 85
8	March 2016	Updated GPS frequency range and added Galileo. Updated I2C1_CLK references from ‘O’ to ‘I/O’. Removed DRX_IQ from Figure 2-1 on page 19. Removed ‘sku-dependent’ notes from GNSS availability throughout document. Updated Power Supply Ratings on page 25 description, Table 3-2 on page 25, Table 3-4 on page 26, and added Figure 3-1 on page 27. Updated current consumption descriptions and values in Table 3-6 on page 29, Figure 3-3 on page 30, and Table 3-7 on page 31. Added Active State to ULPM Transition on page 31. Updated POWER_ON_N on page 47 (momentary switch recommendation) Table 4-3 on page 47), and Figure 4-1 on page 47 (POWER_ON_N and SAFE_PWR_REMOVE signals). Exposed additional GPIOs —General Purpose Input/Output (GPIO) on page 52, Figure 9-1 on page 89, Table 9-1 on page 90). Exposed additional ADCs —ADC on page 57, Figure 9-1 on page 89, Table 9-1 on page 90). Removed pins (for GPIOs/ADCs) from Table 9-4 on page 96. Removed auxiliary PCM timing content. Added RF trace design requirement to Important Compliance Information for North American Users on page 85

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1: Introduction

This document defines the high-level product features and illustrates the interfaces for the AirPrime WP8548 Smart Embedded Module. It covers the hardware aspects of the product, including electrical and mechanical.

The AirPrime WP8548 is an HSPA, WCDMA, and quad-band GSM/GPRS/EDGE embedded wireless module.

1.1 General Features

The AirPrime WP8548 is an industrial-grade LGA 239-pad module. Its wireless modem provides voice and data connectivity on HSPA, WCDMA, EDGE and GPRS networks, and GNSS functionality.

In addition to modem features, the AirPrime WP8548 also embeds several cores for maximum flexibility and security for embedded software execution, including:

- A Telecom Core that natively manages 2G/3G modem features
- An Application Core dedicated to customer applications, natively provided with Legato Application framework.

Table 1-2 details the bands/connectivity supported by the AirPrime WP8548.

Table 1-1: Supported Bands/Connectivity

Technology	RF band	Transmit band (Tx) (MHz)	Receive band (Rx) (MHz)
UMTS	B1	1920–1980	2110–2170
	B2	1850–1910	1930–1990
	B5	824–849	869–894
	B6	830–840	875–885
	B8	880–915	925–960
	B19	830–845	875–890
GPRS/EDGE	GSM 850	824–849	869–894
	E-GSM 900	880–915	925–960
	DCS 1800	1710–1785	1805–1880
	PCS 1900	1850–1910	1930–1990
GNSS	GPS	-	1575.42 ± 1.023
	GLONASS	-	1597.52–1605.92
	Galileo	-	1575.42 ± 2.046

1.2 Interfaces

The AirPrime WP8548 module provides the following interfaces and peripheral connectivity:

- Digital section running under 1.8V
- Dual UIM interfaces—See UIM interface on page 50.
- VBAT_RF/VBAT_BB power supply—See Power Supply Ratings on page 25.
- RF (RF_MAIN)—See RF on page 32.
- GNSS (RF_GNSS)—See GNSS on page 37.
- Real Time Clock battery backup—See BAT_RTC on page 46.
- ON/OFF control:
  - POWER_ON_N—See POWER_ON_N on page 47.
  - RESET_IN_N—See Reset Signal (RESET_IN_N) on page 55.
- USB 2.0—See USB on page 48.
- Two UART serial links—primary (8-line) and secondary (4-line)—See UART on page 49.
- GPIOs—See General Purpose Input/Output (GPIO) on page 52.
- SDIO—See Secure Digital IO (SDIO) interface on page 53.
- I^2C—See I2C Interface on page 54.
- 1.8V voltage reference—See VGPIO on page 54.
- Four ADCs—See ADC on page 57.
- Digital audio (PCM/I^2S)—See Digital Audio on page 57.
- HSIC bus—See HSIC Bus on page 63.
- Digital I/O
- Antenna control—See Antenna control on page 67.
- Two System Clock outputs—See Clock on page 64.
- Test pins—See Test Pins on page 66.
- Tx Activity Indicator (TX_ON)—See Tx Activity Indicator (TX_ON) on page 67.

1.3 Common Flexible Form Factor (CF3)

The AirPrime WP8548 belongs to the Common Flexible Form Factor (CF3) family of modules. This family consists of a series of WWAN modules that share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from GSM to LTE advanced) and band groupings
- Supports bit-pipe (Essential Module Series) and value-add (Smart Module Series) solutions
- Offers electrical and functional compatibility

1.4 Physical Dimensions and Connection Interface

The AirPrime WP8548 module is a compact, robust, fully shielded and labeled module with the dimensions noted in Table 1-2.

Table 1-2: AirPrime WP8548 Dimensions[1]

Parameter	Nominal	Tolerance	Units
Length	23.00	±0.10	mm
Width	22.00	±0.10	mm
Thickness	4.352	±0.203	mm
Weight (with label)	4.2	±0.1	g

1. Dimensions are accurate as of the release date of this document.

The AirPrime WP8548 module is an LGA form factor device. All electrical and mechanical connections are made through the 239 Land Grid Array (LGA) pads on the bottom side of the PCB. (See Figure 9-1 on page 89 for details.)

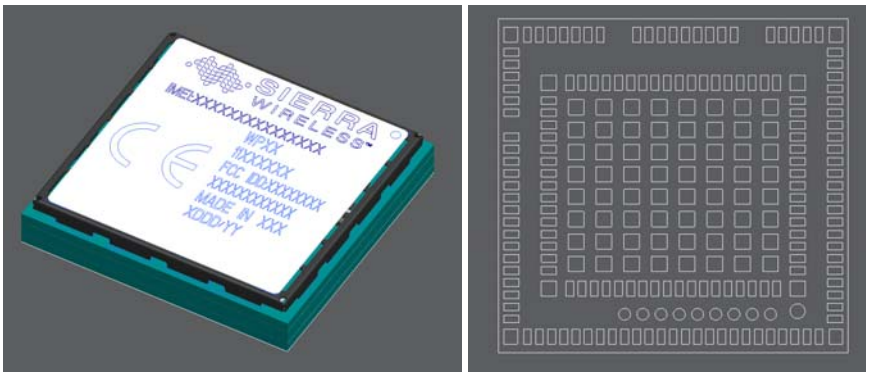

Figure 1-1: AirPrime WP8548 Mechanical Overview

The 239 pads have the following distribution:

- 157 signal pads, 1.0x0.5 mm, 0.8 mm pitch
  - 66 inner signal pads
  - 91 outer signal pads
- 10 test points:
  - 1 polarity mark (Ground), 1.0 mm diameter
  - 9 test points, 0.8 mm diameter, 1.20 mm pitch
- 72 ground pads:
  - 64 inner ground pads, 1.0x1.0 mm, pitch 1.83 mm/1.48 mm
  - 4 inner corner ground pads, 1.0x1.0 mm
  - 4 outer corner ground pads, 1.0x0.9 mm

2: Functional Specifications

2.1 Architecture

Figure 2-1 presents an overview of the AirPrime WP8548 module's internal architecture and external interfaces.

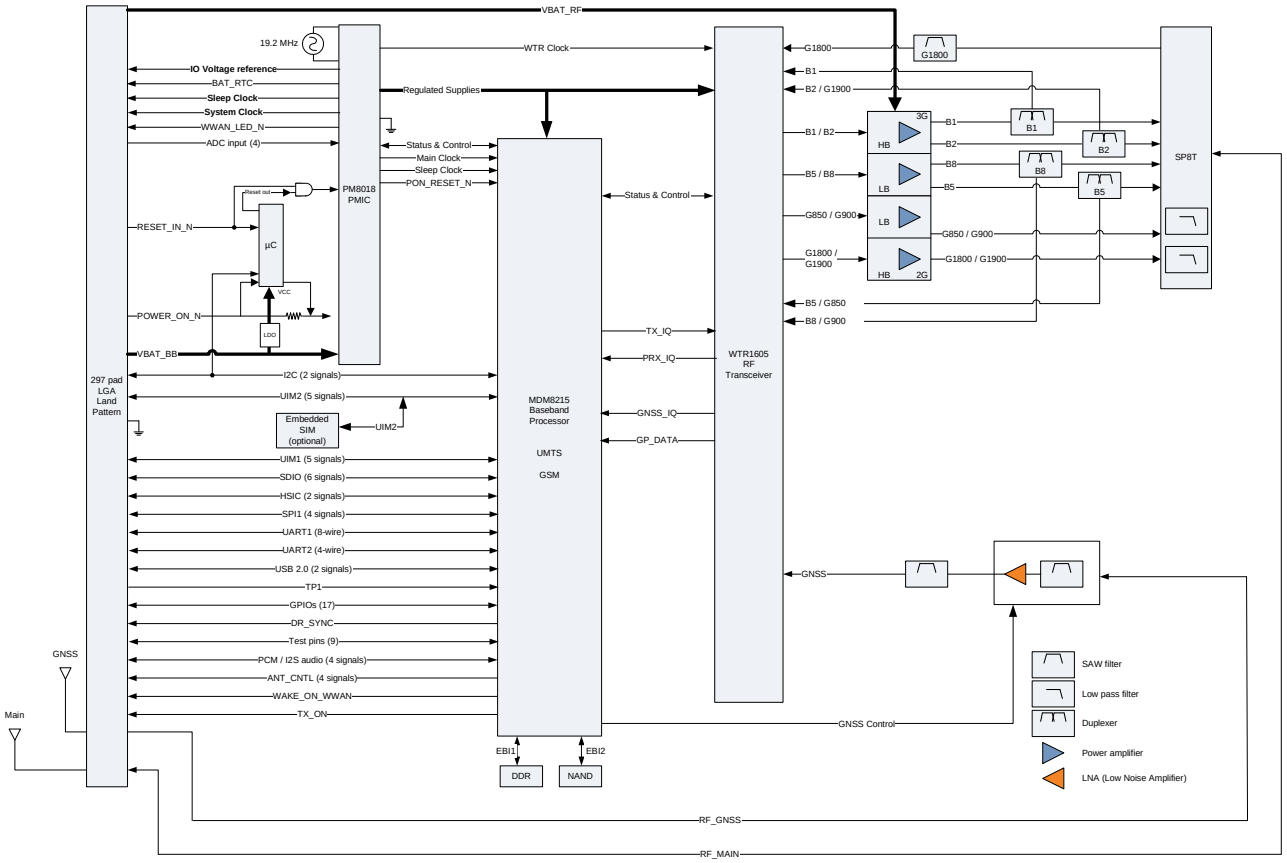

Figure 2-1: AirPrime WP8548 Architecture Overview

2.1.1 Chipsets

The AirPrime WP8548 module is based on the Qualcomm MDM8215 baseband processor.

2.2 Telecom Features

Table 2-1 summarizes the AirPrime WP8548 module's capabilities offered through the Telecom core.

Table 2-1: AirPrime WP8548 capabilities

Feature	Description
Electrical	3.4–4.3V supply voltage (VBAT_BB, VBAT_RF): • Single supply (recommended), VBAT_BB tied to VBAT_RF *or* • Dual supplies, single supply each for VBAT_BB and VBAT_RF
Voice (Digital Audio) (Future firmware release)	• PCM/I^2S digital audio interface • Supports Enhanced Full Rate (EFR), Full Rate (FR), Half Rate (HR), and both Narrow-Band and Wide-band Adaptive Multirate (AMR-NB and AMR-WB) vocoders • MO and MT calling • Echo cancellation and noise reduction • Emergency calls (112, 110, 911, etc.) • Incoming call notification • DTMF generation
SMS	• SMS MO and MT • CS and PS support • SMS saving to UIM card or ME storage • SMS reading from UIM card or ME storage • SMS sorting • SMS concatenation • SMS Status Report • SMS replacement support • SMS storing rules (support of AT+CNMI, AT+CNMA)
Supplementary services (Future firmware release)	• Call Barring • Call Forwarding • Call Hold • Caller ID • Call Waiting • Multi-party service • USSD • Automatic answer

Table 2-2: WP8548 RF bands/connectivity

Technology	RF band	Transmit band (Tx) (MHz)	Receive band (Rx) (MHz)	Maximum output power
UMTS	B1	1920–1980	2110–2170	23 dBm ± 2 dBm; Class 3bis
	B2	1850–1910	1930–1990	23 dBm ± 2 dBm; Class 3bis
	B5	824–849	869–894	23 dBm ± 2 dBm; Class 3bis
	B6	830–840	875–885	23 dBm ± 2 dBm; Class 3bis
	B8	880–915	925–960	23 dBm ± 2 dBm; Class 3bis
	B19	830–845	875–890	23 dBm ± 2 dBm; Class 3bis
GPRS/EDGE	GSM 850	824–849	869–894	2 Watts GSM/GPRS/EDGE
	E-GSM 900	880–915	925–960	2 Watts GSM/GPRS/EDGE
	DCS 1800	1710–1785	1805–1880	1 Watt GSM/GPRS/EDGE
	PCS 1900	1850–1910	1930–1990	1 Watt GSM/GPRS/EDGE
GNSS	GPS	-	1575.42 ± 1.023	-
	GLONASS	-	1597.52–1605.92	-
	Galileo	-	1575.42 ± 2.046	-

2.2.1 Network Technology Specifications

2.2.1.1 GSM/GPRS/EDGE Specifications

Table 2-3: Supported GSM/GPRS/EDGE Specifications

Standard	Feature Description
GPRS	Packet-switched data: • DTM (simple class A) operation • GPRS Multislot class 10 (no backoff)—Four Rx slots (maximum), two Tx slots (maximum), five active slots total • Coding schemes—CS1–CS4 • GEA1, GEA2, and GEA3 ciphering • WCDMA/GERAN system selection

EDGE	• E2 power class for 8 PSK
	• DTM (simple class A), multislot class 12
	• EGPRS—Multislot class 12 (with backoff)—Four Rx slots (maximum), four Tx slots (maximum), five active slots total
	• Coding schemes—MCS1–MCS9
	• BEP reporting
	• SRB loopback and test modes A and B
	• 8-bit and 11-bit RACH
	• PBCCH support
	• One-phase/two-phase access procedures
	• Link adaptation and IR
	• NACC, extended UL TBF
	• PFC/PFI (Packet Flow Context/Packet Flow Identifier) support - allows identity tagging of RLC blocks to identify separate QoS streams at the radio link layer
	• GPRS/EDGE MSC12-EDA - permits allocation of more than two uplink timeslots for GPRS/EDGE
	• Enh DL RLC/MAC Segmentation - permits reception of MAC control messages that exceed one radio block capacity in length
	• Enhanced Ext UL TBF - dummy block transmission is punctured for current saving purposes
	• 2G PS handover - packet-switched equivalent of CS handover to ensure faster cell change and improved throughput
	• WCDMA/GERAN
	  • Band Scan: Run-time Configurable RRC Band Scan Order
	  • Power and Network Optimizations: Frame Early Termination for Power Optimization
	  • Protocols: MRAB-Pack-1 Enhancements - reduces multi-RAB call drops

2.2.1.2 WCDMA Specifications

Table 2-4: Supported WCDMA Specifications

Standard	Feature Description

R99	• All modes and data rates for WCDMA FDD, with the following restrictions:
	  ◦ The downlink supports the following specifications:
	  ▪ Up to four physical channels, including the broadcast channel (BCH), if present
	  ▪ Up to three dedicated physical channels (DPCHs)
	  ▪ Spreading factor (SF) range support from 4 to 256
	  ◦ The uplink supports the following specifications:
	  ▪ One physical channel, eight TrCH, and 16 TrBks starting at any frame boundary
	  ▪ A maximum data rate of 384 kbps
	  ◦ Full SF range support from 4 to 256
	• PS data rates of 384 kbps DL and 384 kbps UL

R5 HSDPA	• PS data speeds up to 42 Mbps (UE category 24) on the downlink
	• HS-DSCH (HS-SCCH, HS-PDSCH, and HS-DPCCH)
	• Maximum of 15 HS-PDSCH channels, both QPSK and 16 QAM modulation
	• Support for 3GPP-defined features:
	  ◦ R99 transport channels
	  ◦ Maximum of four simultaneous HS-SCCH channels
	  ◦ CQI and ACK/NACK on HS-DPCCH channel
	  ◦ All incremental redundancy versions for HARQ
	  ◦ Configurable support for power classes 3 or 4, per TS 25.101
	  ◦ TFC selection limitation on UL factoring in transmissions on the HS-DPCCH, per TS 25.133
	• Switching between HS-PDSCH and DPCH channel resources, as directed by the network
	• Network activation of compressed mode by SF/2 or HLS on the DPCH for conducting inter-frequency or inter-radio access technology (RAT) measurements when the HS-DSCH is active
	• STTD on both associated DPCH and HS-DSCH simultaneously
	• CLTD mode 1 on the DPCH when the HS-PDSCH is active
	• STTD on HS-SCCH when STTD or CLTD mode 1 are configured on the associated DPCH
	• SCH-IC support
	• HS-DSCH DRX support

Table 2-4: Supported WCDMA Specifications (Continued)

Standard	Feature Description

R6 HSUPA	• E-DCH data rates of up to 5.76 Mbps for 2 ms TTI (UE category 6) uplink
	• Support for 3GPP-defined features:
	  ◦ E-AGCH, E-RGCH, and E-HICH channels for downlink; E-RGCH and E-HICH supports serving and nonserving radio links, with up to four radio links in the E-DCH active set
	  ◦ All HARQ incremental redundancy versions and maximum number of HARQ retransmissions
	  ◦ Uplink E-DCH channel with support for up to four E-DPDCH channels
	  ◦ HSUPA channels run simultaneously with R99 and HSDPA channels
	• STTD on all HSUPA downlink channels
	• CLTD mode 1 on HS-PDSCH and DPCH along with HSUPA channels
	• Switch between HSUPA channels and DPCH channel resources, as directed by the network
	• Handover using compressed mode with simultaneous E-DCH and HS-DSCH interactive, background, and streaming QoS classes
	• DPCCH DTX support

2.2.2 Modem Specifications

Table 2-5: Supported Modem Specifications[1]

Standard	Feature Description
Data	• IPHC protocol as RFC 2509 • Stateless DHCPv4 protocol to get P-CSCF and DNS addresses • IPv4/IPv6 • 4 PDNs Support over Multi-RmNet • Dual IP on single RmNet • IP only Mode/Raw IP Mode • Multi-RmNet Data Call

1. Preliminary

2.3 Multi-Core Processing Capabilities

The AirPrime WP8548 is a powerful multiple-core system that includes:

- One QDSP6 core, embedding Telecom firmware with integrated cellular voice (future firmware release), data and wireless Internet connectivity
- One Cortex-A5 core entirely dedicated to customer application and natively provided with Linux operating system

3: Technical Specifications

3.1 Environmental

The environmental specifications for operation and storage of the AirPrime WP8548 are defined in Table 3-1.

Table 3-1: Environmental Specifications

Parameter	Range	Operating Class
Ambient Operating Temperature	-30°C to +70°C	Class A
	-40°C to +85°C	Class B
Ambient Storage Temperature	-40°C to +85°C	-
Ambient Humidity	95% or less	-

Class A is defined as the operating temperature range within which the device:

- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature range within which the device:

- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish any of the device's supported call modes (SMS, Data, and emergency calls) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

3.2 Power Supply Ratings

The AirPrime WP8548 is powered via:

- (Recommended) A single regulated DC power supply (3.7V nominal)
- Two regulated DC power supplies (3.7V nominal), one each for VBAT_BB and VBAT_RF

The AirPrime WP8548 does not support USB bus-operation. DC power is supplied via the VBAT_RF and VBAT_BB signals.

Table 3-2: Absolute Maximum Ratings

Parameter	Min	Max	Units
Power supply voltage (VBAT_BB/VBAT_RF)	-0.3	+6.0	V

Table 3-3: Power Supply Pins

Pin	Name	Direction	Function	If unused
63, 158	VBAT_BB	Input	Baseband power supply	63—Must be used 158—Optional
61, 62, 157	VBAT_RF	Input	RF power supply	61/62—Must be used 157—Optional

Table 3-4: Operating Conditions

Parameter	Min	Typ	Max	Units	Notes
Power supply voltage[1]	3.4	3.7	4.3	V	Must be within min/max values over all operating conditions (including voltage ripple, droop, and transient), especially during the GSM transmit burst.
Power supply ripple	-	-	100	mV_{pp}	See Figure 3-1 on page 27.
Power supply voltage droop	-	-	250	mV	See Figure 3-1 on page 27 and Under-Voltage Lockout (UVLO) on page 27.
Power supply voltage transient (overshoot/undershoot)	-	-	300	mV	See Figure 3-1 on page 27.
Supply current	-	1.0	3.0	A	• Typical value varies and depends on output power, band, and operating voltage. See Current Consumption on page 31 for values measured under normal operating conditions. • Max value measured over 100 µs period.

1. Power supply voltage outside the required range may affect call quality (dropped calls, data transfer errors, etc.).

Customer should characterize the ripple, droop, and transient response (overshoot/undershoot) of the power supply delivery system at the module input under full GSM transmit power. To minimize voltage variation, add suitable capacitors to the supply line as close as possible to the module—depending on the power supply design, these capacitors may range from tens to several thousand µF.

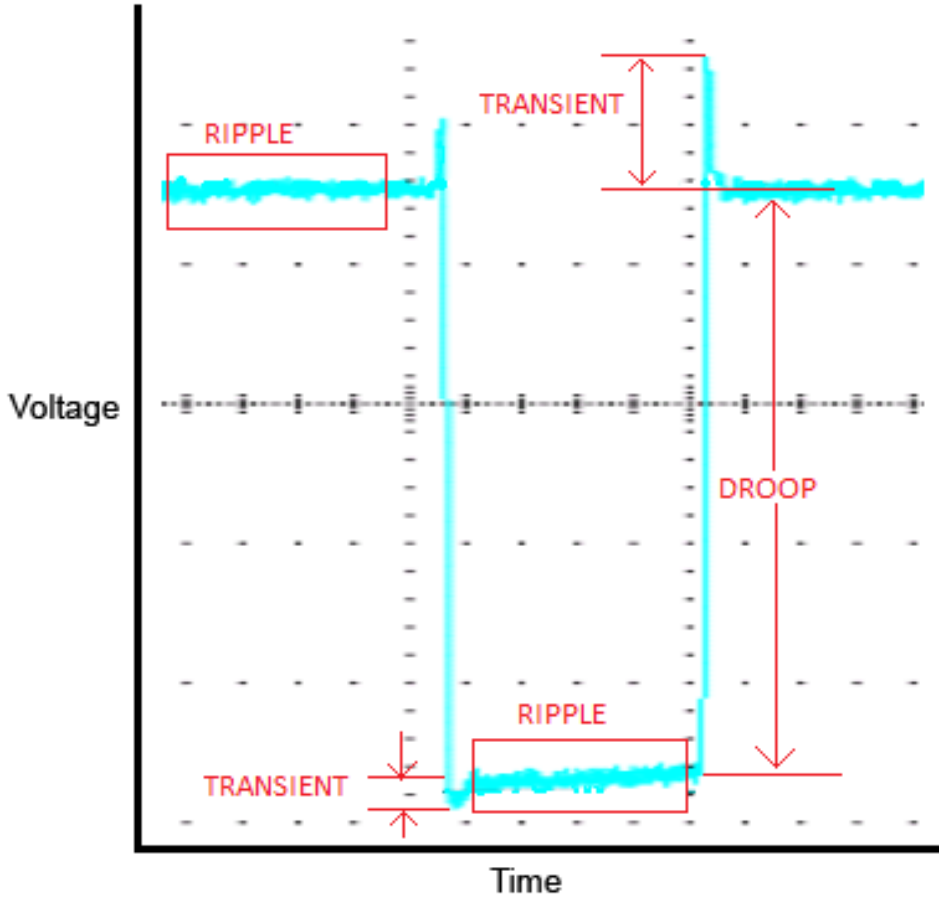

Figure 3-1: Power Supply Characteristics (capture enlarged)

3.2.1 Under-Voltage Lockout (UVLO)

The power management section of the AirPrime WP8548 includes an under-voltage lockout circuit that monitors supply and shuts down when VBAT_BB/ VBAT_RF falls below the threshold.

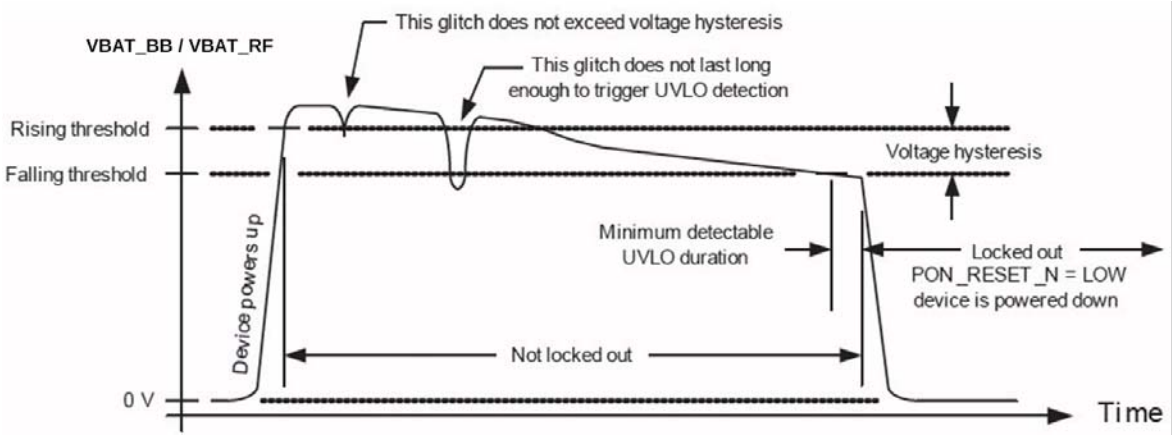

Figure 3-2: Under-Voltage Lockout (UVLO) Diagram

The AirPrime WP8548 will power down and remain off until the level of VBAT_BB/ VBAT_RF returns to the valid range and the ON/OFF signal is active.

Note: If the device experiences six consecutive UVLO events less than 45 seconds apart (approximately) and a host-initiated power down or reset has not occurred, the device enters a mode in which only the DM port enumerates on the USB.

Table 3-5: UVLO Specifications[1]

Parameter	Min	Typ	Max	Units	Notes
Threshold voltage, falling	1.500	2.550	3.050	V	Programmable value
Threshold voltage, accuracy	-5	-	+5	%	
Hysteresis	100	175	250	mV	
UVLO detection interval	-	1.0	-	µs	

1. All values are preliminary and subject to change.

3.2.2 Power Consumption States

The AirPrime WP8548 has three basic power states (Active, Ultra Low Power Mode, and Off). As the module transitions between power states, the range of available device functionality adjusts appropriately, as described in Table 3-6 on page 29 and Figure 3-3 on page 30.

Table 3-6: Supported Power States

State	Description
Active	Module is fully powered and operating in one of the following modes: • Full function (WWAN radio active; GNSS radio can be turned on/off)—Highest power consumption. • Idle (Module registered on network, but no active connection; GNSS radio can be turned on/off) • Airplane mode (WWAN radio off; GNSS radio can be active if allowed by PRI) • Sleep (USB Selective Suspend)—Lowest power consumption while module is in Active state. When the module is in Sleep mode, the processor monitors certain signals that can 'wake' the module—see Wakeup Interrupt (Sleep Mode) on page 53 for details. While in the Active state, the module actively reduces power consumption by disabling components that are not in use (for example, stepping down clock signals, putting the USB into 'selective suspend', etc.). If the device needs to be in use infrequently and greater current consumption savings are needed, the module can be configured to enter Ultra Low Power Mode. See Active State to ULPM Transition on page 31 for details.

Ultra Low Power Mode (ULPM)	Module is in its lowest power state monitoring configured triggers that will return the module to the Active state.
	• For details on how ULPM is configured and entered, see Active State to ULPM Transition on page 31.
	• The module remains in ULPM until:
	  ◦ A configured trigger occurs
	  ◦ RESET_IN_N is used to reset the module
	• ULPM current consumption varies depending on which triggers are configured. For example, the lowest consumption occurs when the processor is waiting only for a timer (approximately 6 µA), and the highest consumption occurs when all supported triggers are configured.

OFF	Module is OFF (no power to the system). Apply power for system to go to Active state.

Figure 3-3 on page 30 illustrates the current consumption requirements of the different power states and the possible transitions between power states. For specific values, see Table 3-7 on page 31.

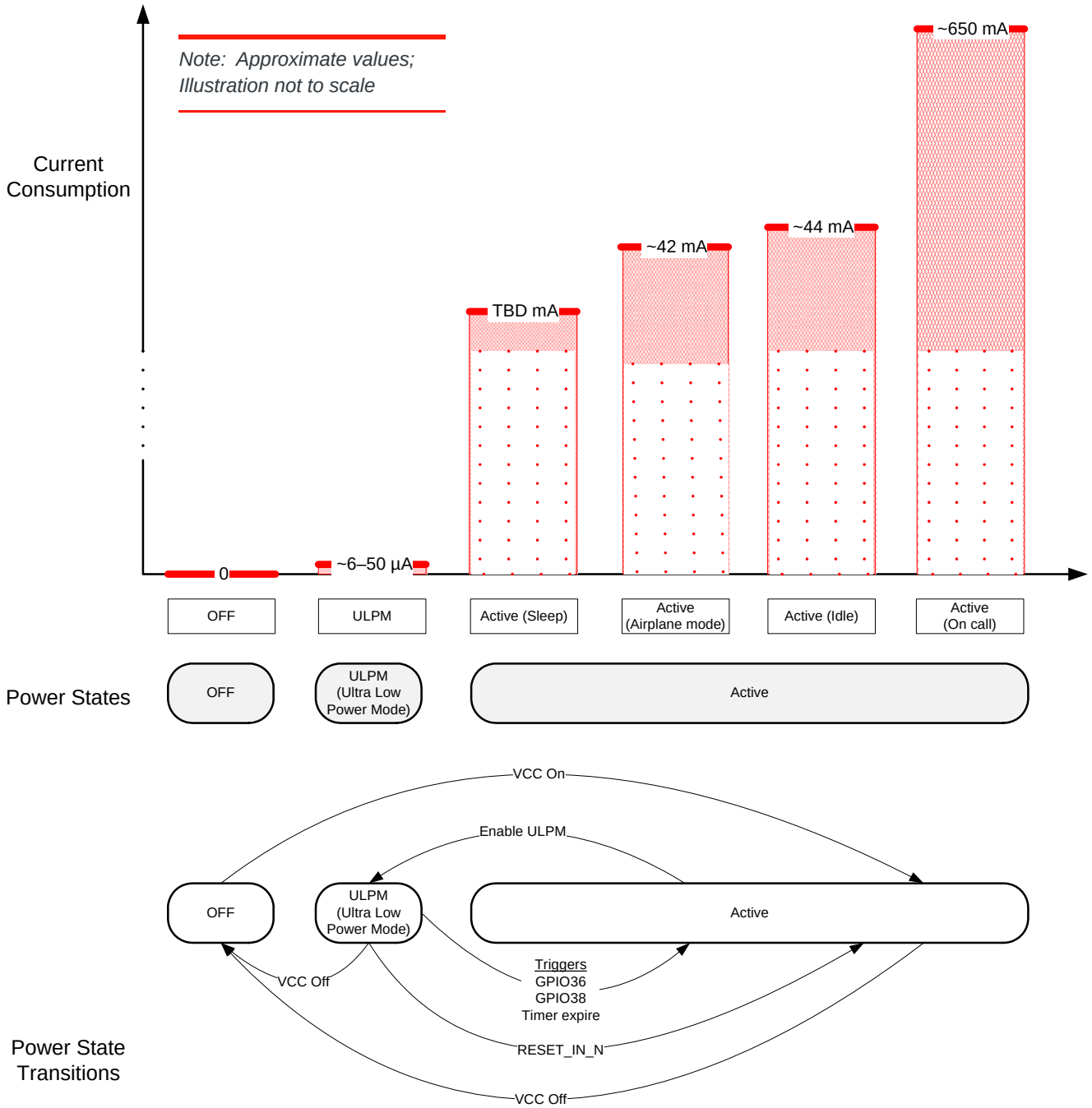

Figure 3-3: Power State Transitions

3.2.3 Active State to ULPM Transition

If the module will be used in situations where it needs to be active very infrequently (for example, in a remote monitoring station that must transmit data once a day), it can be placed in Ultra Low Power Mode (ULPM) to achieve significantly lower power consumption than is possible in Sleep mode (low power active state):

1. Configure one or more supported wakeup triggers that the processor will monitor when the module is in ULPM. Supported triggers include:
   - Interrupt-capable GPIOs (GPIO36, GPIO38)
   - Timer — The module returns to Active state after a specified period. (1–4294967 seconds; 0=timer disabled)
   - Note — Additional triggers may be included in future firmware revisions.
2. Initiate ULPM via the sysfs interface or the corresponding Legato interface. If the configured wakeup conditions are still valid (they have not triggered yet), the module will enter ULPM, otherwise the request will fail and will need to be repeated.

Note: These triggers are non-persistent — if the module enters ULPM and then returns to Active power state, the triggers are erased and will need to be reconfigured.

3.2.4 Current Consumption

Table 3-7 describes the AirPrime WP8548 module's current consumption under various power states. Typical values are measured at nominal supply voltage, nominal ambient temperature, and with a conducted 50Ω load on the antenna port.

Table 3-7: Current Consumption Values[1]

Mode	Parameter	Min	Typ	Max	Units
Power state—Active					
On Call—GSM	850/900 MHz PCL5 +32 dBm	-	300[2]	600[3]	mA
	1800/1900 MHz PCL0 +29 dBm	-	200[2]	500[3]	mA
GSM Peak current	850/900 MHz PCL5 +32 dBm	-	-	2.5[3]	A
	1800/1900 MHz PCL0 +29 dBm	-	-	1.5[3]	A
HSDPA Data transfer	Band 1 @ +23 dBm	450	550	650	mA
	Band 2 @ +23 dBm	450	550	650	mA
	Band 5 @ +23 dBm	350	500	600	mA
	Band 6 @ +23 dBm	330	500	550	mA
	Band 8 @ +23 dBm	410	550	650	mA
	Band 19 @ +23 dBm	330	500	550	mA

Table 3-7: Current Consumption Values[1] (Continued)

Mode	Parameter		Min	Typ	Max	Units
Idle—GSM	Registered	USB enumerated	tbd	44	tbd	mA
		USB not enumerated	tbd	tbd	tbd	mA
Idle—WCDMA	Registered	USB enumerated	tbd	tbd	tbd	mA
		USB not enumerated	tbd	tbd	tbd	mA
Airplane mode			tbd	42	tbd	mA
Sleep mode	Average current, QPCH, SCI=2		tbd	tbd	tbd	mA
	Average current, WCDMA, DRX=8		tbd	tbd	tbd	mA
Power state—Ultra Low Power Mode (ULPM)						
MCU monitoring triggers	Timer and GPIO triggers (GPIO36, GPIO38) configured		-	50	-	µA
	Only wakeup timer trigger is configured		-	6	-	µA
GNSS[4]						
GNSS	Acquisition (Airplane mode, cold start)		30	40	50	mA
	Tracking (Registered)		25	35	45	mA

1. All values are preliminary, subject to change.
2. Typical—values for one slot
3. Maximum—values for four slots with no backoff
4. GNSS current consumption values are for the GNSS radio only. For total consumption, add the GNSS value to the consumption for the mode being used.

3.3 RF

This section presents the AirPrime WP8548 WWAN RF interface, and defines the specifications for the HSPA, WCDMA, and GSM interfaces.

AirPrime WP8548 embedded modules are designed to be compliant with the standards in Table 3-8.

Table 3-8: Standards Compliance

Technology	Standards
UMTS (WCDMA)	• 3GPP Release 8
GSM/GPRS/EDGE	• 3GPP Release 8

3.3.1 GSM RF Interface

This section presents the AirPrime WP8548 GSM RF specification.

3.3.1.1 GSM Tx Output Power

The maximum transmitter output power of the AirPrime WP8548 is specified in Table 3-9.

Table 3-9: Conducted Tx Max Output Power Tolerances — GSM[1]

RF band	Min	Typ	Max	Notes
GSM 850	31	32	33	GMSK mode, connectorized (Class 4; 2 W; 33 dBm)
E-GSM 900	31	32	33	
DCS 1800	28	29	30	GMSK mode, connectorized (Class 1; 1 W, 30 dBm)
PCS 1900	28	29	30	
GSM 850	25.5	26.5	27.5	8PSK mode, connectorized (Class E2; 0.5 W; 27 dBm)
E-GSM 900	25.5	26.5	27.5	
DCS 1800	24.5	25.5	26.5	8PSK mode, connectorized (Class E2; 0.4 W, 26 dBm)
PCS 1900	24.5	25.5	26.5	

1. Stated power tolerances satisfy 3GPP TS 51.010-1 requirements for normal (25°C) conditions.

3.3.1.2 GSM Rx Sensitivity

The receiver sensitivity of the AirPrime WP8548 is specified in Table 3-10.

Table 3-10: Conducted Rx Sensitivity — GSM/EDGE Bands[1]

GSM/EDGE Bands			Sensitivity @ +25°C (dBm)[2]	Sensitivity @ Class A (dbm)[3]	Standard Limit (dBm)
GSM 850	2.44% BER CS	CS	-109	-108	-102
	10% BLER	GMSK CS1	-113	-112	-104
	10% BLER	EDGE MCS5	-105	-104	-98
EGSM 900	2.44% BER CS	CS	-109	-108	-102
	10% BLER	GMSK CS1	-113	-112	-104
	10% BLER	EDGE MCS5	-105	-104	-98
DCS 1800	2.44% BER CS	CS	-108	-107	-102
	10% BLER	GMSK CS1	-112	-111	-104
	10% BLER	EDGE MCS5	-104	-103	-98

Table 3-10: Conducted Rx Sensitivity — GSM/EDGE Bands[1]

GSM/EDGE Bands			Sensitivity @ +25°C (dBm)[2]	Sensitivity @ Class A (dbm)[3]	Standard Limit (dBm)
PCS 1900	2.44% BER CS	CS	-108	-107	-102
	10% BLER	GMSK CS1	-112	-111	-104
	10% BLER	EDGE MCS5	-104	-103	-98

1. Stated sensitivity values satisfy 3GPP TS 51.010-1 requirements for normal (25°C) and Class A (extreme) conditions.
2. Typical value
3. Typical value, tested at Class A extreme condition

3.3.2 WCDMA RF Interface

This section presents the AirPrime WP8548 WCDMA RF specification.

3.3.2.1 WCDMA Tx Output Power

The maximum transmitter output power of the AirPrime WP8548 is specified in Table 3-11.

Table 3-11: Conducted Tx Max Output Power Tolerances — WCDMA[1]

RF band	Min	Typ	Max	Notes
B1	22	23	24	Connectorized (Class 3)
B2	22	23	24	Connectorized (Class 3)
B5	22	23	24	Connectorized (Class 3)
B6	22	23	24	Connectorized (Class 3)
B8	22	23	24	Connectorized (Class 3)
B19	22	23	24	Connectorized (Class 3)

1. Stated power tolerances satisfy 3GPP TS 34.121-1 requirements for normal (25°C) conditions.

3.3.2.2 WCDMA Rx Sensitivity

The receiver sensitivity of the AirPrime WP8548 is specified in Table 3-12.

Table 3-12: Conducted Rx Sensitivity—WCDMA Bands[1]

Band	Sensitivity @ +25°C (dBm)[2]	Sensitivity @ Class A (dbm)[3]	Standard Limit (dBm)	Notes
B1	-109	-108	-106	CS 0.1% BER 12.2 kbps Reference Measurement Channel
B2	-110	-109	-104	
B5	-111	-110	-104	
B6	-111	-110	-106	
B8	-111	-110	-103	
B19	-111	-110	-106	

1. Stated sensitivity values satisfy 3GPP TS 34.121-1 V8.10.0 requirements for normal (25°C) and Class A (extreme) conditions.
2. Typical value
3. Typical value, tested at Class A extreme condition

3.3.3 WWAN Antenna Interface

The WWAN antenna interface of the AirPrime WP8548 is defined in Table 3-13.

Table 3-13: WWAN Antenna Interface Pins

Pin #	Signal name	Direction	Function
48	GND		Primary Antenna Ground
49	RF_MAIN	Input/Output	Primary Antenna Interface
50	GND		Primary Antenna Ground
136	GND		Primary Antenna Ground
139	GND		Primary Antenna Ground

3.3.3.1 WWAN Antenna Recommendations

Table 3-14 defines the key characteristics to consider for antenna selection.

Table 3-14: Antenna recommendations[1,2]

Parameter	Recommendations	Comments
Antenna system	External multi-band antenna system	
Operating bands	824–960 MHz	Operating bands depend on the module's supported bands/modes.
	1710–1990 MHz	
	2110–2170 MHz	
VSWR	< 2.5:1 (worst case)	• 1:1 (ideal) • On all bands including band edges
Total radiated efficiency	> 50% on all bands	• Measured at the RF connector. • Includes mismatch losses, losses in the matching circuit, and antenna losses, excluding cable loss. • Sierra Wireless recommends using antenna efficiency as the primary parameter for evaluating the antenna system. • Peak gain is not a good indication of antenna performance when integrated with a host device (the antenna does not provide omnidirectional gain patterns). Peak gain can be affected by antenna size, location, design type, etc.—the antenna gain pattern remains fixed unless one or more of these parameters change.
Radiation patterns	Nominally omnidirectional radiation pattern in azimuth plane.	
Mean Effective Gain (MEG)	≥ -3 dBi	
Maximum antenna gain	Must not exceed antenna gains due to RF exposure and ERP/ EIRP limits, as listed in the module's FCC grant.	

Table 3-14: Antenna recommendations[1,2] (Continued)

Parameter	Recommendations	Comments
Maximum voltage applied to antenna	15 VDC	
Power handling	• > 2 W RF power on low bands • > 1 W on high bands	• Measure power endurance over 4 hours (estimated talk time) using a 2 W CW signal—set the CW test signal frequency to the middle of the PCS Tx band (1880 MHz for PCS). • Visually inspect device to ensure there is no damage to the antenna structure and matching components. • VSWR/TIS/TRP measurements taken before and after this test must show similar results.

1. These worst-case VSWR figures for the transmitter bands may not guarantee RSE levels to be within regulatory limits. The device alone meets all regulatory emissions limits when tested into a cabled (conducted) 50 ohm system. With antenna designs with up to 2.5:1 VSWR or worse, the radiated emissions could exceed limits. The antenna system may need to be tuned in order to meet the RSE limits as the complex match between the module and antenna can cause unwanted levels of emissions. Tuning may include antenna pattern changes, phase/delay adjustment, passive component matching. Examples of the application test limits would be included in FCC Part 22, Part 24 and Part 27, test case 4.2.16 for GSM (ETSI EN 301 511), and test case 4.2.2 for WCDMA (ETSI EN 301 908-1), where applicable.
2. All values are preliminary and subject to change.

3.4 GNSS

The AirPrime WP8548 includes Global Navigation Satellite System (GNSS) capabilities via the Qualcomm IZat™ Gen8A Engine (formerly gpsOne), capable of operation in assisted and standalone GNSS modes (GPS/Galileo/GLONASS).

3.4.1 GNSS Characteristics

The GNSS implementation supports GPS L1, Galileo E1, and GLONASS L1 FDMA operation.

Table 3-15: GNSS Characteristics [1]

Parameter		Value
Sensitivity	Standalone or MS-based tracking sensitivity	-161 dB
	Cold start sensitivity	-145 dB
	MS-assisted GNSS acquisition sensitivity	-158 dBm
Accuracy in open sky (1 Hz tracking)		< 2 m CEP-50
Total number of SV available		~55
Support for predicted orbits		Yes

Table 3-15: GNSS Characteristics (Continued)[1]

Parameter		Value
Predicted orbit CEP-50 accuracy		5 m
Standalone Time To First Fix (TTFF)	Hot	1 s
	Warm	29 s
	Cold	32 s
GNSS message protocols		NMEA

1. All values are preliminary and subject to change.

Note: Acquisition/tracking sensitivity performance figures assume open sky with active patch GNSS antenna and a 2.5 dB noise figure.

3.4.2 GNSS Antenna Interface

TheAirPrime WP8548 GNSS antenna interface is defined in Table 3-16.

Table 3-16: GNSS Antenna Interface Pads

Pad	Name	Direction[1]	Function
37	GND		GNSS Antenna Ground
38	RF_GNSS	Input	GNSS Antenna Interface
39	GND		GNSS Antenna Ground
125	GND		GNSS Antenna Ground
128	GND		GNSS Antenna Ground

1. Signal direction with respect to the module.

3.4.2.1 GNSS Antenna Recommendations

Table 3-17 defines the key characteristics to consider for antenna selection.

Table 3-17: GNSS Standalone Antenna Recommendations[1]

Parameter	Recommendations	Notes
Frequency range	• Wide-band GPS, Galileo, and GLONASS: 1573–1606 MHz recommended • Narrow-band GPS: 1575.42 MHz ± 2.046 MHz minimum	
Field of view (FOV)	• Omni-directional in azimuth • -45° to +90° in elevation	

Table 3-17: GNSS Standalone Antenna Recommendations[1] (Continued)

Parameter	Recommendations	Notes
Polarization (average Gv/Gh)	> 0 dB	Vertical linear polarization is sufficient.
Free space average gain (Gv+Gh) over FOV	> -6 dBi (preferably > -3 dBi)	Gv and Gh are measured and averaged over -45° to +90° in elevation, and ±180° in azimuth.
Gain	• Maximum gain and uniform coverage in the high elevation angle and zenith. • Gain in azimuth plane is not desired.	
Average 3D gain	> -5 dBi	
Isolation between GNSS and RF Antenna	> 10 dB in all uplink bands	
Typical VSWR	< 2.5:1	
Polarization	Any other than LHCP (left-hand circular polarized) is acceptable.	Type of antenna and polarization (RHCP/ linear) to be implemented is a matter of consideration based on specific end application.
Maximum voltage applied to antenna	15 VDC	
700 MHz harmonic[2]	< -56 dBm (input jammer 787.76 MHz at -25 dBm and measure the harmonic tone at 1575.42 MHz)	This specification is for B13 coexistence.
IIP2[2]	> 45 dBm (Input jammers at 824.6 MHz with level -25 dBm and 2400 MHz with level -32 dBm and measure output IM2 at 1575.4 MHz)	Out of band
IIP3[2]	> 2 dBm (Input jammers at 1712.7 MHz with level -20 dBm and 1850 MHz with level -65 dBm and measure output IM3 at 1575.4 MHz)	Out of band
Input 1 dB power compression point[2]	> -10 dBm	
Out of band rejection for an active antenna		
777–798 MHz	> 50 dB	
814–915 MHz	> 40 dB	50 dB is preferred
925–960 MHz	> 30 dB	50 dB is preferred

Table 3-17: GNSS Standalone Antenna Recommendations[1] (Continued)

Parameter	Recommendations	Notes
1427–1463 MHz	> 35 dB	
1710–1785 MHz	> 35 dB	
1850–1980 MHz	> 40 dB	
2010–2025 MHz	> 40 dB	
2305–2315 MHz	> 40 dB	
2401–2483 MHz	> 40 dB	
2500–2570 MHz	> 35 dB	

1. All values are preliminary and subject to change.
2. For the LNA used by an active antenna

3.5 Electrical Specifications

This section provides details of the key electrical specifications of the AirPrime WP8548 embedded module.

3.5.1 Absolute Maximum Ratings

This section defines the absolute maximum ratings of the AirPrime WP8548.

Warning: *If these parameters are exceeded, even momentarily, damage may occur to the device.*

Table 3-18: Absolute Maximum Ratings [1]

Parameter		Min	Typ	Max	Units
Power supply voltages					
VBAT_BB/ VBAT_RF	Power Supply Input	-0.3	-	6.0	V
VDD_Px (low-voltage operation)	Digital pad circuits	-	-	2.2	V
VDD_Px (high-voltage operation)	Digital pad circuits	-	-	3.05	V
USB signal pins					
USB_D+	High-speed USB data plus	-	-	5.25	V
USB_D-	High-speed USB data minus	-	-	5.25	V
USB_VBUS	High-speed USB bus voltage	-	-	5.25	V

Table 3-18: Absolute Maximum Ratings (Continued)[1]

Parameter		Min	Typ	Max	Units
Thermal conditions					
TS	Storage temperature	-40		85	°C
TJ	Junction temperature	-	-	tbd	°C
Maximum voltage applied to antenna interface pins					
VANT	RF_MAIN	-		15	Vdc
	RF_GNSS	-		15	Vdc
ESD ratings					
See EMC and ESD Recommendations on page 76.					

1. All values are preliminary and subject to change.

3.5.2 Digital I/O Characteristics

The I/O characteristics for supported digital interfaces are described in:

- Table 3-19—GPIOs, UART, ANT_CNTL, HSIC, TX_ON, and PCM/I^2S signals
- Table 3-20—SDIO signals

Table 3-19: Digital I/O Characteristics (V_{DD_PX} = 1.80 V (nominal)) [1]

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	-	V_{DD_PX} + 0.3	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	-	0.35 * V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	-	-	mV
I_{IH}	Input high leakage current[2]	No pull-down	-		1	µA
I_{IL}	Input low leakage current[3]	No pull-up	-1		-	µA
R_P	Pull up/down resistance		55		390	kΩ
V_{OH}	High level output voltage	CMOS, at pin-rated drive strength	V_{DD_PX} - 0.45	-	V_{DD_PX}	V
V_{OL}	Low level output voltage	CMOS, at pin-rated drive strength	0	-	0.45	V
I_{OZH}	Tri-state leakage current[2]	Logic high output, no pull-down	-		1	µA
I_{OZL}	Tri-state leakage current[3]	Logic low output, no pull-up	-1		-	µA
R_K	Keeper resistance		30		150	kΩ
I_{ISL}	Sleep crystal input leakage		-0.15	-	0.15	µA

Table 3-19: Digital I/O Characteristics (V_{DD_PX} = 1.80 V (nominal)) (Continued)[1]

Parameter		Comments	Min	Typ	Max	Units
I_{IHVKP}	High-V tolerant input leakage	With keeper	-1	-	-	µA
C_{IN}	Input capacitance[4]		-	-	5	pF
I_{PIN}	Current per pin		-	-	16	mA

1. All values are preliminary and subject to change.
2. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
3. Pin voltage = GND and supply = V_{DD_PX} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
4. Input capacitance is guaranteed by design, but is not 100% tested.

Table 3-20: Digital I/O Characteristics (VDD_PX = 2.95 V (nominal) signals) [1]

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	-	V_{DD_PX} + 0.3	V
V_{IL}	Low level input voltage	CMOS/Schmitt	-0.3	-	0.25 * V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	-	-	mV
I_{IH}	Input high leakage current[2]	No pull-down	-		10	µA
I_{IL}	Input low leakage current[3]	No pull-up	-10		-	µA
R_{PSD}	High-V pad pull up/down resistance	For SDIO_CLK, SDIO_CMD, SDIO_DATA[0:3]	10		100	kΩ
I_{OZH}	Tri-state leakage current[2]	Logic high output, no pull-down	-		10	µA
I_{OZL}	Tri-state leakage current[3]	Logic low output, no pull-up	-10		-	µA
R_{KSD}	High-V pad keeper resistance	For SDIO_CLK, SDIO_CMD, SDIO_DATA[0:3]	10		100	kΩ
V_{OH}	High-level output voltage	CMOS, at pin-rated drive strength	V_{DD_PX}-0.45		V_{DD_PX}	V
V_{OL}	Low-level output voltage	CMOS, at pin-rated drive strength	0		0.45	V
C_{IN}	Input capacitance[4]		-	-	5	pF
I_{PIN}	Current per pin		-	-	8	mA

1. All values are preliminary and subject to change.
2. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
3. Pin voltage = GND and supply = V_{DD_PX} max. for keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
4. Input capacitance is guaranteed by design, but is not 100% tested.

3.5.3 Internal Device Frequencies

Table 3-21 summarizes the frequencies generated within the AirPrime WP8548. This table is provided for reference only to the device integrator.

Table 3-21: Internal Device Frequencies [1]

Subsystem / Feature	Frequency	Units
Real Time Clock	32.768	kHz
PCM Audio Interface (Primary PCM Master Mode)	128, 2048	kHz
I^2C Interface	400	kHz
PMIC switching power supplies	1.6	MHz
Fundamental clock	19.2	MHz
PLL	• PLL0: 276.000 • PLL4: 393.216 • PLL5: 576.000 • PLL6: 460.800 • PLL7: 499.200 • PLL8: 384.000 • PLL9: 440.000 (v1) / 550.000 (v2+) • PLL11: 400.000 • PLL14: 480.000	MHz
PMIC	1.6	MHz
USB	480	Mb/s

1. All values are preliminary and subject to change.

3.6 Processing

3.6.1 Application Core

The Application Core is based on a Cortex A5 32-bit RISC architecture core. It has the following main characteristics:

- Up to 550 MHz operation
- Cache: Instruction (32kB) and Data (32kB)

The Application Core supports Legato™, an open source embedded platform built on Linux, which allows the simultaneous safe running of multiple applications.

Refer to Interfaces Specification on page 46 for the list of interfaces supported by this core.

3.6.2 Embedded Memory

The AirPrime WP8548 module's embedded memory includes 512 MB Flash and 256 MB RAM.

Half of this memory (256 MB Flash, 128 MB RAM) is dedicated to the Legato platform running on the application processor, including:

- Linux kernel
- Root file system
- Application framework
- Customer applications
- Telecom image

3.7 Mechanical Drawing

The AirPrime WP8548 module's LGA footprint is a 239-pad array of copper pads (see Physical Dimensions and Connection Interface on page 18). The following drawing illustrates the device footprint and dimensions.

Note: Dimensions in Figure 3-4 are preliminary and subject to change.

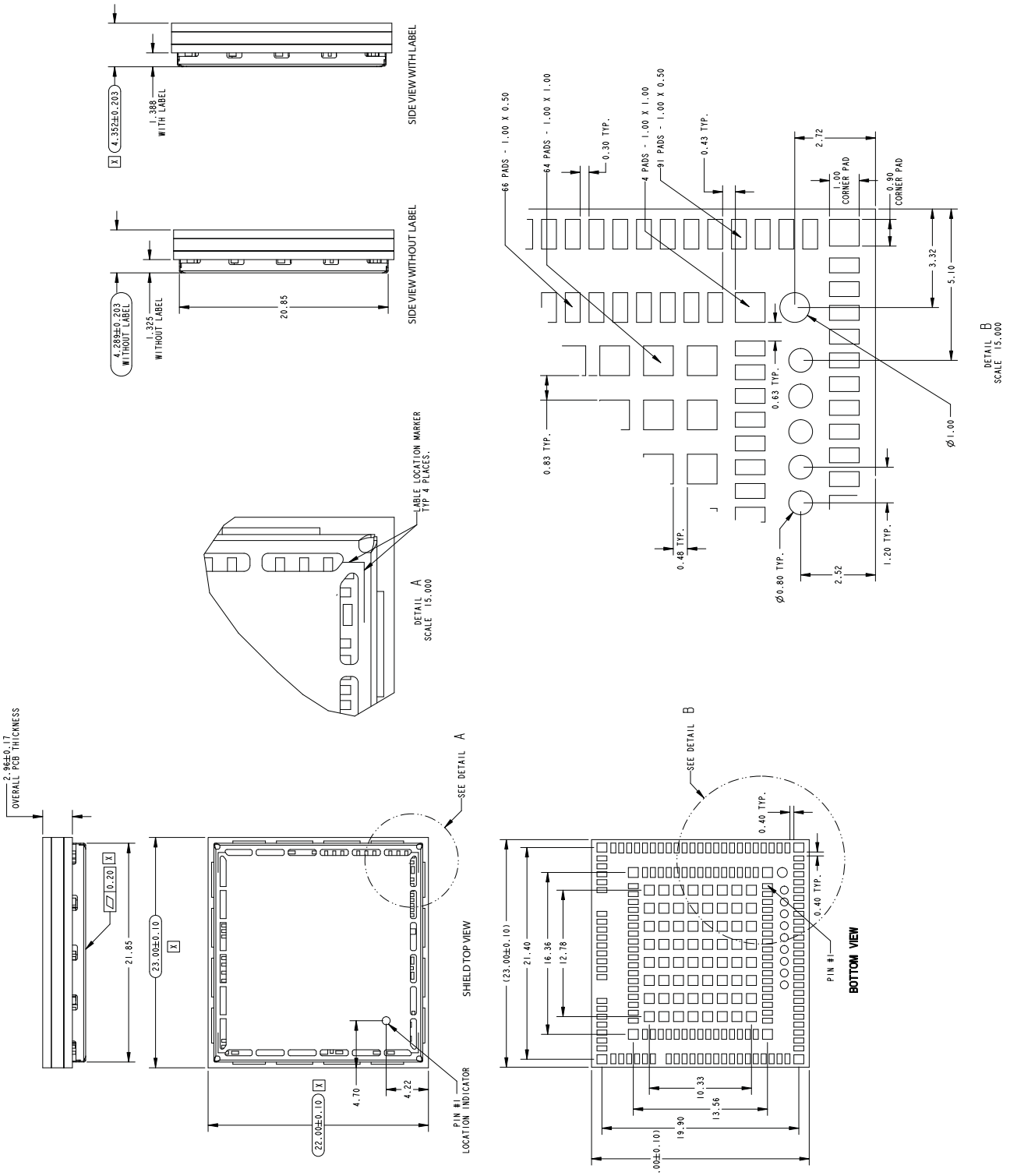

Figure 3-4: AirPrime WP8548 Mechanical Drawings

4: Interfaces Specification

4.1 Overview

This section describes the interfaces supported by the AirPrime WP8548 embedded module and provides specific voltage, timing, and circuit recommendations for each interface.

4.2 BAT_RTC

The AirPrime WP8548 module's internal RTC is powered from the VBAT_BB supply (when available).

The module also provides an interface (BAT_RTC) for using a coin cell to maintain the internal RTC when VBAT_BB is removed from the module. The coin cell can also be charged via BAT_RTC when VBAT_BB is available.

Table 4-1: BAT_RTC Pin

Pin	Name	Direction	Function	If Unused
21	BAT_RTC	Input/Output	Voltage input/Charging output	Leave Open

Table 4-2: BAT_RTC Charging Specifications [1]

Specification		Comments	Min	Typ	Max	Units
Target regulator voltage		V_{IN} > 3.3 V, I_{CHG} = 100 µA	-	2.5	-	V
Target series resistance[2]			800	-	2100	Ω
Coin cell voltage			2.0	-	2.25	V
Coin cell charger voltage error		I_{CHG} = 0 µA	-5	-	+5	%
Coin cell charger resistor error			-20	-	+20	%
Dropout voltage[3]		I_{CHG} = 2 mA	-	-	200	mV
Current draw	Charging		-	2.0	-	mA
	Off		-	5.0	8.0	µA
Ground current, charger enabled	VBAT=3.6V	IC = off; BAT_RTC = open, T=27°C	-	4.5	-	µA
	VBAT=3.4–4.3 V		-	-	8.0	µA
Capacitance			-	-	4.7	µF

1. All values are preliminary and subject to change
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω
3. Dropout is measured by reducing the supply voltage (VBAT) from 3.5 V until the charging voltage drops by 100 mV. Then calculate the dropout voltage: $V_{dropout}$ = VBAT - charger output voltage.

4.3 POWER_ON_N

The AirPrime WP8548 module requires a low level signal (POWER_ON_N) that is used to switch the module ON.

The signal is connected internally to the permanent 1.8V supply regulator inside the module via a pull-up resistor. Once VBAT_BB is supplied to the module, this 1.8V supply regulator will be enabled and so the POWER_ON_N signal is by default at high level. Use a momentary switch to control this line to reduce leakage current.

Table 4-3 describes the POWER_ON_N signal's characteristics.

Table 4-3: POWER_ON_N Electrical Characteristics[1]

Parameter	Min	Typ	Max	Units
Input Voltage—Low		-	0.63	V
Input Voltage—High	1.7	-	1.9	V
POWER_ON_N assertion time[2]	36.5			ms

1. All values are preliminary and subject to change.
2. Assertion time is the time between POWER_ON_N falling to VGPIO going high.

4.3.1 Power-up Sequence

4.3.1.1 Power On/Off Timing

Figure 4-1 describes the timing sequence for powering the module on and off.

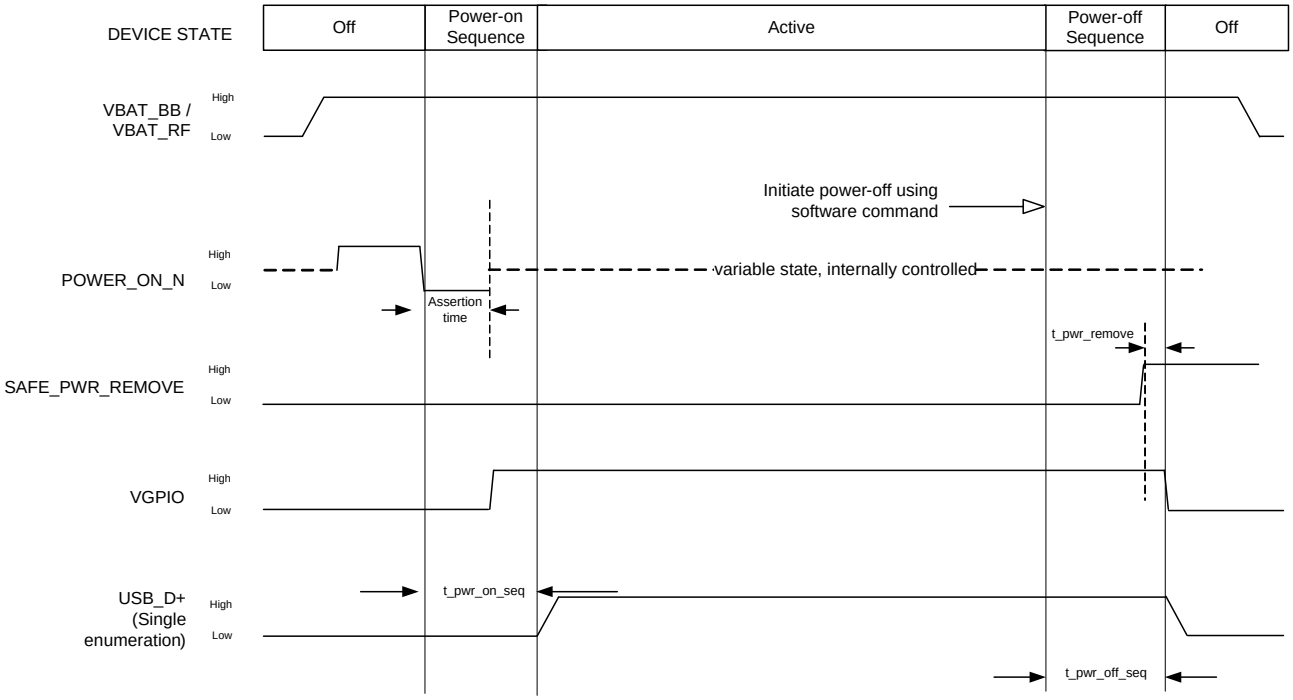

Figure 4-1: Signal timing (POWER_ON_N, and USB Enumeration)

Table 4-4: POWER_ON_N timing parameters

Parameter	Typical	Maximum	Units
t_pwr_on_seq	14.5	15.5	s
t_pwr_off_seq	0.4–5.5[1]	6[1]	s
t_pwr_remove	13	-	ms

1. Preliminary, subject to change

4.3.1.2 USB enumeration

The unit supports single USB enumeration with the host. Enumeration starts within (maximum) t_pwr_on_seq seconds of power-on.

4.3.2 Software-Initiated Power Down

TBD

4.4 Emergency Power Off

The module can be switched off by controlling the RESET_IN_N pin. This must only be used in emergency situations if the system freezes (not responding to commands).

To perform an emergency power off, assert (logic low) RESET_IN_N for at least 32 ms while POWER_ON_N is de-asserted (high level). This action will immediately power down the module.

4.5 USB

The AirPrime WP8548 implements one high-speed USB2.0 Interface, which conforms to the *Universal Serial Bus Specification, Revision 2.0*, except for USB_VBUS implementation (not currently connected internally).

See USB Interface on page 75 for a reference USB schematic.

Table 4-5: USB Pin Descriptions

Pin	Signal name	Direction[1]	Function
12	USB_D-	Input/Output	Differential data interface negative
13	USB_D+	Input/Output	Differential data interface positive
16	Reserved	Input	For compatibility with Sierra Wireless HL devices, connect as indicated in the reference USB schematic.
16	USB_VBUS[2]	Input	USB supply voltage
91	USB_ID	Input	Used for USB_OTG

1. Signal direction with respect to the module. Example: USB_ID is an input to the module from the host.
2. Not currently connected internally, but customer solutions should provide this input for compatibility with future module revisions.

4.6 UART

The AirPrime WP8548 provides two UART interfaces. The primary UART (UART1) is an 8-wire interface and the secondary UART (UART2) is a 4-wire interface.

The UART interfaces are used for data communication between the AirPrime WP8548 modules and a PC or host processor. These interfaces comply with the RS-232 interface.

Flow control is managed using the RTS/CTS signals, or using software XON/XOFF.

Table 4-6 describes the signals used for UART1 and UART2.

Note: UART signals are named with respect to the host device, and directions are listed with respect to the module. For example, UART1_RX is an output from the module to the host.

Table 4-6: UART Pins

Pin	Interface	Name[1]	Direction[2]	Function	If unused
2	UART1	UART1_RI	Output	Ring Indicator Signal incoming calls (voice and data), SMS, etc.	Leave open
3		UART1_RTS	Input	Ready To Send, flow control	Leave open[3]
4		UART1_CTS	Output	Clear To Send, flow control	Leave open
5		UART1_TX	Input	Transmit Data	Leave open
6		UART1_RX	Output	Receive Data	Leave open
7		UART1_DTR	Input (active low)	Data terminal ready Prevents the AirPrime AirPrime WP8548 from entering sleep mode, switches between data mode and command mode, and wakes the module.	Leave open
8		UART1_DCD	Output	Data Carrier Detect Signal data connection in progress	Leave open
9		UART1_DSR	Output	Data Set Ready Signal UART interface is ON	Leave open

Table 4-6: UART Pins

Pin	Interface	Name[1]	Direction[2]	Function	If unused
96	UART2	UART2_TX	Input	Transmit data	Leave open
97		UART2_RX	Output	Receive data	Leave open
98		UART2_RTS	Input	Ready To Send, flow control	Leave open
99		UART2_CTS	Output	Clear To Send, flow control	Leave open

1. Signals are named with respect to the host device. For example, UART1_RX is the signal used by the host to receive data from the module.
2. Signal direction with respect to the module. For example, UART1_RX is an output from the module to the host.
3. If UART1 is implemented as a 2-wire interface, UART1_RTS should be pulled low to disable flow control.

4.7 UIM interface

The AirPrime WP8548 has two physical UIM interfaces—UIM1 and UIM2, which support UIM for WCDMA and GSM.

Both UIM interfaces allow control of external 1.8V/3V UIMs and are fully compliant with GSM 11.11 recommendations concerning UIM functions.

Table 4-7 on page 50 describes the signals used for UIM1 and UIM2.

Table 4-7: UIM Interface Pins

Pin	Interface	Name	Direction[1]	Function	If Unused
26	UIM1	UIM1_VCC	Output	Supply output	Leave open
27		UIM1_CLK	Output	Clock	Leave open
28		UIM1_DATA	Input/Output	Data connection	Leave open
29		UIM1_RESET_N	Output	Reset	Leave open
64		UIM1_DET	Input	Detect UIM	Leave open
55	UIM2	UIM2_VCC	Output	Supply output	Leave open
56		UIM2_DATA	Input/Output	Data connection	Leave open
57		UIM2_RESET_N	Output	Reset	Leave open
58		UIM2_CLK	Output	Clock	Leave open
65		UIM2_DET	Input	Detect UIM	Leave open

1. Signal direction with respect to the module. Examples: UIM1_DET (pin 64) is an input to the module from the host; UIM1_RESET_N (pin 29) is an output from the module to the host.

Figure 4-2 illustrates the recommended implementation of a UIM holder. (For a more detailed UIM schematic, see Figure 5-4 on page 77.)

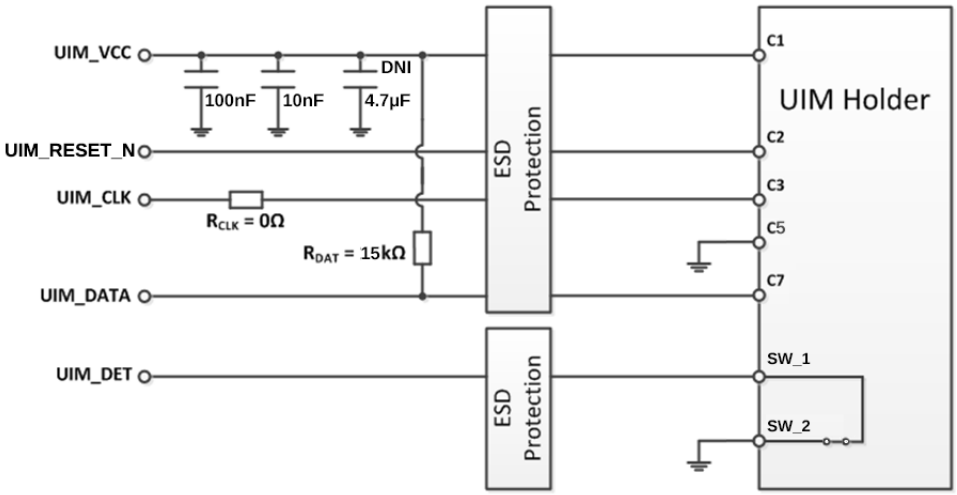

Figure 4-2: Recommended UIM Holder Implementation

The UIM Detect signals (UIM1_DET, UIM2_DET) are used to detect the physical presence of a UIM card in the UIM holder. Each UIM Detect signal has a pull-up internal to the AirPrime WP8548. It should be set to GND when a UIM is not present. All signals near the UIM holder must be ESD-protected.

The UIM Detect signals transition:

- When a UIM is inserted—high (logic 0 to logic 1)
- When a UIM is removed—low (logic 1 to logic 0)

The capacitor and the two resistors, RCLK and RDAT, should be added as placeholders to compensate for potential layout issues. UIM_DAT trace should be routed away from the UIM_CLK trace. Keep the distance between the module and the UIM holder as short as possible.

An ESD device specifically designed for UIM cards is recommended for the UIM1 and UIM2 VCC, RESET_IN_N, CLK, and DAT signals (for example, STMicroelectronics DALC208SC6). For UIM1_DET/UIM2_DET a low leakage ESD suppressor should be selected.

4.8 General Purpose Input/Output (GPIO)

The AirPrime WP8548 defines several GPIOs for customer use, as described in Table 4-8.

Table 4-8: GPIO Pin Description

Pin	Signal Name	Function	If Unused
10	GPIO2[1]	General purpose I/O	Leave open
40	GPIO7		Leave open
41	GPIO8		Leave open
44	GPIO13		Leave open
92	GPIO38[2]		Leave open
93	GPIO39 (future firmware release)		Leave open
94	GPIO40 (future firmware release)		Leave open
95	GPIO41 (future firmware release)		Leave open
100	GPIO34[3]		Leave open
101	GPIO35[3]		Leave open
102	GPIO36[4]		Leave open
103	GPIO37[3]		Leave open
104	GPIO32		Leave open
105	GPIO33		Leave open
109	GPIO42		Leave open
147	GPIO21[1]		Leave open
148	GPIO22		Leave open
149	GPIO23		Leave open
150	GPIO24[1]		Leave open
159	GPIO25		Leave open

1. Pin is ‘wakeable’ (tbc). Can be used to trigger the module to wake up from sleep mode (low power active state).See Wakeup Interrupt (Sleep Mode) on page 53 for details.
2. Can be configured as a wakeup trigger for ULPM. See Power Consumption States on page 28 for details.
3. Accessible via sysfs interface only.
4. Accessible via sysfs interface only, and can be configured as a wakeup trigger for ULPM. See Power Consumption States on page 28 for details.

4.9 Wakeup Interrupt (Sleep Mode)

The following pins can be used to wake the device when it is in sleep mode (low-power active state):

- GPIO2
- GPIO21
- GPIO24
- UIM1_DET
- UIM2_DET

If the device firmware is monitoring these pins while the device is in sleep mode, any transition on these pins will wake the device. (Note: The UIMx_DET pins transition high when a UIM is installed, and low when a UIM is removed.)

Note: These signals wake the device when it is in sleep mode (a low-power ACTIVE state where the module is fully powered). If the device is in ULPM (Ultra Low Power Mode), it is only woken by configured wakeup triggers—see Table 3-6, Supported Power States, on page 29 for details.

4.10 Wakeup Events (ULPM)

The following signals/sources can be configured to wake the device from ULPM (Ultra Low Power Mode):

- GPIO36
- GPIO38
- Timer

Note: These signals wake the device only when it is in ULPM. If the device is in regular sleep mode (a low-power ACTIVE state where the module is fully powered), it can be woken using the signals described in Wakeup Interrupt (Sleep Mode) on page 53.

4.11 Secure Digital IO (SDIO) interface

The AirPrime WP8548 module defines a 3.0V SDIO interface (SD 2.0-compliant) for customer-defined use with SD cards, connection to a Wi-Fi module, etc.

Note: An external 3.0V supply is required to supply power to the SD card.

Table 4-9 describes the signals used for SDIO.

Table 4-9: SDIO pin descriptions

Pin	Signal Name	Direction[1]	Description	If unused	Voltage level
161	SDIO_CMD	Output	SDIO command	Leave Open	3.0V
162	SDIO_CLK	Output	SDIO clock	Leave Open	
163	SDIO_DATA_3	Input/Output	SDIO data bit 3	Leave Open	
164	SDIO_DATA_2	Input/Output	SDIO data bit 2	Leave Open	
165	SDIO_DATA_1	Input/Output	SDIO data bit 1	Leave Open	
166	SDIO_DATA_0	Input/Output	SDIO data bit 0	Leave Open	

1. Signal direction with respect to the module. Example: SDIO_CMD (pin 161) is an output from the module to the host.

4.12 I²C Interface

The AirPrime WP8548 module provides one I²C (Inter-Integrated Circuit) dedicated serial port.

Table 4-10: I²C Interface Pins

Pin	Signal name	Direction	Function	If Unused
1	I2C1_CLK	Input/Output	I²C Clock	Leave open
66	I2C1_DATA	Input/Output	I²C Data	Leave open

The I²C signals are implemented internally as open drain outputs (per the I²C specification) with 2.2 kΩ pull-up resistors to VGPIO.

4.13 VGPIO

The AirPrime WP8548 utilizes 1.8V logic, provided via the VGPIO (GPIO voltage output) pin.

Table 4-11: VGPIO Reference Pin

Pin	Signal name	Direction[1]	Function	If Unused
45	VGPIO	Output	GPIO voltage output	Leave open

1. Signal direction with respect to the module—VGPIO (pin 45) is an output from the module to the host.

Table 4-12: VGPIO electrical characteristics

Parameter	Min	Typ	Max	Unit	Remarks
Voltage level	1.7	1.8	1.9	V	Both active mode and sleep mode
Current capability	-	-	50	mA	Power Management support up to 50 mA output

The VGPIO pin is available when the module is switched ON, and can be used to:

- Pull-up signals such as I/Os
- Supply external digital transistors driving LEDs
- Act as a voltage reference for the ADC interfaces—ADC0–ADC3

4.14 Reset Signal (RESET_IN_N)

The AirPrime WP8548 provides an interface to allow an external application to reset the module.

Table 4-13: RESET_IN_N Pin

Pin	Signal name	Direction[1]	Function	If Unused
11	RESET_IN_N	Input	External Reset Input	Leave open

1. Signal direction with respect to the module—RESET_IN_N (pin 11) is an input to the module from the host.

The RESET_IN_N signal is internally pulled-up with a 40 kΩ resistor. An open collector transistor or equivalent should be used to ground the signal when necessary to reset the module.

To reset the module, a low level pulse must be sent on the RESET_IN_N pin for 32 ms. This will immediately restart the module with the POWER_ON_N signal at low level. (If the POWER_ON_N signal is at high level, the module will be powered off.)

The RESET_IN_N signal will reset the registers of the CPU and reset the RAM memory as well, for the next power on.

Note: Using RESET_IN_N to reset the module could result in memory corruption if used inappropriately. This signal should only be used if the module has become unresponsive and it is not possible to perform a power cycle.

Table 4-14: Reset Timing [1]

Symbol	Parameter	Min	Typ	Max
Trdet	Duration of RESET_IN_N signal before firmware detects it (debounce timer)	-	32 ms	-

Table 4-14: Reset Timing (Continued)[1]

Symbol	Parameter	Min	Typ	Max
Trlen	Duration reset asserted	42 ms	-	∞
Trdel	Delay between minimum Reset duration and internal reset generated	-	500 ms	-

1. All values are preliminary and subject to change

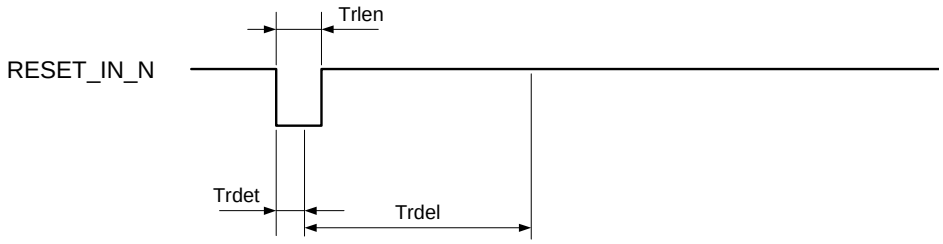

Figure 4-3: Illustration of Reset Timing When RESET_IN_N < Trdel

4.15 Reset Out (RESET_OUT_N)

The AirPrime WP8548 provides a signal that will hold peripheral devices (such as a USB hub, I2C device, etc.) in reset until the power-up sequence is complete.

Table 4-15: RESET_OUT_N Pin

Pin	Signal name	Direction[1]	Function	If Unused
46	RESET_OUT_N	Output	Module reset peripheral device control	Leave open

1. Signal direction with respect to the module—RESET_OUT_N is an output from the module to the host.

When the module is in reset or powering up, the signal is held low to put peripheral devices in reset. Once the power-on sequence is complete, the RESET_OUT_N signal will be turned high to take the peripherals out of reset.

4.16 ADC

The AirPrime WP8548 provides four general purpose ADC (Analog to Digital Converter) inputs, as described Table 4-16 and Table 4-17.

Note: Software support for these inputs will be added in a future firmware revision.

Table 4-16: ADC Interface Pins

Pin	Signal name	Direction[1]	Function	If Unused
24	ADC1	Input	Analog to Digital Converter	Leave open or Ground
25	ADC0	Input	Analog to Digital Converter	Leave open or Ground
107	ADC2	Input	Analog to Digital Converter	Leave open or Ground
108	ADC3	Input	Analog to Digital Converter	Leave open or Ground

1. Signal direction with respect to the module. Example: ADC1 (pin 24) is an input to the module from the host.

Table 4-17: ADC Interface Characteristics[1]

	ADC0 / ADC1 Value	ADC2 / ADC3 Value	Units
Full-scale voltage level	0–1.8	0–1.8	V
Resolution	15	12	bit
Sample rate	tbd	818 tbc	ksps
Voltage error	8 (Typ) 16 (Max)	2 (Typ)	mV

1. All values are preliminary and subject to change

4.17 Digital Audio

The AirPrime WP8548 provides a 4-wire digital audio interface that can be configured as either PCM (Pulse Code Modulation) or I^2S (Inter-IC Sound).

Table 4-18 on page 58 describes the audio interface signals.

Note: Audio availability is firmware-dependent.

Table 4-18: PCM/I²S interface signals [1]

Pin	Signal name	Direction[2]	Function	If Unused
33	PCM_OUT	Output	PCM Data Out The frame “data out” relies on the selected configuration mode.	Leave open
	I2S_OUT	Output	I2S Data Out The frame “data out” relies on the selected configuration mode.	
34	PCM_IN	Input	PCM Data In The frame “data in” relies on the selected configuration mode.	Leave open
	I2S_IN	Input	I2S Data In The frame “data in” relies on the selected configuration mode.	
35	PCM_SYNC	Primary: Input/Output Auxiliary: Output	PCM Sync The frame synchronization signal delivers an 8 kHz frequency pulse that synchronizes the frame data in and the frame data out.	Leave open
	I2S_WS	Output	I2S Word Select The word select clock indicates which channel is currently being transmitted (low cycle indicates left audio channel, high cycle indicates right audio channel).	
36	PCM_CLK	Primary: Input/Output Auxiliary: Output	PCM Clock The frame bit clock signal controls data transfer with the audio peripheral.	Leave open
	I2S_CLK	Output	I2S Clock The frame bit clock signal controls data transfer with the audio peripheral.	

1. All values are preliminary and subject to change
2. Signal direction with respect to the module. Examples: PCM_IN (pin 34) is an input to the module from the host; PCM_OUT (pin 33) is an output from the module to the host.

4.17.1 PCM

Table 4-19 defines the PCM interface configuration.

Table 4-19: PCM Interface Configurations

Element	Primary PCM
Slot configuration	Slot-based
Sync type	Short
Duty cycle	
Clock (in Master mode)	2.048 MHz

Table 4-19: PCM Interface Configurations (Continued)

Element	Primary PCM
Data formats	16-bit linear, 8-bit A-law, 8-bit mu-law
Mode	Master or Slave

4.17.1.1 PCM Data Format

The PCM data is 8 kHz and 16 bits with the following PDM (Pulse-density modulation) bit format:

- PCM_DIN—SDDD DDDD DDDD DDVV
- PCM_DOUT—SDDD DDDD DDDD DDVV

Where:

- S—Signed bit
- D—Data
- V—Volume padding

4.17.1.2 Primary PCM Timing

The following table and drawings illustrate PCM signals timing when operating in primary PCM mode.

Table 4-20: Primary PCM Mode Timing[1,2]

Parameter	Description	Min	Typ	Max	Units
T(sync)	PCM_SYNC cycle time	-	125	-	µs
T(synch)	PCM_SYNC high time	-	488	-	ns
T(syncl)	PCM_SYNC low time	-	124.5	-	µs
T(clk)	PCM_CLK cycle time	-	488	-	ns
T(clkh)	PCM_CLK high time	-	244	-	ns
T(clkl)	PCM_CLK low time	-	244	-	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	-	122	-	ns
T(hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	-	-	tbd	ns
T(sudin)	PCM_IN setup time before falling edge of PCM_CLK	60	-	-	ns
T(hdin)	PCM_IN hold time after falling edge of PCM_CLK	60	-	-	ns
T(pdout)	Delay from PCM_CLK rising to PCM_OUT valid	-	-	60	ns
T(zdout)	Delay from PCM_CLK falling to PCM_OUT HIGH-Z	-	-	60	ns

1. Maximum PCM clock rate is 2.048 MHz.
2. All values are preliminary and subject to change

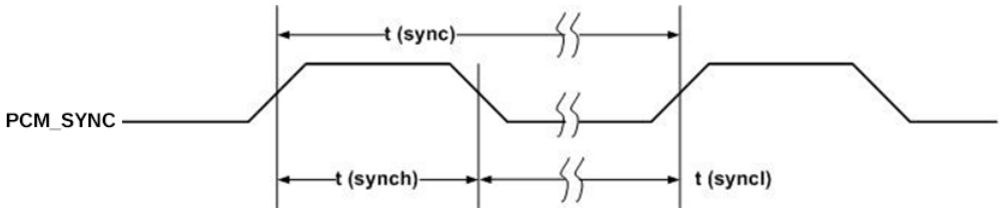

Figure 4-4: PCM_SYNC Timing Diagram (2048 kHz clock)

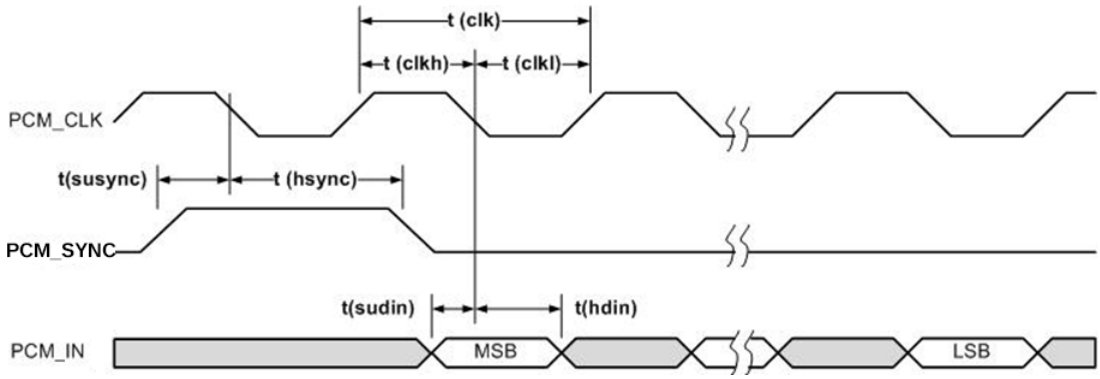

Figure 4-5: PCM Codec to Device Timing Diagram

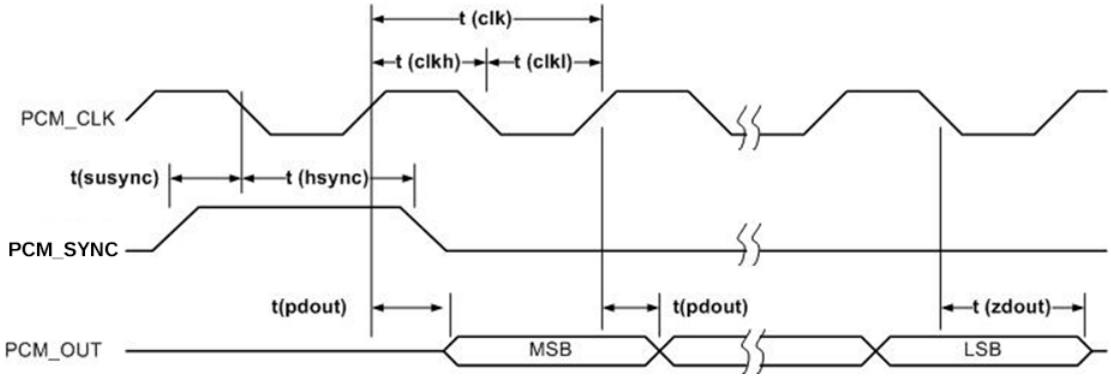

Figure 4-6: Device to PCM Codec Timing Diagram

4.17.2 I²S

The I²S interface can be used to transfer serial digital audio to or from an external stereo DAC/ADC and supports the following features:

- Mode: Master (Slave mode is not supported)
- Sampling rate: 48 kHz
- Bits per frame: 16
- Bit clock: 1536 kHz

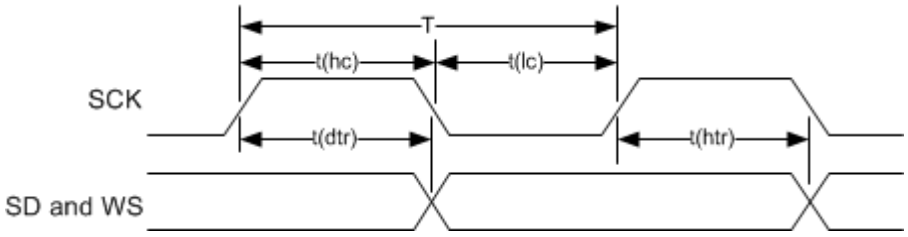

Figure 4-7: I²S Transmitter Timing

Table 4-21: Master transmitter with data rate = 3.072 MHz (±10%)[1]

Parameter	Description	Condition	Min	Typ	Max	Units
T	Clock period	I²S requirement: min T=293	293	326	359	ns
t(hc)	Clock high	I²S requirement: min > 0.35T	120	-	-	ns
t(lc)	Clock low	I²S requirement: min > 0.35T	120	-	-	ns
t(dtr)	Delay	I²S requirment: max < 0.8T	-	-	250	ns
t(htr)	Hold time	I²S requirement: min > 0	100	-	-	ns

1. Maximum sample rate = 48 kHz at 3.072 MHz (16 bits per sample)

4.18 SPI Bus

The AirPrime WP8548 module provides one 4-wire serial peripheral interfaces (SPI1).

The following features are available on the SPI bus:

- Mode: Master (Slave mode is not supported)
- SPI speed from 128 kbps to 26 Mbps in master mode operation
- 4-wire interface
- 4 to 32 bits data length

Table 4-22 on page 61 describes the SPI interface pins.

Table 4-22: SPI pin descriptions

Pin	Signal Name	Direction[1]	Description	Reset State	I/O Type
51	SPI1_MRDY	Output	SPI Master Ready	Z	1V8
52	SPI1_MISO	Input	SPI Master Input/Slave Output (output from slave)	Z	
53	SPI1_CLK	Output	SPI serial clock (output from Master)	Z	
54	SPI1_MOSI	Output	SPI Master Output/Slave Input (output from master)	Z	

1. Signal direction with respect to module. Examples: SPI1_MISO (pin 52) is an input too the module from the host; SPI1_CLK (pin 53) is an output from the module to the host.

4.18.1 SPI Configuration

Table 4-23: SPI Configuration

Operation	Max Speed	SPI-Mode	Duplex	4-wire Type
Master	26 Mb/s	0,1,2,3	Full	SCLK (SPI1_CLK) MOSI (SPI1_MOSI) MISO (SPI1_MISO) SS (SPI1_MRDY)

4.18.2 SPI Waveforms

The following figure shows waveforms for SPI transfer using a 4-wire configuration.

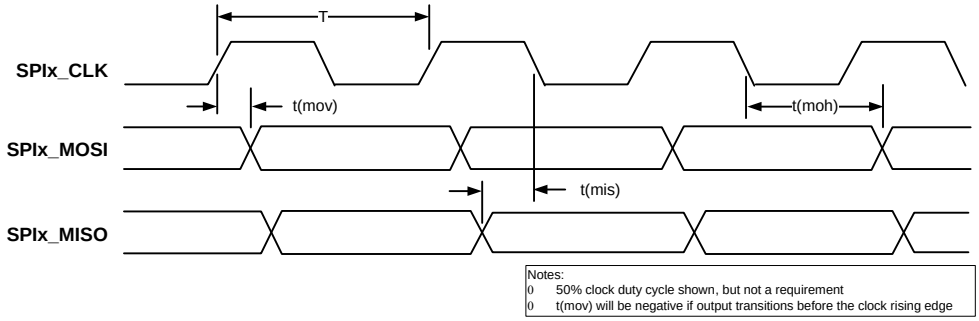

Figure 4-8: 4-Wire Configuration SPI Transfer

Table 4-24: SPI Master Timing Characteristics

Parameter		Min	Typ	Max	Unit
SPI clock frequency		-	-	26	MHz
T	SPI clock period	38	-	-	ns
t(ch)	Clock high	17	-	-	ns
t(cl)	Clock low	17	-	-	ns
t(mov)	Master output valid	-5	-	5	ns
t(mis)	Master input setup	3	-	-	ns
t(moh)	Master output hold	3	-	-	ns
t(tse)	Tri-state enable	-5	-	5	ns
t(tsd)	Tri-state disable	-5	-	5	ns

4.18.3 Application

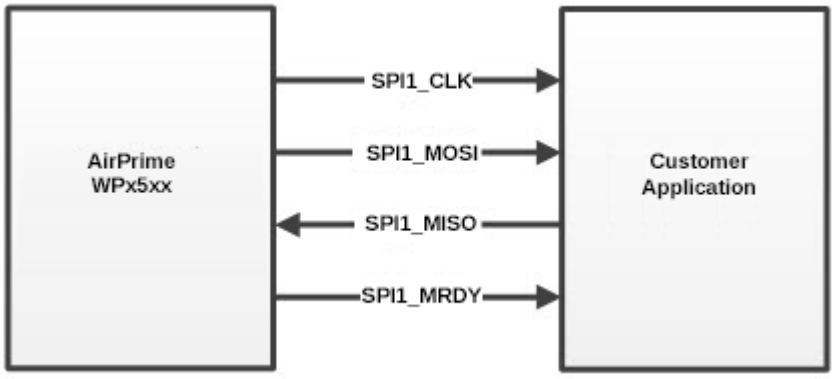

Figure 4-9: Example of 4-wire SPI Bus Application

4.19 HSIC Bus

The AirPrime WP8548 module provides a 2-wire HSIC (High-Speed Inter-Chip) bus.

Table 4-25: HSIC pin descriptions

Pin	Signal Name[1]	Direction[1]	Description	Reset State	I/O Type
14	HSIC_DATA	I/O	HSIC data	Z	1V8
15	HSIC_STRB	I/O	HSIC strobe signal	Z	

1. From host view

4.19.1 HSIC Waveforms

Refer to [1] Inter-Chip USB Supplement to the USB 2.0 Specification Revision 1.0.

4.19.2 Application

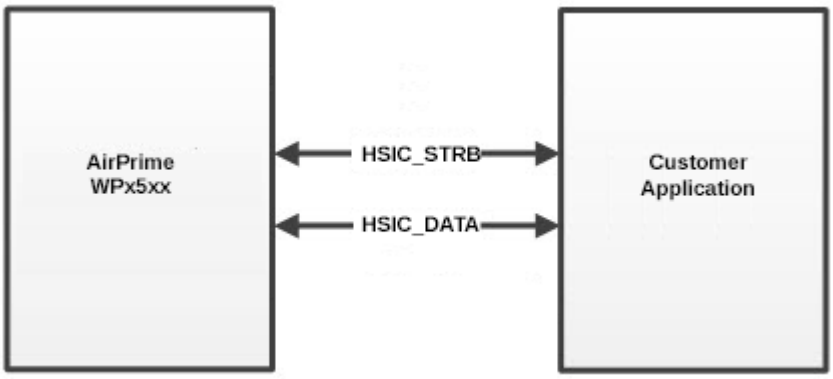

Figure 4-10: Example of 2-wire HSIC Bus Application

Application notes:

- Trace length < 10 cm
- Skew between data and strobe signals < 15 ps
- HSIC_DATA and HSIC_STRB should maintain a 50Ω impedance routing, and isolation between the lines should be maintained

4.20 Clock

The AirPrime WP8548 module supports two digital clock interfaces that are connected directly from the PMIC.

Table 4-26 describes the clock interface pins.

Table 4-26: Clock interface pin descriptions

Pin	Signal name	I/O	I/O type	Description	If Unused
22	SYS_CLK	Output	1.8V	19.2 MHz digital clock output	Leave open
23	SLEEP_CLK	Output	1.8V	32.768 kHz digital clock output	Leave open

4.21 TP1 (Boot Pin)

The TP1 pin is a mandatory test point used by Sierra Wireless for RMA debugging purposes. It is also used as an input that is monitored by the boot loader at power-up. If the signal is low, the boot loader prevents normal power-up and prepares to download firmware by DM port.

Note: Firmware downloads also occur using software tools available on source.sierrawireless.com or over the air using an AirVantage server.

Table 4-27: TP1 Pin Description

Pin	Name	Direction	Function	If Unused
47	TP1	Input	Service (boot load)	Mandatory test point

4.22 Temperature Monitoring

The AirPrime WP8548 provides internal temperature monitoring of the module's baseband thermistor, as detailed below in Figure 4-11 and Table 4-28.

The temperature state can be queried directly, and unsolicited notifications of temperature state transitions can be received by using:

- AT!PATEMP—Display the current temperature state (normal, hi or low warning, hi or low critical)
- AT+WUSLMSK—Enable unsolicited notifications for !PATEMP, to be received over the AT port whenever the state changes.

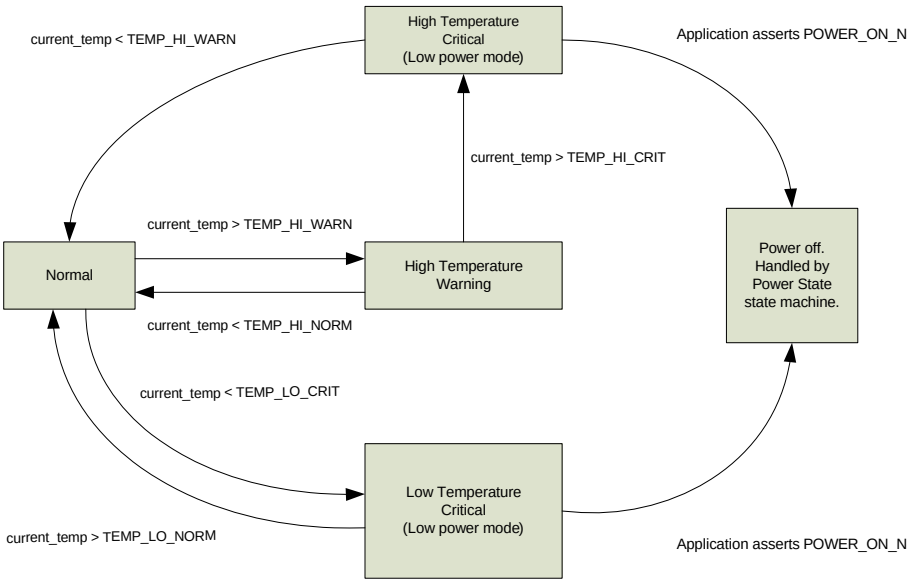

Figure 4-11: Temperature Monitoring State Machine

Table 4-28: Temperature Monitoring States [1]

State	Description	Threshold	Default Temp value (C)	Functionality
Normal	Baseband thermistor is between	TEMP_HI_NORM	+100	All
		TEMP_LO_NORM	-40	
High Temperature Warning	Baseband thermistor has exceeded	TEMP_HI_WARN	+110	All
High Temperature Critical	Baseband thermistor has exceeded	TEMP_HI_CRIT	+120	Low Power Mode
Low Temperature Critical	Baseband thermistor has descended past	TEMP_LO_CRIT	-45	Low Power Mode

1. All values are preliminary and subject to change

To restore full operation, the baseband thermistor's temperature reading must be within the normal or high temperature warning state thresholds.

4.23 Test Pins

Sierra Wireless requires test points on the customer application for Sierra Wireless RMA and debug service.

Table 4-29: Test Pin Descriptions

Pin	Name	Function	If Unused
236	J1	Test point	Mandatory test point
237	J2	Test point	Mandatory test point
238	J3	Test point	Mandatory test point
239	J4	Test point	Mandatory test point
240	J5	Test point	Mandatory test point
241	J6	Test point	Mandatory test point
242	J7	Test point	Mandatory test point
243	J8	Test point	Mandatory test point
244	J9	Test point	Mandatory test point

4.24 Antenna control

Note: Antenna control signals support is optional.

The AirPrime WP8548 provides four output signals that can be used for host designs that incorporate tunable antennas.

The command AT!ANTSEL is used to configure the device to drive the GPIOs high or low, as required, for specific bands.

Table 4-30: Antenna Control Signals

Pin	Name	Direction[1]	Function	If Unused
153	ANT_CNTL0	Output	Customer-defined external switch control for tunable antennas	Leave open
154	ANT_CNTL1	Output		Leave open
155	ANT_CNTL2	Output		Leave open
156	ANT_CNTL3	Output		Leave open

1. Signal direction with respect to module. Examples: ANT_CNTL0 (pin 153) is an output from the module to the host.

4.25 Indication Interfaces

The AirPrime WP8548 module provides several indication interfaces that deliver notifications when specific events occur. These interfaces include:

- Tx Activity Indicator (TX_ON) on page 67
- WWAN_LED_N on page 68
- WAKE_ON_WWAN on page 68
- Ring Indicator on page 69
- SAFE_PWR_REMOVE on page 69
- UIM1_DET/UIM2_DET on page 69

4.25.1 Tx Activity Indicator (TX_ON)

The AirPrime WP8548 module provides a digital output signal to indicate the occurrence of Tx activity.

Table 4-31: Tx Activity Indicator States

Pin	Signal name	Direction[1]	I/O type	Module state	Signal State
60	TX_ON	Output	1.8V	During Tx activity	High
				No Tx	Low

1. Signal direction with respect to module—TX_ON (pin 60) is an output from the module to the host.

4.25.2 WWAN_LED_N

The AirPrime WP8548 provides an LED control output signal pad. This signal is an open drain output.

Table 4-32: LED Interface Pin

Pin	Signal name	Direction[1]	Voltage / Current	Function	If Unused
106	WWAN_LED_N	Output	• Voltage (max)=VBAT_BB + 0.5 V • Maximum current sink capability=300 mA	LED driver control	Leave open

1. Signal direction with respect to module—WWAN_LED_N (pin 106) is an output from the module to the host.

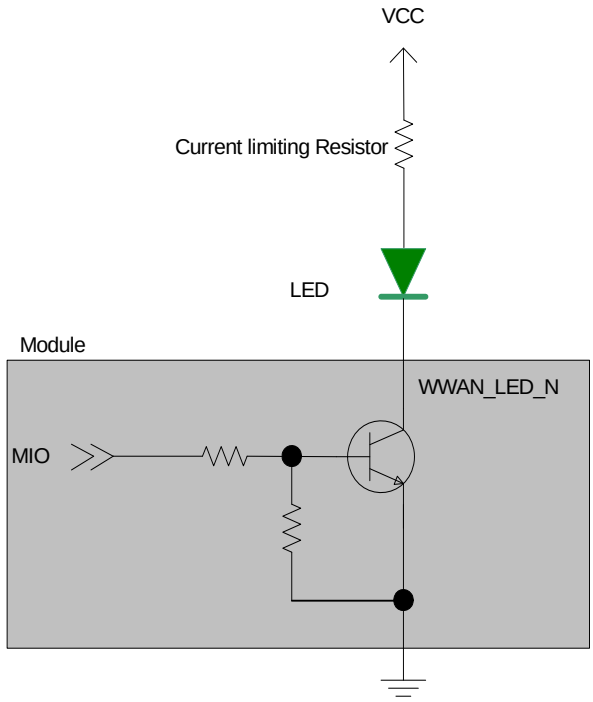

Figure 4-12: LED Reference Circuit

4.25.3 WAKE_ON_WWAN

Note: Host support for WAKE_ON_WWAN signal is optional.

The AirPrime WP8548 drives WAKE_ON_WWAN high to wake the host when specific events occur.

See Figure 4-13 on page 69 for a recommended implementation.

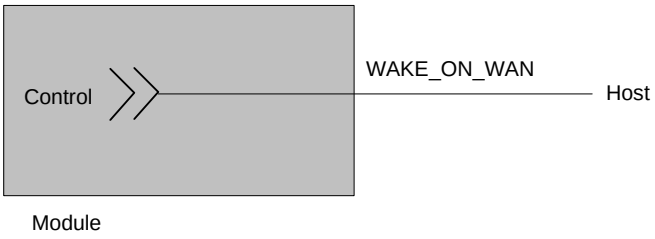

Figure 4-13: Recommended WAKE_ON_WWAN Connection

4.25.4 Ring Indicator

The ring indicator (UART1_RI) may be used to notify an external application of several events such as an incoming call, timer expiration, or incoming SMS. The AirPrime WP8548 pulses the signal high when an event occurs.

Table 4-33: UART1_RI Pin

Pin	Name	Direction[1]	Function	If unused
2	UART1_RI	Output	Ring Indicator Signal incoming calls (voice and data), SMS, etc.	Leave open

1. Signal direction with respect to the module—UART1_RI (pin 2) is an output from the module to the host.

For additional details, refer to the Legato API documentation for Legato.io.

4.25.5 SAFE_PWR_REMOVE

The SAFE_PWR_REMOVE signal is used by the AirPrime WP8548 to indicate to the host device that VBAT_BB/VBAT_RF can be removed. The signal is driven high when it is safe to remove the power supply.

4.25.6 UIM1_DET/UIM2_DET

The UIM Detect signals (UIM1_DET, UIM2_DET) are used to detect the physical presence of UIM cards in the UIM holders. Each UIM Detect signal has a pull-up internal to the AirPrime WP8548. It should be set to GND when a UIM is not present. All signals near the UIM holder must be ESD-protected.

The UIM Detect signals transition:

- When a UIM is inserted—high (logic 0 to logic 1)
- When a UIM is removed—low (logic 1 to logic 0)

4.26 DR_SYNC

The AirPrime WP8548 provides DR_SYNC, an output used for GPS dead reckoning synchronization.

The module pulses the DR_SYNC signal once every integer GPS second. While position fixes are occurring, the DR_SYNC pulse is aligned precisely with the GPS time. When a position fix cannot be made (for example, when a vehicle has entered a tunnel), the module continues to pulse the DR_SYNC signal every second while the level of uncertainty of the GPS time is low. When the uncertainty level is high, the module stops pulsing the signal.

Table 4-34: DR_SYNC Pin details

Pin	Signal name	Direction[1]	Function	If Unused
42	DR_SYNC	Output	GPS dead reckoning sync signal	Leave open

1. Signal direction with respect to the module—DR_SYNC (pin 42) is an output from the module to the host.

4.27 W_DISABLE_N—Wireless Disable

Note: Host support for wireless disable signals is optional.

The host device uses W_DISABLE_N (pin 151) to enable / disable the WWAN or radio modem. When disabled, the modem cannot transmit or receive information.

Letting this signal float high allows the module to operate normally. The pin has an internal pull-up resistor. See Figure 4-14 for a recommended implementation.

When integrating with your host device, keep the following in mind:

- The signal is an input to the module and should be driven LOW only for its active state (controlling the power state); otherwise it should be floating or (High impedance). It should never be driven to a logic high level. The module has an internal pull-up resistor to an internal 1.8V rail, so if the signal is floating or (high impedance), then the radio is on.
- If the host never needs to assert this power state control to the module, leave this signal unconnected from the host interface.

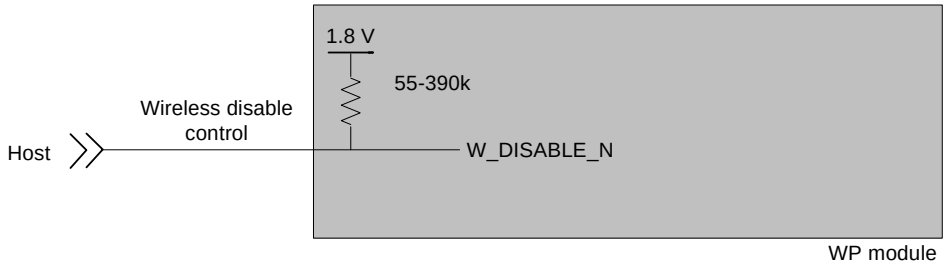

Figure 4-14: Recommended Wireless Disable Connection

5: Routing Constraints and Recommendations

This section describes general routing constraints and recommendations for the AirPrime WP8548 module.

Note: This is a non-exhaustive list of suggested design guidelines. The developer is responsible for deciding whether to implement these guidelines.

5.1 General Rules and Recommendations

Clock and other high-frequency digital signals (e.g. serial buses) should be routed as far as possible from the module's analog signals.

If the application design makes it possible, all analog signals should be separated from digital signals by a ground trace on the PCB.

Tip: *Avoid routing any signals under the module on the application board.*

5.2 PCB Layout Recommendations

Ground pads should be re-flowed on to the host PCB with < 30% voiding to allow effective heat dissipation.

5.3 Power Supply

When designing the power supply, make sure that VBAT_BB/VBAT_RF meet the requirements listed in Power Supply Ratings on page 25.

Careful attention should be paid to the following:

- Power supply quality—PFM, or PSM systems should be avoided; Low ripple, linear regulation or PWM converters are preferred for low noise.
- Capacity to deliver high current peaks in a short time (for pulsed radio emission)
- VBAT_BB/VBAT_RF must support peak currents with an acceptable voltage drop that guarantees the minimum required VBAT_BB/VBAT_RF value.
- VBAT_BB/VBAT_RF signal pads must never exceed the maximum required VBAT_BB/VBAT_RF value, otherwise the module's power amplifier and GPS chipset may be severely damaged.
- A weakly-designed (not robust) power supply could affect EMC performance, the emission spectrum, and the phase error and frequency error.

5.4 Antenna

Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application, or to adapt an existing solution to the application.

For information on routing constraints for the RF circuit, see RF Circuit on page 73.

5.5 PCB Specifications for the Application Board

Sensitive signals (such as audio, UIM, and clocks) should be protected by ground planes/fills. Routing sensitive signals close to noisy signals could result in noise being coupled.

5.6 Recommended PCB Land Pattern

Refer to the AirPrime WP8548 Customer Process Guidelines document, available at http://source.sierrawireless.com.

5.7 Routing Constraints

5.7.1 Power Supply

If the following design recommendations are not followed, phase error (peak) and power loss could occur.

Note: The recommended power supply capacity (Table 3-4 on page 26) is greater than the maximum peak current to provide an operating margin.

- Since the maximum peak current can reach 2.5 A, Sierra Wireless strongly recommends having a large width for the layout of the power supply signal (to avoid voltage loss between the external power supply and VBAT_BB/ VBAT_RF.

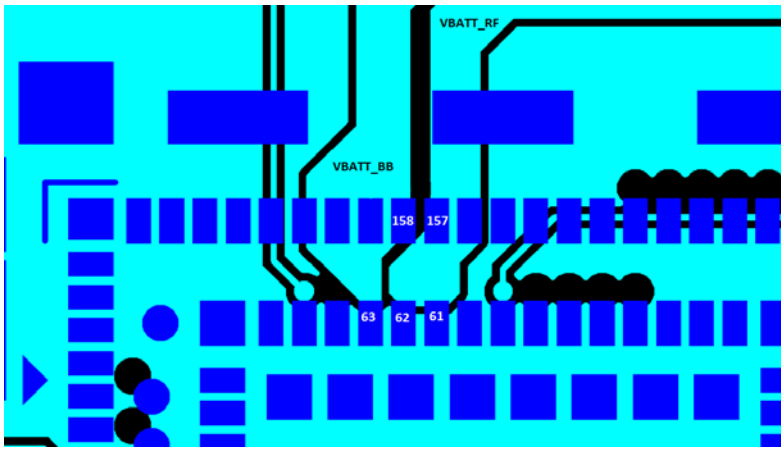

Figure 5-1: Power Supply Routing Example

Note: Figure 5-1 shows separate traces for VBAT_BB and VBAT_RF. If VBAT_BB and VBAT_RF share a single power supply, these traces should be connected.

Note: For optimal decoupling, place the capacitors on the underside of the board, directly under the pins.

- Filtering capacitors (100 nF to 1500 µF) are recommended near the module's power supply.
- Attention should be paid to the ground trace or the ground plane on the application board for the power supply that supplies the module. The ground trace or ground plane, as well as the VBAT trace, must be able to support current peaks.
- If the ground trace between the module and the power supply is a copper plane, make sure it is a solid plane.
- Design routing to make sure total line impedance does not exceed 10 mΩ @ 217 Hz.

5.7.1.1 Ground Plane Connection

The AirPrime WP8548 module requires a solid, central ground plane (with solder mask defined pads) located directly under the module. This will:

- Ensure high current signal returns
- Provide heat dissipation under higher operating temperatures

The ground plane should be connected (with vias) to the reference ground layer of the application board.

5.7.2 UIM Interface

- The length of the tracks between the AirPrime WP8548 and the UIM socket should be as short as possible. Maximum recommended length is 10cm.
- ESD protection is mandatory on the UIM lines unless:
  - An ESIM is being used, or
  - There is no physical access to the UIM
- The decoupling capacitor(s) should be placed as close as possible to the UIM card connector for the UIM1_VCC signal.

5.7.3 RF Circuit

The RF signal must be routed on the application board using tracks with a 50Ω characteristic impedance.

The characteristic impedance depends on the dielectric, the track width and the ground plane spacing.

It is recommended to use stripline design if the RF path is fairly long (more than 3cm), since microstrip design is not shielded. Consequently, the RF (transmit) signal may interfere with neighboring electronic circuits. In the same way, the neighboring electronics (micro-controllers, etc.) may interfere with the RF (receive) signal and degrade the reception performance.

The RF trace on the development board is routed from the AirPrime WP8548 antenna port to the RF connector (IPEX MHF-4). The RF trace is designed as a 50Ω coplanar stripline and its length is 20.7 mm.

The following drawings show the location of the AirPrime WP8548 on the development board, the routing cross-section, and the top view of the RF trace on the development board.

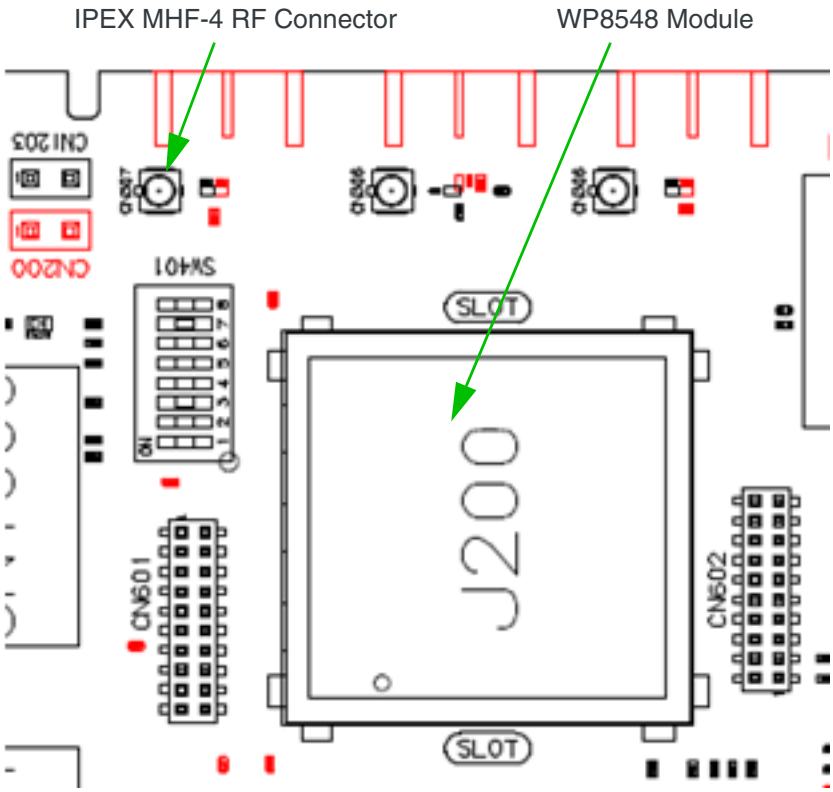

Figure 5-2: Module Location on Development Board

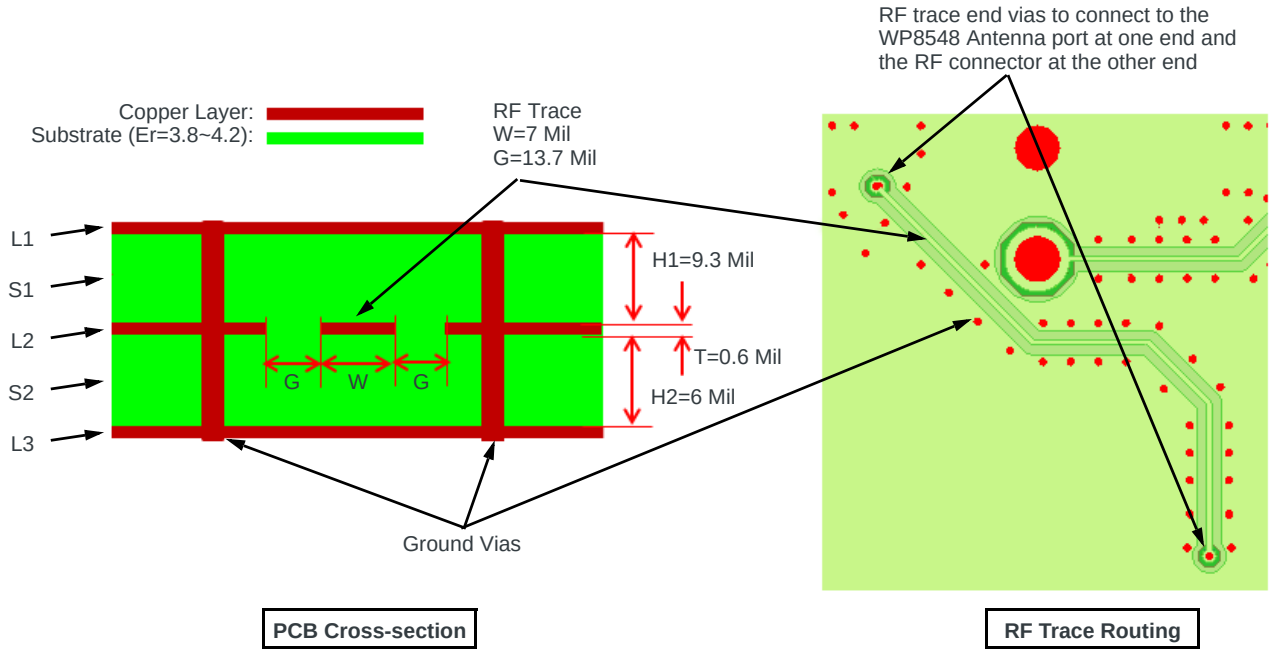

Figure 5-3: Development Board RF Trace Design

5.7.4 USB Interface

When the USB interface is externally accessible, ESD protection is required on the USB_VBUS, USB_D+, and USB_D- signals.

5.8 Thermal Considerations

When transmitting, the AirPrime WP8548 can generate significant amounts of heat (due to the internal Power Amplifier) that must be dissipated in the host device for safety and performance reasons.

The amount of thermal dissipation required depends on the following factors:

- Supply voltage—Maximum power dissipation for these modules can be up to 3 W at voltage supply limits.
- Usage—Typical power dissipation values depend on the location within the host, amount of data transferred, etc.

To enhance heat dissipation:

- Maximize airflow over / around the module
- Locate the module away from other components that generate heat
- Ensure the module is connected to a solid ground plane

5.9 EMC and ESD Recommendations

EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emissions radiated by the application to the RF receiver in the receiver band
- ESD protection—Typically, ESD protection is mandatory for externally accessible signals, including:
  - VBAT_RF/VBAT_BB
  - UIM (if accessible from outside)
  - Serial link
  - USB
  - Antennas
- Length of the UIM interface lines (preferably <10 cm)
- Length of the HSIC interface lines (<10 cm, as required by the HSIC specification)
- EMC protection on audio input/output (filters against 900 MHz emissions)
- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds

Note: The AirPrime WP8548 does not include any protection against over-voltage.

The host device must provide adequate ESD protection on digital circuits and antenna ports as detailed in the following table.

Note: The level of protection required depends on your application.

Table 5-1: ESD specifications [1,2]

Category	Connection	Specification
Operational	RF ports UIM connector USB connector UART connector	IEC-61000-4-2 - Level (Electrostatic Discharge Immunity Test) • ± 6kV Contact • ± 8kV Air
Non-operational	Host connector interface	Unless otherwise specified: • JESD22-A114 ± 2kV Human Body Model • JESD22-A115 ± 200V Machine Model • JESD22-C101C ± 500V Charged Device Model

1. ESD specifications are preliminary, subject to change.
2. ESD protection is highly recommended at the point where the UIM contacts are exposed, and for any other signals that would be subjected to ESD by the user.

5.10 Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Pads of the AirPrime WP8548 to be soldered to the ground plane
- Ensuring proper board layout
- Providing sufficient space around the module for heat dissipation

5.11 Signal Reference Schematics

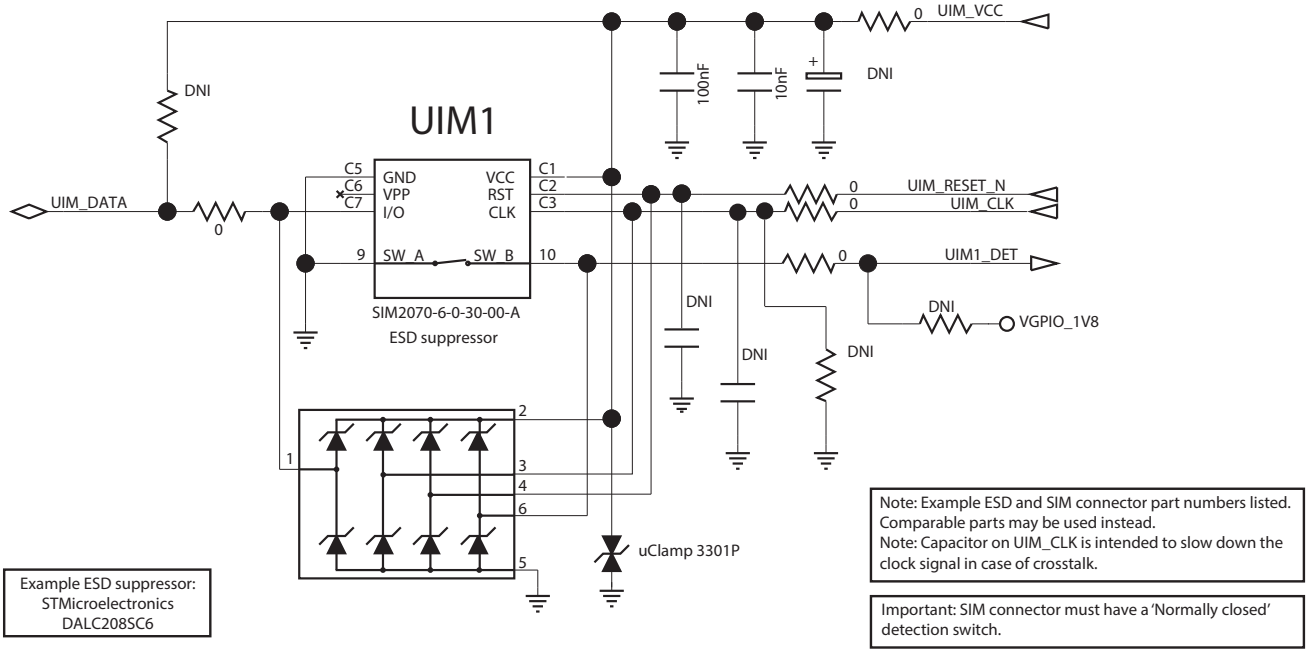

Figure 5-4: UIM Interface

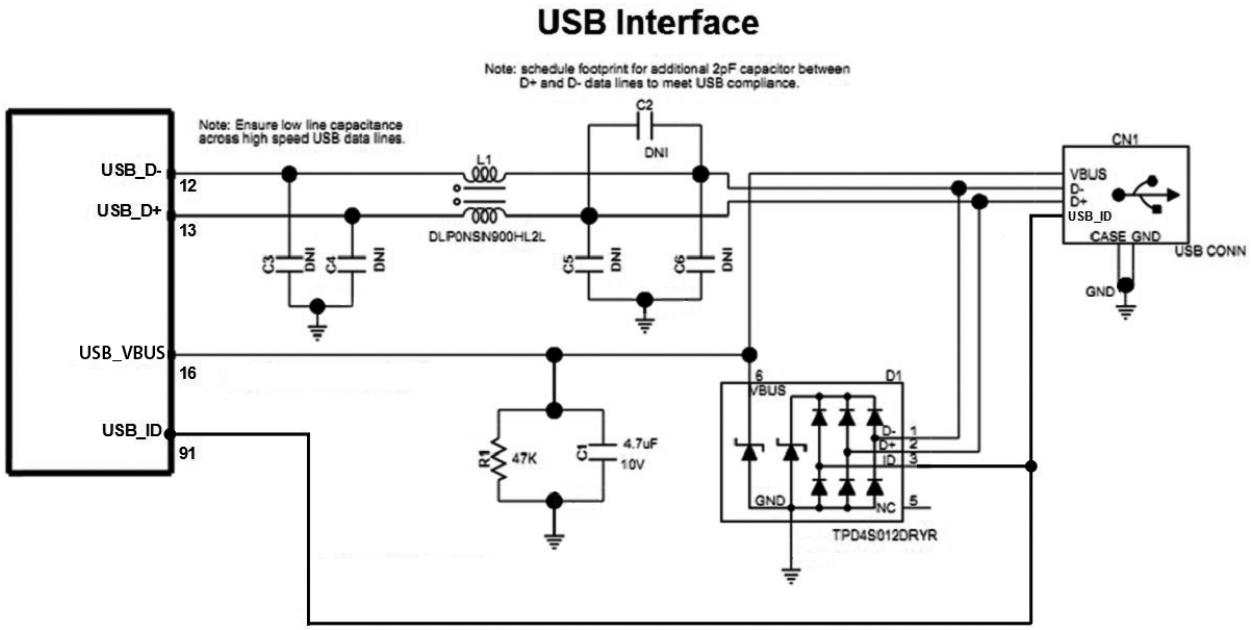

Figure 5-5: USB Interface

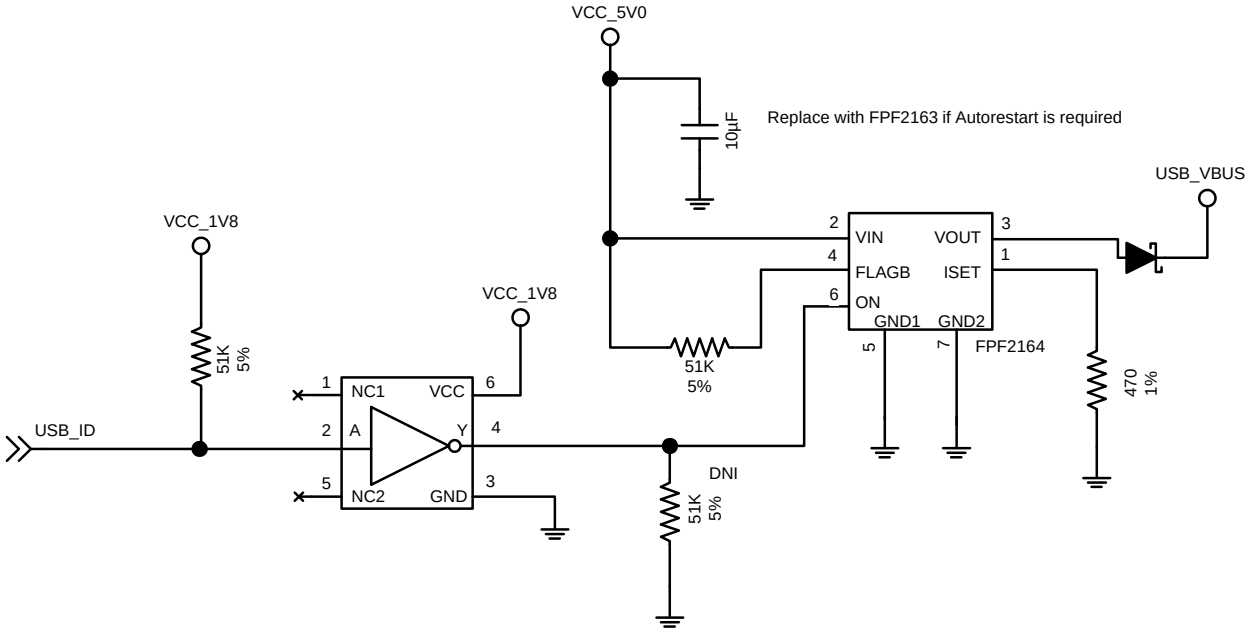

Figure 5-6: USB OTG Interface

6: Software and Tools

6.1 Support Tools

The AirPrime WP8548 is compatible with the following support tools from Sierra Wireless and authorized third parties:

- QXDM from Qualcomm—trace tool that allows users to send error logs to Sierra Wireless.
- SwiLogPlus—trace tool that allows users to send error logs to Sierra Wireless.

6.2 SED (Smart Error Detection)

The AirPrime WP8548 uses a form of SED to track premature module resets. In such cases, the module automatically forces a pause in boot-and-hold mode at power-on to accept an expected firmware download to resolve the problem.

1. Module tracks consecutive resets within 30 seconds of power-on.
2. After a sixth consecutive reset, the module waits in boot-and-hold mode (up to 30 seconds) for a firmware download to resolve the power-cycle problem.

In addition, the Linux QMI SDK includes a RAM dump tool that can be used to extract information to isolate the cause of the premature resets.

6.3 Firmware Upgrade

Firmware upgrades are downloaded to the embedded module over the USB or UART interfaces. Contact your Sierra Wireless account representative for assistance. Refer to Labeling on page 80 for more information on determining the hardware version of your embedded module.

6.4 Operating System Upgrade

The AirPrime WP8548 module's operating system is stored in flash memory and can be easily upgraded.

Tip: *To follow regular changes in the 3GPP standard and to offer a state-of-the-art operating system, Sierra Wireless recommends that the application designed around an embedded module (or embedded module based product) should allow easy operating system upgrades on the embedded module via the recommended firmware download protocol. Therefore, the application shall either allow a direct access to the embedded module USB interface through an external connector or implement any mechanism allowing the embedded module operating system to be downloaded.*

6.5 Labeling

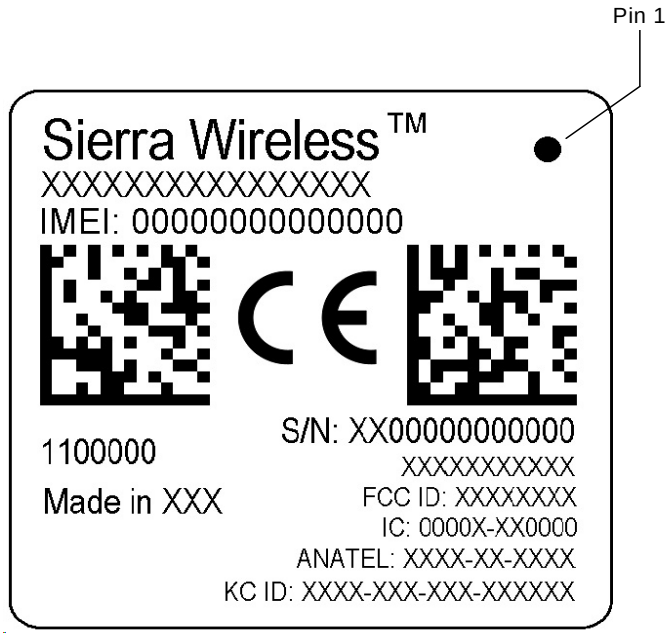

Figure 6-1: Unit Label Example (Contents will vary by SKU)

The AirPrime WP8548 label is non-removable and may contain:

- Product identification (Model name, serial number)
- IMEI or MEID number and barcode
- Fabrication country
- Required regulatory markings (FCC ID, IC certification number, etc., as appropriate)
- Pin 1 indicator

Note: The AirPrime WP8548 supports OEM partner specific label requirements.

7: Debug and Assembly Considerations

7

7.1 Testing Assistance Provided by Sierra Wireless

Sierra Wireless offers optional professional services based assistance to OEMs with regulatory approvals.

7.2 Integration Requirements

When integrating the AirPrime WP8548 module, the following items must be addressed:

- Mounting—Effect on temperature, shock, and vibration performance
- Power supply—Impact on battery drain and possible RF interference
- Antenna location and type—Impact on RF performance
- Regulatory approvals—As discussed in Approval on page 84
- Service provisioning—Manufacturing process

Sierra Wireless provides guidelines for successful AirPrime WP8548 module integration with the document suite and offers integration support services as necessary.

7.3 IOT/Operator

Interoperability and Operator/Carrier testing of the finished system is the responsibility of the OEM. The test process will be determined with the chosen network operator(s) and will be dependent upon your business relationship with them, as well as the product's application and sales channel strategy.

Sierra Wireless offers assistance to OEMs with the testing process, if required.

7.4 Module Testing Recommendations

When testing your integration design:

- Test to your worst case operating environment conditions (temperature and voltage)
- Test using worst case operation (transmitter on 100% duty cycle, maximum power)
- Monitor the module temperature using AT!PATEMP. This command polls a thermistor located near the module's power amplifier (typically the hottest spot on the module).

Note: Make sure that your system design provides sufficient cooling for the module. The RF shield temperature should be kept below 85 °C when integrated to prevent damaging the module's components.

7.5 Serial Link Access

Direct access to the UART1/UART2 serial link is very useful for:

- Testability operations
- Firmware download (for more information on firmware upgrade, see SED (Smart Error Detection) on page 79

Refer to the following figure for a level shifter implementation that allows UART1 serial link access. (A UART2 level shifter would use the corresponding WP8548 UART2 pins—UART2_TX (pin 96), UART2_RX (pin 97), UART2_RTS (pin 98), UART2_CTS (pin 99).)

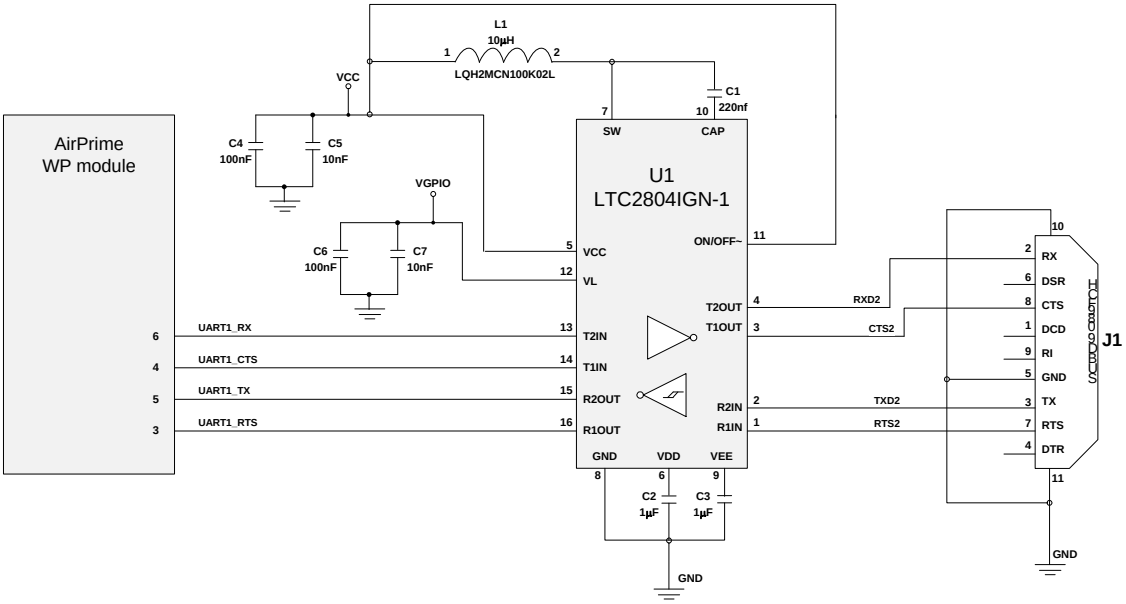

Figure 7-1: Level Shifter Implementation for UART1 Serial Link Access

7.6 RF Output Accessibility

During the integration phase of the AirPrime WP8548, it can be helpful to connect the module to a WCDMA/HSDPA/HSUPA/GSM/GPRS simulator to check critical RF TX parameters and power behavior.

Although the AirPrime WP8548 module has been certified, some parameters may have degraded due to some basic precautions not having been followed (poor power supply, for example). This will not affect the functionality of the product, but the product will not comply with GSM specifications.

The following TX parameters can be checked using a Radio Communication tester:

- Phase & Frequency Error
- Output Power and Burst Time
- Output Spectrum (Modulation and Switching)

The following are available typical Radio Communication testers:

- Rohde & Schwarz: CMU200, CMW500
- Keysight (formerly Agilent): 8960
- Anritsu: MD8475

Because of the high prices associated with Radio Communication testers and the necessary RF know-how to perform simulations, customers can check their applications in the Sierra Wireless laboratories. Contact the Sierra Wireless support team for more information.

8: Approval

8.1 RoHS Directive Compliance

The AirPrime WP8548 module is compliant with RoHS Directive 2011/65/EU which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)".

8.2 Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmental friendly manner.

8.3 Important Notice

Due to the nature of wireless communications, transmission and reception of data can never be guaranteed. Data may be delayed, corrupted (i.e., have errors) or be totally lost. Although significant delays or losses of data are rare when wireless devices such as the Sierra Wireless modem are used in a normal manner with a well-constructed network, the Sierra Wireless modem should not be used in situations where failure to transmit or receive data could result in damage of any kind to the user or any other party, including but not limited to personal injury, death, or loss of property. Sierra Wireless accepts no responsibility for damages of any kind resulting from delays or errors in data transmitted or received using the Sierra Wireless modem, or for failure of the Sierra Wireless modem to transmit or receive such data.

8.4 Safety and Hazards

Do not operate your AirPrime WP8548 Embedded Module:

- In areas where blasting is in progress
- Where explosive atmospheres may be present including refueling points, fuel depots, and chemical plants
- Near medical equipment, life support equipment, or any equipment which may be susceptible to any form of radio interference.

In such areas, the AirPrime WP8548 modem **MUST BE POWERED OFF**. Otherwise, the AirPrime WP8548 modem can transmit signals that could interfere with this equipment.

In an aircraft, the AirPrime WP8548 modem **MUST BE POWERED OFF**. Otherwise, the AirPrime WP8548 modem can transmit signals that could interfere with various onboard systems and may be dangerous to the operation of the aircraft or disrupt the cellular network. Use of a cellular phone in an aircraft is illegal in some jurisdictions. Failure to observe this instruction may lead to suspension or denial of cellular telephone services to the offender, or legal action or both.

Some airlines may permit the use of cellular phones while the aircraft is on the ground and the door is open. The AirPrime WP8548 modem may be used normally at this time.

8.5 Compliance Acceptance and Certification

The AirPrime WP8548 is designed to be compliant with the 3GPP Release 8 UTRA Specification for Mobile Terminated Equipment. Final regulatory and operator certification requires regulatory agency testing and approval with the fully integrated UTRA UE host device incorporating the AirPrime WP8548 module.

The OEM host device and, in particular, the OEM antenna design and implementation will affect the final product functionality, RF performance, and certification test results.

Note: Tests that require features not supported by the AirPrime WP8548 (as defined by this document) are not supported.

8.6 Certification Compliance

TBD

8.6.1 Important Compliance Information for North American Users

The AirPrime WP8548 module, upon commercial release, will have been granted modular approval for mobile applications. Integrators may use the AirPrime WP8548 module in their final products without additional FCC/IC (Industry Canada) certification if they meet the following conditions. Otherwise, additional FCC/IC approvals must be obtained.

1. The end product must use the RF trace design approved with the AirPrime WP8548 module. The Gerber file of the trace design can be obtained from Sierra Wireless upon request.
2. At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.

3. To comply with FCC/IC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed:

   - 4.0 dBi in Cellular band
   - 3.0 dBi in PCS band

Note: Gain values are preliminary and subject to change.

4. The AirPrime WP8548 module may transmit simultaneously with other collocated radio transmitters within a host device, provided the following conditions are met:
   - Each collocated radio transmitter has been certified by FCC/IC for mobile application.
   - At least 20 cm separation distance between the antennas of the collocated transmitters and the user's body must be maintained at all times.
   - The output power and antenna gain in a collocated configuration must not exceed the limits and configurations stipulated in the following table.

Table 8-1: WP8548 Collocated configuration specifications

Device	Technology	Band	Frequency (MHz)	Antenna Gain Limits (dBi)		Maximum conducted power (dBm)
				Standalone	Collocated	
AirPrime WP8548	UMTS	2	1850–1910	3	3	
		5	824–849	4	3	
	GPRS/EDGE	850	824–849	4	3	
		1900	1850–1910	3	3	
Collocated transmitters[1]	WLAN	2.4 GHz	2400–2500			27
		5 GHz	5150–5850			27
	WiMAX		2300–2400			27
			2500–2700			27
			3300–3800			27
	BT		2400–2500			20

1. Valid collocated transmitter combinations: WLAN+BT; WiMAX+BT. (WLAN+WiMAX+BT is not permitted.)

5. A label must be affixed to the outside of the end product into which the AirPrime WP8548 module is incorporated, with a statement similar to the following:
   - **This device contains FCC ID: N7NWP8/IC:2417C-WP8.**
6. A user manual with the end product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC/IC RF exposure guidelines.

The end product with an embedded AirPrime WP8548 module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

Note: If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093 and IC RSS-102.

9: Pinout

The system interface of the AirPrime WP8548 is through the LGA pattern on the bottom of the PCB.

AirPrime WP8548 pins are divided into three functional categories:

- Core functions and associated pins—Cover all the mandatory features for M2M connectivity and will be available by default across all CF3 family of modules. These Core functions are always available and always at the same physical pin locations. A customer platform using only these functions and associated pins is guaranteed to be forward and/or backward compatible with the next generation of CF3 modules.
- Extension functions and associated pins—Bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pin location.
- Custom functions and associated pins—These are module-specific and make use of specific chipset functions and I/Os.

Warning: *Custom features should be used with caution as there is no guarantee that the custom functions available on a given module will be available on other CF3 modules.*

Pins marked as "Leave open" or "Reserved" should not be used or connected.

9.1 Pin Configuration

Figure 9-1 illustrates the pin configuration of the AirPrime WP8548 module.

Figure 9-1: Pin Configuration (bottom view)

9.2 Pin Description

Table 9-1 on page 90 lists detailed information for the LGA pins.

Note: Some pin numbers (112, 126, 127, 137, 138, 235) do not appear in this table because there are no corresponding pads on the module's PCB.

Table 9-1: Pin definitions

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
1	I2C1_CLK	I2C	I/O	1.8V	PU		Leave open	I^2C clock	Core
2	UART1_RI	UART1	O[2]	1.8V		H	Leave open	UART1 Ring indicator	Core
3	UART1_RTS	UART1	I[2]	1.8V		L	Leave open	UART1 Request to send	Core
4	UART1_CTS	UART1	O[2]	1.8V		L	Leave open	UART1 Clear to send	Core
5	UART1_TX	UART1	I[2]	1.8V			Leave open	UART1 Transmit data	Core
6	UART1_RX	UART1	O[2]	1.8V			Leave open	UART1 Receive data	Core
7	UART1_DTR	UART1	I	1.8V		L	Leave open	UART1 Data terminal ready	Core
8	UART1_DCD	UART1	O[2]	1.8V		L	Leave open	UART1 Data carrier detect	Core
9	UART1_DSR	UART1	O[2]	1.8V		L	Leave open	UART1 Data set ready	Core
10	GPIO2[3]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
11	RESET_IN_N	Control signal	I	1.8V	PU	L	Leave open	Input reset signal	Core
12	USB_D-	USB	I/O				Leave open	USB Data negative	Core
13	USB_D+	USB	I/O				Leave open	USB Data positive	Core
14	HSIC_DATA	HSIC	I/O				Leave open	High Speed Inter-Chip Data	Extension
15	HSIC_STRB	HSIC	I/O				Leave open	High Speed Inter-Chip Strobe	Extension
16	USB_VBUS[4]	USB	I	5V			Mandatory connection (Connect to USB_VBUS, or if unavailable, connect to VBAT_BB)	USB power supply	Core
17–20	Reserved	No Connection					See footnote[5].		Extension
21	BAT_RTC	Power	I/O				Leave open	Power supply for RTC backup	Extension
22	SYS_CLK	Clock	O				Leave open	19 MHz digital clock output	Extension
23	SLEEP_CLK	Clock	O				Leave open	32.768 kHz digital clock output	Extension

Table 9-1: Pin definitions (Continued)

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
24	ADC1	ADC	I				Leave open	Analog to digital conversion	Core
25	ADC0	ADC	I				Leave open	Analog to digital conversion	Core
26	UIM1_VCC	UIM1	O	1.8V/3V			Mandatory connection	1.8V/3V UIM1 Power supply	Core
27	UIM1_CLK	UIM1	O	1.8V/3V			Mandatory connection	UIM1 Clock	Core
28	UIM1_DATA	UIM1	I/O	1.8V/3V			Mandatory connection	UIM1 Data	Core
29	UIM1_RESET_N	UIM1	O	1.8V/3V		L	Mandatory connection	UIM1 Reset	Core
30	GND	Ground	0V	0V			Mandatory connection	Ground	Extension
31	Reserved						See footnote[5].		Extension
32	GND	Ground	0V	0V			Mandatory connection	Ground	Extension
33	PCM_OUT	PCM	O	1.8V			Leave open	PCM data out	Core
	I2S_OUT	I2S	O	1.8V			Leave open	I2S data out	
34	PCM_IN	PCM	I	1.8V			Leave open	PCM data in	Core
	I2S_IN	I2S	I	1.8V			Leave open	I2S data in	
35	PCM_SYNC	PCM	Pri: I/O Aux: O	1.8V			Leave open	PCM sync	Core
	I2S_WS	I2S	O	1.8V			Leave open	I2S word select	
36	PCM_CLK	PCM	Pri: I/O Aux: O	1.8V			Leave open	PCM clock	Core
	I2S_CLK	I2S	O	1.8V			Leave open	I2S clock	
37	GND	RF	0V	0V			Mandatory connection	GNSS antenna ground	Core
38	RF_GNSS	RF					Mandatory connection	RF GNSS input	Extension
39	GND	RF	0V	0V			Mandatory connection	GNSS antenna ground	Core
40	GPIO7	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
41	GPIO8	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
42	DR_SYNC	GPS	O	1.8V			Leave open	GPS dead reckoning sync	Extension
43	EXT_GPS_LNA_EN	Control signal	O	1.8V		H	Leave open	External GNSS LNA enable	Extension

Table 9-1: Pin definitions (Continued)

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
44	GPIO13	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
45	VGPIO	Voltage reference	O	1.8V			Leave open	GPIO voltage output	Core
46	RESET_OUT_N	Control signal	O	1.8V	PU	L	Leave open	Reset	Core
47	TP1 (Boot pin)	Boot	I	1.8V		L	Mandatory test point	Test point 1 • 0—Download mode • Open—Normal mode	Extension
48	GND	RF	0V	0V			Mandatory connection	Main antenna ground	Core
49	RF_MAIN	RF					Mandatory connection	Main RF antenna	Core
50	GND	RF	0V	0V			Mandatory connection	Main antenna ground	Core
51	SPI1_MRDY	SPI1	O	1.8V			Leave open	SPI Master Ready	Core
52	SPI1_MISO	SPI1	I	1.8V			Leave open	SPI Master Input/ Slave Output (output from slave)	Core
53	SPI1_CLK	SPI1	O	1.8V			Leave open	SPI serial clock (output from Master)	Core
54	SPI1_MOSI	SPI1	O	1.8V			Leave open	SPI Master Output/ Slave Input (output from master)	Core
55	UIM2_VCC	UIM2	O	1.8V/3V			Optional connection	UIM2 Power supply	Core
56	UIM2_DATA	UIM2	I/O	1.8V/3V			Optional connection	UIM2 Data	Core
57	UIM2_RESET_N	UIM2	O	1.8V/3V		L	Optional connection	UIM2 Reset	Core
58	UIM2_CLK	UIM2	O	1.8V/3V			Optional connection	UIM2 Clock	Core
59	POWER_ON_N	Control	I	1.8V	PU	L	Mandatory connection	Power On control signal	Core
60	TX_ON	Indication	O	1.8V		H	Leave open	Tx activity indicator	Extension
61	VBAT_RF	Power	I	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	RF power supply (see Power Supply Ratings on page 25)	Core
62	VBAT_RF	Power	I	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	RF power supply (see Power Supply Ratings on page 25)	Core
63	VBAT_BB	Power	I	3.4V (min) 3.7V (typ) 4.3V (max)			Mandatory connection	Baseband power supply (see Power Supply Ratings on page 25)	Core

Table 9-1: Pin definitions (Continued)

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
64	UIM1_DET	UIM1		1.8V			Mandatory connection	Detect UIM1 insertion/removal. (Pin must be open to detect the UIM, or grounded if no UIM is present.)	Core
65	UIM2_DET	UIM2		1.8V			Ground	Detect UIM2 insertion/removal (Pin must be open to detect the UIM, or grounded if no UIM is present.)	Extension
66	I2C1_Data	I2C	I/O	1.8V	PU		Leave open	I^2C data	Core
67–70	GND	Ground	0V	0V			Mandatory connection	Ground	Core
71–90	Reserved	No Connection					See footnote[5].		
91	USB_ID	USB	I				Leave open	Reserved for use with USB OTG	Extension
92	GPIO38[6]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
93	GPIO39 (future firmware release)	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
94	GPIO40 (future firmware release)	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
95	GPIO41 (future firmware release)	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
96	UART2_TX	UART2	I^2	1.8V			Leave open	UART2 Transmit data	Extension
97	UART2_RX	UART2	O^2	1.8V			Leave open	UART2 Receive data	Extension
98	UART2_RTS	UART2	I^2	1.8V			Leave open	UART2 Request To Send	Extension
99	UART2_CTS	UART2	O^2	1.8V			Leave open	UART2 Clear To Send	Extension
100	GPIO34[7]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
101	GPIO35[7]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
102	GPIO36[8]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
103	GPIO37[7]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
104	GPIO32	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
105	GPIO33	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension
106	WWAN_LED_N	Indication	O	VBAT_BB[9]		L	Leave open		Extension
107	ADC2	ADC	I				Leave open		Extension
108	ADC3	ADC	I				Leave open		Extension
109	GPIO42	GPIO	I/O	1.8V			Leave open	General purpose I/O	Extension

Table 9-1: Pin definitions (Continued)

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
110	WAKE_ON_WWAN	Indication	O	1.8V		H	Leave open	Driven high to wake the host when specific events occur.	Extension
111	GND	Ground	0V	0V			Mandatory connection	Ground	Core
113	GND	Ground	0V	0V			Mandatory connection	Ground	Core
114–124	Reserved	No Connection					See footnote[5].		
125	GND	RF	0V	0V			Mandatory connection	GNSS antenna ground	Core
128	GND	RF	0V	0V			Mandatory connection	GNSS antenna ground	Core
129–135	Reserved	No Connection					See footnote[5].		
136	GND	RF	0V	0V			Mandatory connection	Main antenna ground	Core
139	GND	RF	0V	0V			Mandatory connection	Main antenna ground	Core
140–146	Reserved	No Connection					See footnote[5].		
147	GPIO21[3]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
148	GPIO22	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
149	GPIO23	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
150	GPIO24[3]	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
151	W_DISABLE_N	Control	I	1.8V		L		Wireless disable (main RF radio)	Core
152	SAFE_PWR_REMOVE	Indication	O	1.8V		H	Leave open	Indicate to host that Main DC power can be removed	Extension
153	ANT_CNTL0	Antenna control	O	1.8V			Leave open		Extension
154	ANT_CNTL1	Antenna control	O	1.8V			Leave open		Extension
155	ANT_CNTL2	Antenna control	O	1.8V			Leave open		Extension
156	ANT_CNTL3	Antenna control	O	1.8V			Leave open		Extension
157	VBAT_RF	Power	I	3.4V (min) 3.7V (typ) 4.3V (max)			Optional connection	RF power supply (see Power Supply Ratings on page 25)	Core
158	VBAT_BB	Power	I	3.4V (min) 3.7V (typ) 4.3V (max)			Optional connection	Baseband power supply (see Power Supply Ratings on page 25)	Core

Table 9-1: Pin definitions (Continued)

Pin	Signal name	Group	I/O[1]	Voltage	PU/ PD	Active	If unused	Function	Type
159	GPIO25	GPIO	I/O	1.8V			Leave open	General purpose I/O	Core
160	Reserved	No Connection					See footnote[5].		
161	SDIO_CMD	SDIO	O	2.95V			Leave open	SDIO command	Extension
162	SDIO_CLK	SDIO	O	2.95V			Leave open	SDIO clock	Extension
163	SDIO_DATA_3	SDIO	I/O	2.95V			Leave open	SDIO data bit 3	Extension
164	SDIO_DATA_2	SDIO	I/O	2.95V			Leave open	SDIO data bit 2	Extension
165	SDIO_DATA_1	SDIO	I/O	2.95V			Leave open	SDIO data bit 1	Extension
166	SDIO_DATA_0	SDIO	I/O	2.95V			Leave open	SDIO data bit 0	Extension
167–234	GND	Ground	0V	0V			Mandatory connection	Ground	Core
236	J1[10]			1.8V		L	Mandatory test point	Test point	Extension
237	J2[10]			1.8V			Mandatory test point	Test point	Extension
238	J3[10]			1.8V			Mandatory test point	Test point	Extension
239	J4[10]			1.8V			Mandatory test point	Test point	Extension
240	J5[10]			1.8V		L	Mandatory test point	Test point	Extension
241	J6[10]			1.8V			Mandatory test point	Test point	Extension
242	J7[10]			1.8V			Mandatory test point	Test point	Extension
243	J8[10]			1.8V			Mandatory test point	Test point	Extension
244	J9[10]			1.8V			Mandatory test point	Test point	Extension

1. Signal direction with respect to the module (except for UART signals). Examples: PCM_OUT (pin 33) is an output from the module to the host; PCM_IN (pin 34) is an input to the module from the host.
2. (UART signals only) Signal direction with respect to the host. Examples: UART1_RTS (pin 3) is an input to the host from the module; UART1_CTS (pin 4) is an output from the host to the module.
3. Wakeable GPIO. See Wakeup Interrupt (Sleep Mode) on page 53 for details.
4. Not currently connected internally, but customer solutions should provide this input for compatibility with future module revisions.
5. Pins are not connected internally, but are reserved for future use. Leave them unconnected to ensure compatibility with other Sierra Wireless CF3 modules.
6. Can be used as a regular GPIO (future firmware revision), and can be configured as a wakeup trigger for ULPM. See Power Consumption States on page 28 for details.
7. Accessible via sysfs interface only.
8. Accessible via sysfs interface only, and can be configured as a wakeup trigger for ULPM. See Power Consumption States on page 28 for details.
9. Maximum rating is VBAT_BB + 0.5V, with maximum current sink capability of 300 mA.
10. Accessibility restricted to soldered-down modules. Not available for socket-mounted modules.

Table 9-2: RF Pin Information

Signal name	Pin #	Description
RF_GNSS	38	RF GNSS input
RF_MAIN	49	Main RF port (input/output)

Table 9-3: Supply Pin Information

Signal name	Pin #	Description
VBAT_RF	61, 62, 157	RF power supply
VBAT_BB	63, 158	Baseband power supply
BAT_RTC	21	Power supply for RTC backup
USB_VBUS	16	Connected to VBAT_BB

Table 9-4: Ground & Reserved Pin Information

Signal name	Pin #	Description
Ground	30, 32, 37, 39, 48, 50, 67–70, 111, 113, 125, 128, 136, 139, 167–234	Ground connection
Reserved	17–20, 31, 71–90, 114–124, 129–135, 140–146, 160	Pins are not connected internally, but are reserved for future use. Leave them unconnected to ensure compatibility with other Sierra Wireless CF3 modules.

10: Customization

Subject to commercial terms, Sierra Wireless can supply custom-configured modems to facilitate a carrier's network and performance requirements. Sierra Wireless also offers a standard configuration for each country.

Custom configurations are entered into a selector spreadsheet that Sierra supplies. A unique part number is assigned to each custom configuration to facilitate customer ordering.

Table 10-1: Customizable Features

Name	Description	Default
MEP network locked	Mobile Equipment Personalization network locked to only allow use with specific preconfigured PLMNs (UIMs). MMI supports the entry of an unlock code subject to permanent locking feature below.	Off
MEP service provider locked		
Permanent MEP locked	Can block deactivation of MEP locked feature	Off
UIM PUK prompt enable	If enabled, Skylight shows the message “SIM blocked please enter PIN code”.	Disabled. Skylight displays “Contact Service Provider” when SIM PIN is blocked.
Display of IMSI	Display of International Mobile Subscriber Identity via AT+CIMI command	Display enabled
UART baud rate	Default UART speed	115200 bps
UART enabled	Defines whether UART port is enabled by default or not	UART disabled

11: References

For more details, several references can be consulted, as detailed below.

11.1 Web Site Support

Check http://source.sierrawireless.com for the latest documentation available for the AirPrime WP8548.

11.2 Reference Documents

[1] Inter-Chip USB Supplement to the USB 2.0 Specification Revision 1.0

[2] Legato.io for Legato API details

[3] AirPrime WPx5 Series Customer Process Guidelines

12: Abbreviations

Table 12-1: Acronyms and definitions

Acronym or term	Definition
3GPP	3rd Generation Partnership Project
8PSK	Octagonal Phase Shift Keying
ADC	Analog to Digital Converter
AF	Audio-Frequency
API	Application Programming Interface
AT	Attention (prefix for modem commands)
BeiDou	BeiDou Navigation Satellite System A Chinese system that uses a series of satellites in geostationary and middle earth orbits to provide navigational data.
BER	Bit Error Rate—A measure of receive sensitivity
BLER	Block Error Rate
Bluetooth	Wireless protocol for data exchange over short distances
CEP	Circular Error Probable
CF3	Common Flexible Form Factor
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CQI	Channel Quality Indication
CS	Circuit-Switched
	Coding Scheme
CTS	Clear To Send
CW	Continuous waveform
DAC	Digital to Analog Converter
dB	Decibel = 10 x $\log_{10}$ (P1/P2) *P1 is calculated power; P2 is reference power* Decibel = 20 x $\log_{10}$ (V1/V2) *V1 is calculated voltage, V2 is reference voltage*
dBm	A logarithmic (base 10) measure of relative power (dB for decibels); relative to milliwatts (m). A dBm value will be 30 units (1000 times) larger (less negative) than a dBW value, because of the difference in scale (milliwatts vs. watts).
DC	Direct Current

Table 12-1: Acronyms and definitions (Continued)

Acronym or term	Definition
DCD	Data Carrier Detect
DCS	Digital Cellular System A cellular communication infrastructure that uses the 1.8 GHz radio spectrum.
DL	Downlink (network to mobile)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTR	Data Terminal Ready
E-GSM	Extended GSM
EDGE	Enhance Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGPRS	Enhance GPRS
EIRP	Effective (or Equivalent) Isotropic Radiated Power
EMC	Electromagnetic Compatibility
EN	Enable
ERP	Effective Radiated Power
ESD	Electrostatic Discharges
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission The U.S. federal agency that is responsible for interstate and foreign communications. The FCC regulates commercial and private radio spectrum management, sets rates for communications services, determines standards for equipment, and controls broadcast licensing. Consult www.fcc.gov.
FDD	Frequency Division Duplexing
FDMA	Frequency Division Multiple Access
firmware	Software stored in ROM or EEPROM; essential programs that remain even when the system is turned off. Firmware is easier to change than hardware but more permanent than software stored on disk.
FOV	Field Of View
FR	Full Rate
FSN	Factory Serial Number—A unique serial number assigned to the mini card during manufacturing.
Galileo	A European system that uses a series of satellites in middle earth orbit to provide navigational data.
GCF	Global Certification Forum
GLONASS	Global Navigation Satellite System—A Russian system that uses a series of 24 satellites in middle circular orbit to provide navigational data.

Table 12-1: Acronyms and definitions (Continued)

Acronym or term	Definition
GMSK	Gaussian Minimum Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite Systems (GPS, GLONASS, BeiDou, and Galileo)
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System An American system that uses a series of 24 satellites in middle circular orbit to provide navigational data.
GSM	Global System for Mobile communications
Hi Z	High impedance (Z)
Host	The device into which an embedded module is integrated
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
Hz	Hertz = 1 cycle/second
I/O	Input/Output
IC	Industry Canada
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
IMS	IP Multimedia Subsystem—Architectural framework for delivering IP multimedia services.
inrush current	Peak current drawn when a device is connected or powered on
IOT	Interoperability Testing
IS	Interim Standard. After receiving industry consensus, the TIA forwards the standard to ANSI for approval.
LED	Light Emitting Diode. A semiconductor diode that emits visible or infrared light.
LGA	Land Grid Array
LHCP	Left-Hand Circular Polarized
LNA	Low noise Amplifier
MAX	Maximum
MCS	Modulation and Coding Scheme
MHz	Megahertz = 10e6 Hz

Table 12-1: Acronyms and definitions (Continued)

Acronym or term	Definition
MIC	Microphone
MIMO	Multiple Input Multiple Output—wireless antenna technology that uses multiple antennas at both transmitter and receiver side. This improves performance.
MIN	Minimum
MO	Mobile Originated
MT	Mobile Terminated
N/A	Not Applicable
NMEA	National Marine Electronics Association
NOM	Nominal
OEM	Original Equipment Manufacturer—a company that manufactures a product and sells it to a reseller.
PA	Power Amplifier
packet	A short, fixed-length block of data, including a header, that is transmitted as a unit in a communications network.
PBCCH	Packet Broadcast Control Channel
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System A cellular communication infrastructure that uses the 1.9 GHz radio spectrum.
PDN	Packet Data Network
PFM	Power Frequency Modulation
PLL	Phase Lock Loop
PMIC	Power Management Integrated Circuit
PSM	Phase Shift Modulation
PSS	Primary synchronisation signal
PST	Product Support Tools
PTCRB	PCS Type Certification Review Board
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation. This form of modulation uses amplitude, frequency, and phase to transfer data on the carrier wave.
QPSK	Quadrature Phase-Shift Keying
RAM	Random Access Memory

Table 12-1: Acronyms and definitions (Continued)

Acronym or term	Definition
RAT	Radio Access Technology
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RSE	Radiated Spurious Emissions
RSSI	Received Signal Strength Indication
RST	Reset
RTC	Real Time Clock
RTS	Request To Send
RX	Receive
SCLK	Serial Clock
SED	Smart Error Detection
Sensitivity (Audio)	Measure of lowest power signal that the receiver can measure.
Sensitivity (RF)	Measure of lowest power signal at the receiver input that can provide a prescribed BER/BLER/SNR value at the receiver output.
SIM	Subscriber Identity Module. Also referred to as USIM, UIM, or UICC.
SKU	Stock Keeping Unit—identifies an inventory item: a unique code, consisting of numbers or letters and numbers, assigned to a product by a retailer for purposes of identification and inventory control.
SMS	Short Message Service
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SPK	Speaker
SW	Software
TBC	To Be Confirmed
TBD	To Be Determined
TIA/EIA	Telecommunications Industry Association / Electronics Industry Association. A standards setting trade organization, whose members provide communications and information technology products, systems, distribution services and professional services in the United States and around the world. Consult www.tiaonline.org.
TIS	Total Isotropic Sensitivity
TP	Test Point
TRP	Total Radiated Power

Table 12-1: Acronyms and definitions (Continued)

Acronym or term	Definition
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UE	User Equipment
UICC	Universal Integrated Circuit Card (Also referred to as a SIM, USIM, OR UIM card.)
UIM	User Identity Module
UL	Uplink (mobile to network)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module (UMTS)
USSD	Unstructured Supplementary Services Data
UTRA	UMTS Terrestrial Radio Access
VBAT-BB	Baseband power supply
VBAT-RF	RF power supply
VCC	Supply voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access (also referred to as UMTS)
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network
ZIF	Zero Intermediate Frequency

13: Safety Recommendations (For Information Only)

For the efficient and safe operation of your GSM application based on the AirPrime WP8548 Embedded Module, please read the following RF safety information carefully.

13.1 RF Safety

13.1.1 General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

13.1.2 Exposure to RF Energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy, there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

13.1.3 Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

- If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.
- Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

13.1.4 Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

13.2 General Safety

13.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- Give full attention to driving,
- Pull off the road and park before making or answering a call if driving conditions so require.

13.2.2 Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

13.2.3 Vehicle Electronic Equipment

Check with your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

13.2.4 Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

13.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

13.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

13.2.7 Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

13.2.8 Potentially Explosive Atmospheres

Turn your terminal OFF when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.


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