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PRODUCT BULLETIN

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ISSUE DATE: 08-Apr-2016
NOTIFICATION: 17140
TITLE: i.MX 6SoloX Errata Documentation Revision Update to Rev 1
EFFECTIVE DATE: 09-Apr-2016

DEVICE(S)

MPN
KCIMX6X1CVK08AB
LPCW431924
MCIMX6X1AVK08AB
MCIMX6X1AVO08AB
MCIMX6X1CVK08AB
MCIMX6X1CVO08AB
MCIMX6X1EVK10AB
MCIMX6X1EVO10AB
MCIMX6X2AVN08AB
MCIMX6X2AVN10AB
MCIMX6X2CVN08AB
MCIMX6X2EVN10AB
MCIMX6X2EVN10ABR
MCIMX6X3CVK08AB
MCIMX6X3CVN08AB
MCIMX6X3CVO08AB
MCIMX6X3CVO10AB
MCIMX6X3EVK10AB
MCIMX6X3EVK10ABR
MCIMX6X3EVN10AB
MCIMX6X3EVO10AB
MCIMX6X4AVM08AB
MCIMX6X4CVM08AB
MCIMX6X4EVM10AB

AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

The i.MX 6SoloX errata documentation has been updated to include additional errata that have been identified as well as updates to existing errata.

The updated errata documentation is attached to this notice and can be found at:
www.nxp.com/files/32bit/doc/errata/IMX6SXCE.pdf

Additions to the errata are as follows:

- ERR003741: ARM/PL310: 729815—The “High Priority for SO and Dev reads” feature can cause Quality of Service issues to cacheable read transactions
- ERR004324: ARM/MP: 761319—Ordering of read accesses to the same memory location may not be ensured
- ERR005200: ARM/MP: 765569—Prefetcher can cross 4 KB boundary if offset is programmed with value 23
- ERR005829: FlexCAN: FlexCAN does not transmit a message that is enabled to be transmitted in a specific moment during the arbitration process
- ERR007006: ARM/MP:794072-- Short loop including a DMB instruction might cause a denial of service
- ERR007881: USB: Timeout error in Device mode
- ERR008506: ROM: Incorrect NAND BAD Block Management
- ERR009535: eCSPI: Burst completion by SS signal in slave mode is not functional
- ERR009541: PXP: CSC2 does not perform RGB to YCbCr and RGB to YUV conversions
- ERR009572: RDC: Access to RDC registers will cause the CPU to hang if the PCIE_DISABLE fuse has disabled PCIe
- ERR009596: MMDC: ARCR_GUARD bits of MMDC Core AXI Re-ordering Control register (MMDC_MAARCR) doesn’t behave as expected
- ERR009606: eCSPI: In master mode, burst lengths of 32n+1 will transmit incorrect data
- ERR009636: MMDC: Random data corruption during reads from DDR memory
- ERR009742: ARM: 795769 - “Write Context ID" event is updated on read access
- ERR009743: ARM: 799770 - DBGPRSR Sticky Reset status bit is set to 1 by the CPU debug reset instead of by the CPU non-debug reset
- ERR009858: ARM/PL310: 796171 When data banking is implemented, data parity errors can be incorrectly generated

Refer to the errata document IMX6SXCE for more details.

REASON FOR CHANGE

The errata documentation for the i.MX 6SoloX product line has been updated.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

The errata describes existing conditions identified on current production devices. There are potential hardware and/or software implications to customers.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Support Case. Be aware that after you select this link to enter your request, you must choose the topic "Product Change Notification" once on the Salesforce page.

For sample inquiries - please go to www.nxp.com

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT:
17140_IMX6SXCE__Rev1.pdf
