# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MIC/14/8685
Dated 03 Oct 2014

**Conversion to High Density Matrix Leadframe - LQFP 64 10x10 products listed below**

### Table 1. Change Implementation Schedule

| | |
|---|---|
| Forecasted implementation date for change | 10-Feb-2015 |
| Forecasted availability date of samples for customer | 10-Jan-2015 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 10-Jan-2015 |
| Estimated date of changed product first shipment | 10-Feb-2015 |

### Table 2. Change Identification

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | LQFP 64 10x10 package products |
| Type of change | Assembly additional location |
| Reason for change | To increase assembly capacity |
| Description of the change | ST Microcontrollers Division has decided to add a High Density Matrix leadframe line in Muar (Malaysia) assembly site, for LQFP 64 10x10 products listed below. The objective is to increase assembly capacity. The assembly plants and Bill Of Materials are changed as indicated below. |
| Change Product Identification | See indicated below |
| Manufacturing Location(s) | |

**Table 3. List of Attachments**

| | |
|---|---|
| Customer Part numbers list | |
| Qualification Plan results | |

- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

| Customer Acknowledgement of Receipt | PCN MMS-MIC/14/8685 |
|---|---|
| Please sign and return to STMicroelectronics Sales Office | Dated 03 Oct 2014 |
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

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# DOCUMENT APPROVAL

| Name | Function |
|---|---|
| Colonna, Daniel | Marketing Manager |
| Buffa, Michel | Product Manager |
| Narche, Pascal | Q.A. Manager |

# PRODUCT/PROCESS CHANGE NOTIFICATION

## Conversion to High Density Matrix Leadframe – LQFP 64 10x10 products listed below

### MMS - Microcontrollers Division (MCD)

Dear Customer,

ST Microcontrollers Division has decided to add a High Density Matrix leadframe line in Muar (Malaysia) assembly site, for LQFP 64 10x10 products listed below.

The objective is to increase assembly capacity.

**What are the changes?**

On LQFP 64 10x10 products listed below, the assembly plants and Bill Of Materials are as below:

| Current | | |
|---|---|---|
| Assembly site | Bill Of Materials (BOM) | |
| Muar (Malaysia) | Leadframe | PrePlated Frame (PPF) |
| | Die attached material | Hitachi EN4900 |
| | Molding compound | Sumitomo G700F |
| | Wire | Gold 1.0mil |
| STATS ChipPAC Shanghai (China) | Leadframe | Pure Sn |
| | Die attached material | Ablestik 3230 |
| | Molding compound | Sumitomo G700E |
| | Wire | Gold 0.8mils |

| New | | |
|---|---|---|
| Assembly site | Bill Of Materials (BOM) | |
| Muar (Malaysia) | Leadframe | Pure Sn |
| | Die attached material | Hitachi EN4900GC |
| | Molding compound | Sumitomo G700LS |
| | Wire | Gold 0.8mils |

**Why ?**

ST Microcontrollers Division add a LQFP 64 10x10 products on High Density Matrix leadframe line in Muar (Malaysia) assembly site, to increase assembly capacity.

**When ?**

The production on the new leadframe will start from week 07 2015.

**How will the change be qualified?**

This change will be qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard. You can find below Qualification Plan.

**What is the impact of the change?**

**- Form:** no change

**- Fit:** no change

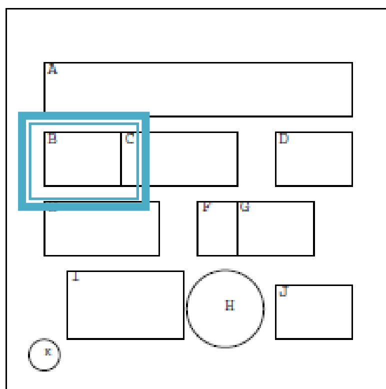
**- Function:** no change

**How can the change be seen?**

Traceability of the change is ensured by ST internal tools.

1/ For products listed below changing from STATS ChipPAC Shanghai (China) to Muar (Malaysia) assembly site:

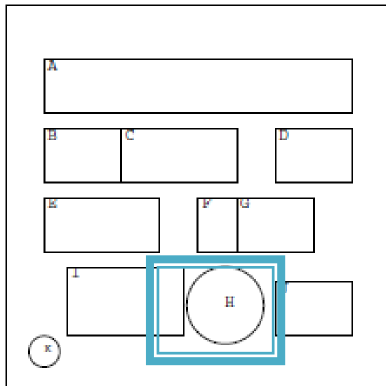
The marking instruction indicated on the products is changing from:




B : Assembly plant changes from GH to 99

2/ For products listed below remaining at Muar (Malaysia) assembly site:

The marking instruction indicated on the products is changing from:




H : Second level interconnect changes from e4 to e3

We remain available to discuss any concern that you may have regarding this Product Change Notification.

With our sincere regards.

Michel Buffa
Microcontroller Division General Manager

Commercial products impacted:

| Commercial Product | Assembly Plant | |
|---|---|---|
| | Current | New |
| STM32F100RCT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F100RCT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101R8T6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101R8T6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RBT6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RBT6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RCT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RCT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RDT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RDT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RDWOWTR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F101RET6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F102R8T6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F102RBT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F102RBT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F102RCT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103R8T6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103R8T6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103R8T7 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RBT6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RBT6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RBT7 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RBT7TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RCT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RCT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RCT7 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RCUVWTR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RDT6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RDT6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RET6 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RET6TR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32F103RET7 | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM32P101RCMBR | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207R6T6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207R6T6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207R8T3 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |

| | | |
|---|---|---|
| STM8S207R8T3TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207R8T6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207R8T6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207RBT3 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207RBT3TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207RBT6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S207RBT6TR | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S208R8T6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S208RBT3 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8S208RBT6 | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |
| STM8SP207R6MEY | Muar (Malaysia) | Muar (Malaysia) |
| | STATS ChipPAC Shanghai (China) | Muar (Malaysia) |

# RERMCD 1411 RELIABILITY PLAN

**Qualification of :**

***New BOM with High density leadframe LQFP10*10 at ST Muar for Microcontrollers devices***

| | |
|---|---|
| **Qualification Reference:** | **RERMCD1411** |
| **Issued on:** | **Aug 11, 2014** |
| **Assembly Plant:** | **ST Muar** |
| **Assembly Line:** | **LQFP** |
| **Devices:** | **STM32/ STM8S** |
| **Package / Process:** | **10x10 (64 Leads)** |
| **Lead termination:** | **Pure Sn** |
| **Die attach:** | **Hitachi EN4900GC** |
| **Mold compound:** | **Sumitomo G700LS** |
| **Wire material/ diameter:** | **Gold 0.8mils** |
| **MSL:** | **MSL3** |

**Purpose**

Qualification of new BOM for LQFP10x10- 64 leads at ST Muar.

**Test Vehicles :**

| Package | Device (Partial RawLine Code) | Diffusion Process fab | Number of Lots |
|---|---|---|---|
| **LQFP 10x10 64 leads** | STM32F (5W*410) | 0.18µm- TSMC | **1** |
| | STM32F (5W*414) | 0.18µm- TSMC | **1** |
| | STM8S (5W*765) | F9GO1- ST Rousset | **1** |

**Package Reliability Trials :**

(*) tests performed after preconditioning

| Reliability Trial | | Test Conditions | Pass Criteria | Unit per Lot | Qual Lot nb |
|---|---|---|---|---|---|
| **PC** | Pre Conditioning: Moisture Sensitivity Jedec Level 3<br>J-STD-020/ JESD22-A113 | Bake (125°C / 24 hrs) Soak (30°C / 60% RH / 192 hrs) for level 3 Convection reflow: 3 passes with Jedec level 3 | 3 passes MSL3 | **231** | **3** |
| **AC(*)** | Autoclave<br>JESD22 A102 | 121°C, 100% RH, 2 Atm | 96h | **77** | **3** |
| **TC(*)** | Thermal Cycling<br>JESD22 A104 | -50°C, +150°C | 1000Cy | **77** | **3** |
| **WBP** | Wire Bond Pull<br>Mil Std 883 Method 2011 | | Minimum pull strength after TC=3 grams after TC | **30 wires** | **3** |
| **WBS** | Wire Bond Shear<br>AEC Q100-001 | | Min bond shear 15g after TC | **30 wires** | **3** |
| **THB(*)** | Temperature Humidity Bias<br>JESD22 A101 | 85°C, 85% RH, bias | 1000h | **77** | **3** |
| **HTSL** | High Temperature Storage Life<br>JESD22 A103 | 150°C- no bias | 1000h | **77** | **3** |
| **ESD** | ESD Charge Device Model<br>ANSI/ESDSTM5.3.1 | 500V | 500V | **3** | **All devices** |

| | | | | | |
|---|---|---|---|---|---|
| **Physical dimension** | Dimension measurement<br><br>JESD 22B100/B108 | | CPK<br>>1.33<br>PPK<br>>1.67 | **10** | **3** |
| **Solderability** | Lead solderability<br><br>JESD 22B102 | | >95%<br>lead<br>coverage | **45 leads** | **3** |

***Attachment : Reliability tests description***

## Package oriented tests/ Trials description

### 1. Preconditioning

According to ST spec 0098044.
Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.
Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

### 2. Autoclave (AC)

The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.
Purpose: to investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

### 3. Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).
Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.
Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

### 4. Temperature Humidity Bias (THB)

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.
Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.
The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- Ta=85°C; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed Tj = 95 °C.

## 5. High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
Purpose: to investigate the failure mechanisms activated by high temperature, typically wirebonds solder joint ageing, data retention faults, metal stress-voiding.

## 6. ESD Charge Device Model (CDM)

This ESD failure model is associated with the device and package itself. The CDM is intended to simulate charging/discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in Figure 1.

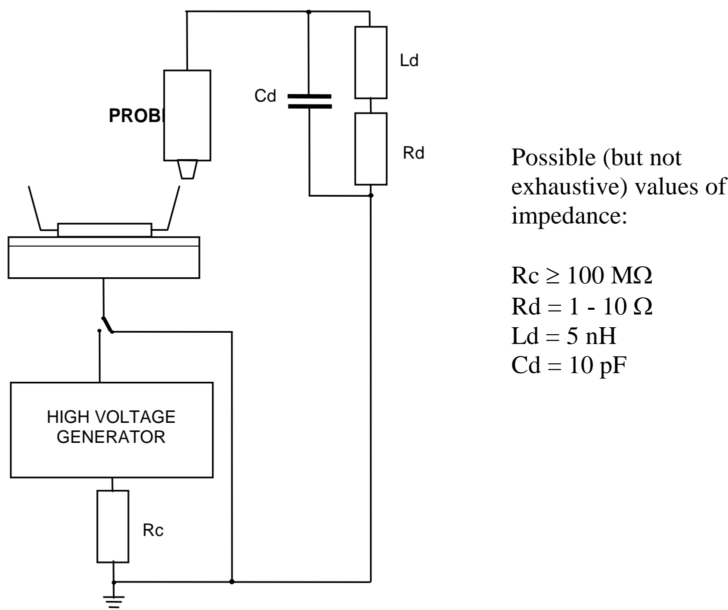



Fig.1 : Field induced CDM equivalent circuit

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