

# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

## Digital Transistors (BRT) R1 = 100 kΩ, R2 = 100 kΩ

### PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current – Continuous	I <sub>C</sub>	100	mAdc
Input Forward Voltage	V <sub>IN(fwd)</sub>	40	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	10	Vdc

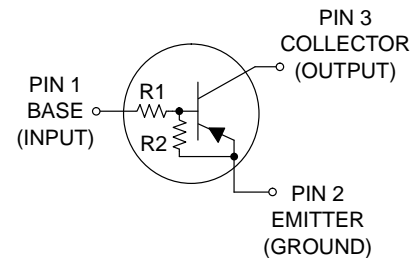
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



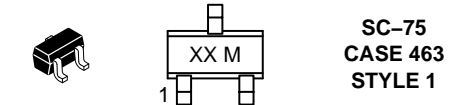
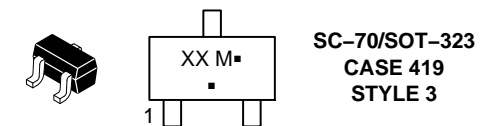
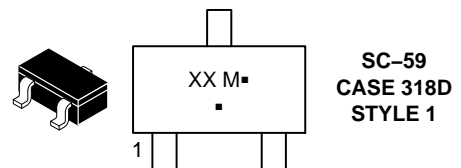
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#### PIN CONNECTIONS



#### MARKING DIAGRAMS



XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

#### ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.

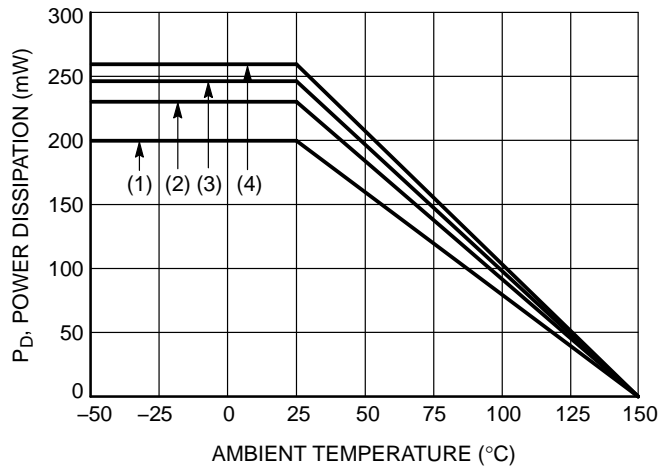
# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

**Table 1. ORDERING INFORMATION**

Device	Part Marking	Package	Shipping†
MUN2136T1G	6N	SC-59 (Pb-Free)	3000 / Tape & Reel
MMUN2136LT1G	ACG	SOT-23 (Pb-Free)	3000 / Tape & Reel
MUN5136T1G	6N	SC-70/SOT-323 (Pb-Free)	3000 / Tape & Reel
DTA115EET1G, NSVDTA115EET1G*	6N	SC-75 (Pb-Free)	3000 / Tape & Reel
DTA115EM3T5G	6N	SOT-723 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



- (1) SC-75 and SC-70/SOT323; Minimum Pad
- (2) SC-59; Minimum Pad
- (3) SOT-23; Minimum Pad
- (4) SOT-723; Minimum Pad

**Figure 1. Derating Curve**

# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

**Table 2. THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
<b>THERMAL CHARACTERISTICS (SC-59) (MUN2136)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	(Note 1) (Note 2) (Note 1) (Note 2)	$P_D$  230 338 1.8 2.7	  mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$  540 370	  $^\circ\text{C/W}$
Thermal Resistance, Junction to Lead	(Note 1) (Note 2)	$R_{\theta JL}$  264 287	  $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS (SOT-23) (MMUN2136L)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	(Note 1) (Note 2) (Note 1) (Note 2)	$P_D$  246 400 2.0 3.2	  mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$  508 311	  $^\circ\text{C/W}$
Thermal Resistance, Junction to Lead	(Note 1) (Note 2)	$R_{\theta JL}$  174 208	  $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS (SC-70/SOT-323) (MUN5136)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	(Note 1) (Note 2) (Note 1) (Note 2)	$P_D$  202 310 1.6 2.5	  mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$  618 403	  $^\circ\text{C/W}$
Thermal Resistance, Junction to Lead	(Note 1) (Note 2)	$R_{\theta JL}$  280 332	  $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS (SC-75) (DTA115EE)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	(Note 1) (Note 2) (Note 1) (Note 2)	$P_D$  200 300 1.6 2.4	  mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$  600 400	  $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS (SOT-723) (DTA115EM3)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	(Note 1) (Note 2) (Note 1) (Note 2)	$P_D$  260 600 2.0 4.8	  mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$  480 205	  $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 Inch Pad.

# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	–	–	100	nAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	–	–	500	nAdc
Emitter–Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	–	0.05	mAdc
Collector–Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 3) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc
<b>ON CHARACTERISTICS</b>					
DC Current Gain (Note 3) ( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )	$h_{FE}$	80	150	–	
Collector–Emitter Saturation Voltage (Note 3) ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )	$V_{CE(sat)}$	–	–	0.25	Vdc
Input Voltage (off) ( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\ \mu\text{A}$ )	$V_{i(off)}$	–	1.2	0.5	Vdc
Input Voltage (on) ( $V_{CE} = 0.3\text{ V}$ , $I_C = 1.0\text{ mA}$ )	$V_{i(on)}$	3.0	1.6	–	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 5.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	–	–	0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	–	–	Vdc
Input Resistor	$R_1$	70	100	130	$\text{k}\Omega$
Resistor Ratio	$R_1/R_2$	0.8	1.0	1.2	

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle  $\leq 2\%$ .

TYPICAL CHARACTERISTICS  
MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3



Figure 2.  $V_{CE(sat)}$  vs.  $I_C$



Figure 3. DC Current Gain



Figure 4. Output Capacitance



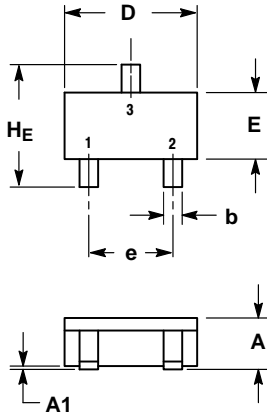
Figure 5. Output Current vs. Input Voltage



Figure 6. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

SC-59  
CASE 318D-04  
ISSUE H

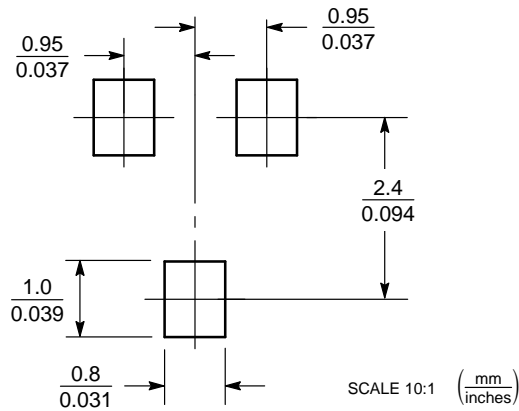


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.15	1.30	0.039	0.045	0.051
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.35	0.43	0.50	0.014	0.017	0.020
c	0.09	0.14	0.18	0.003	0.005	0.007
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	1.70	1.90	2.10	0.067	0.075	0.083
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.80	3.00	0.099	0.110	0.118

- STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

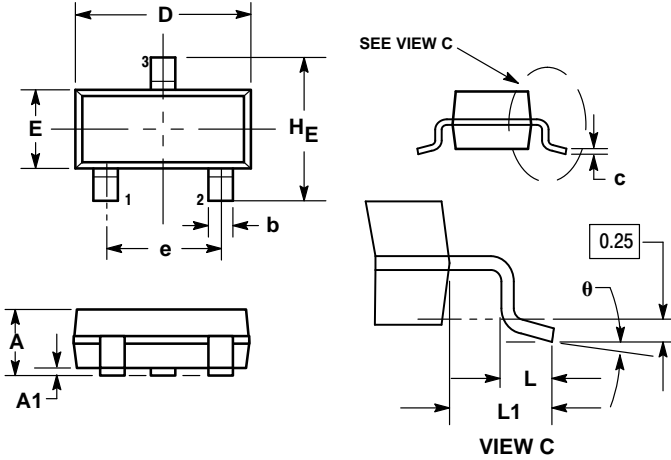
SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AP



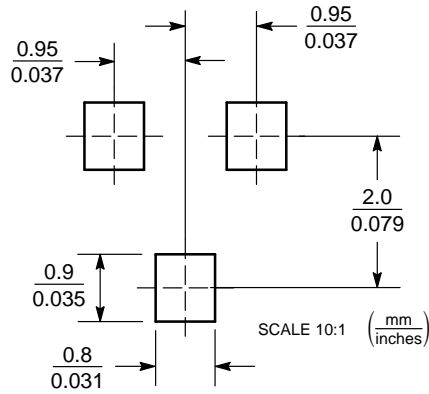
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

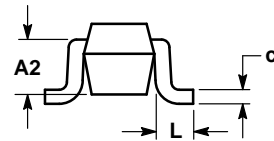
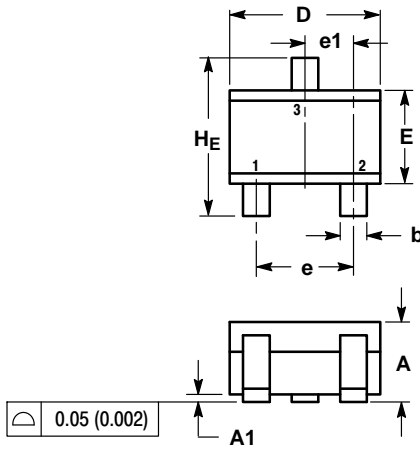
- STYLE 6:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

SC-70 (SOT-323)  
CASE 419-04  
ISSUE N



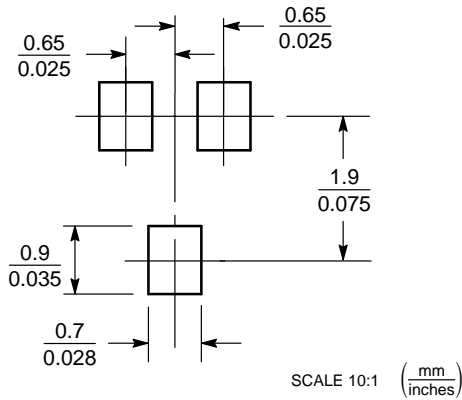
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
HE	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

SOLDERING FOOTPRINT\*

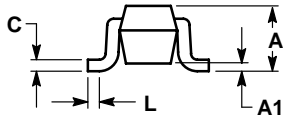
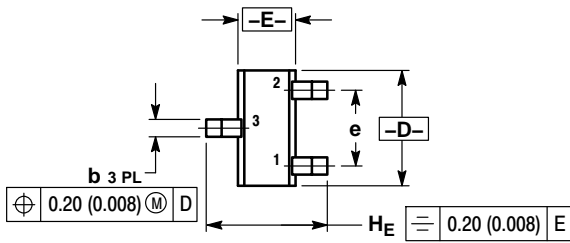


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



PACKAGE DIMENSIONS

SC-75/SOT-416  
CASE 463  
ISSUE F

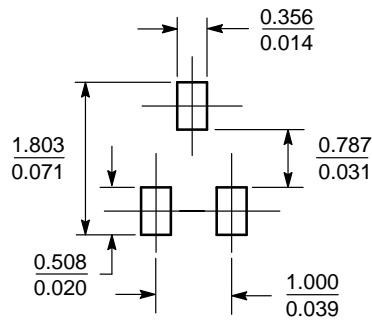


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.059	0.063	0.067
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H <sub>E</sub>	1.50	1.60	1.70	0.061	0.063	0.065

- STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

SOLDERING FOOTPRINT\*



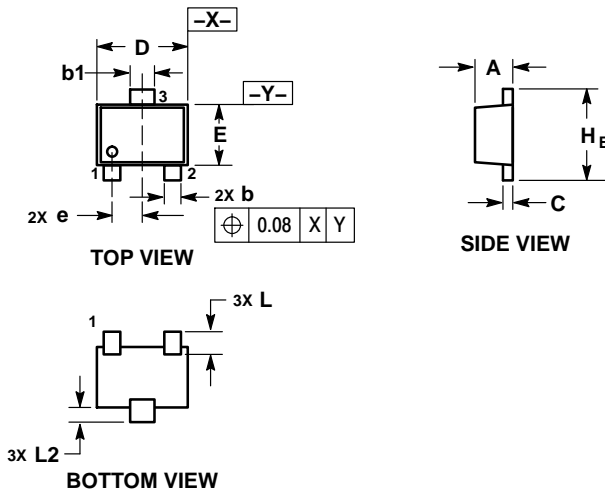
SCALE 10:1 (  $\frac{\text{mm}}{\text{inches}}$  )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

## PACKAGE DIMENSIONS

### SOT-723 CASE 631AA ISSUE D



#### NOTES:

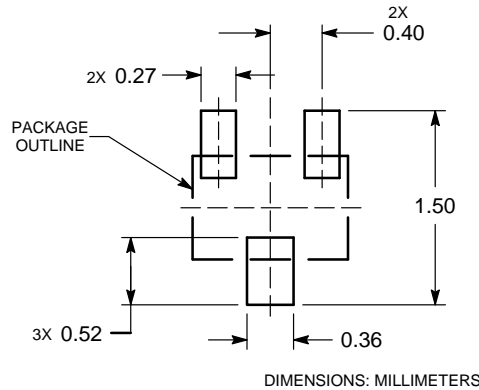
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
C	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H <sub>E</sub>	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25

#### STYLE 1:

1. BASE
2. EMITTER
3. COLLECTOR

### RECOMMENDED SOLDERING FOOTPRINT\*



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