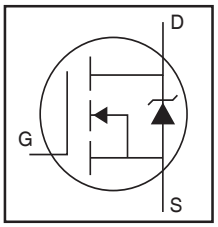
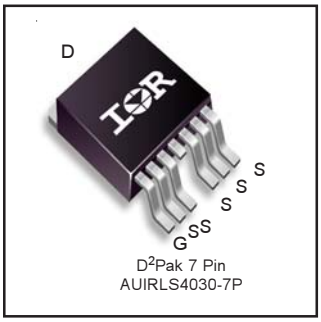
HEXFET® Power MOSFET

## Features

- Optimized for Logic Level Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *




| | | |
|---|---|---|
| $V_{DSS}$ | | 100V |
| $R_{DS(on)}$ | typ. | 3.2mΩ |
| | max. | 3.9mΩ |
| $I_D$ | | 190A |




| G | D | S |
|---|---|---|
| Gate | Drain | Source |

## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| AUIRLS4030-7P | D2Pak 7 Pin | Tube | 50 | AUIRLS4030-7P |
| | | Tape and Reel Left | 800 | AUIRLS4030-7TRL |
| | | Tape and Reel Right | 800 | AUIRLS4030-7TRR |

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ($T_A$) is 25°C, unless otherwise specified.

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 190 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 130 | |
| $I_{DM}$ | Pulsed Drain Current ① | 750 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 370 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 16 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy (Thermally limited) ② | 320 | mJ |
| $I_{AR}$ | Avalanche Current ① | See Fig. 14, 15, 22a, 22b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ④ | | mJ |
| dv/dt | Peak Diode Recovery ③ | 13 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds<br>(1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lbf· in (1.1N· m) | |

### Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑧⑨ | — | 0.40 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑦ | — | 40 | |

HEXFET® is a registered trademark of International Rectifier.
*Qualification standards can be found at http://www.irf.com/

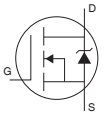
## Static Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.10 | — | V/°C | Reference to 25°C, $I_D$ = 5mA① |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 3.2 | 3.9 | mΩ | $V_{GS}$ = 10V, $I_D$ = 110A ④ |
| | | — | 3.3 | 4.1 | | $V_{GS}$ = 4.5V, $I_D$ = 94A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| gfs | Forward Transconductance | 250 | — | — | S | $V_{DS}$ = 25V, $I_D$ = 110A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 100V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 100V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 16V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -16V |
| $R_{G(int)}$ | Internal Gate Resistance | — | 2.0 | — | Ω | |

## Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge | — | 93 | 140 | nC | $I_D$ = 110A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 27 | — | | $V_{DS}$ = 50V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | 43 | — | | $V_{GS}$ = 4.5V ④ |
| $Q_{sync}$ | Total Gate Charge Sync. ($Q_g$ - $Q_{gd}$) | — | 50 | — | | $I_D$ = 110A, $V_{DS}$ =0V, $V_{GS}$ = 4.5V |
| $t_{d(on)}$ | Turn-On Delay Time | — | 53 | — | ns | $V_{DD}$ = 65V |
| $t_r$ | Rise Time | — | 160 | — | | $I_D$ = 110A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 110 | — | | $R_G$ = 2.7Ω |
| $t_f$ | Fall Time | — | 87 | — | | $V_{GS}$ = 4.5V ④ |
| $C_{iss}$ | Input Capacitance | — | 11490 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 680 | — | | $V_{DS}$ = 50V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 300 | — | | $f$ = 1.0MHz |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related) | — | 760 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 80V ⑥ |
| $C_{oss}$ eff. (TR) | Effective Output Capacitance (Time Related) | — | 1170 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 80V ⑤ |

## Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 190 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 750 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 110A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 53 | — | ns | $T_J$ = 25°C $V_R$ = 85V, |
| | | — | 63 | — | | $T_J$ = 125°C $I_F$ = 110A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 99 | — | nC | $T_J$ = 25°C di/dt = 100A/µs ④ |
| | | — | 155 | — | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | — | 3.3 | — | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.05mH $R_G$ = 25Ω, $I_{AS}$ = 110A, $V_{GS}$ =10V. Part not recommended for use above this value .

③ $I_{SD}$ ≤ 110A, di/dt ≤ 1520A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑥ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑨ $R_{\theta JC}$ value shown is at time zero.

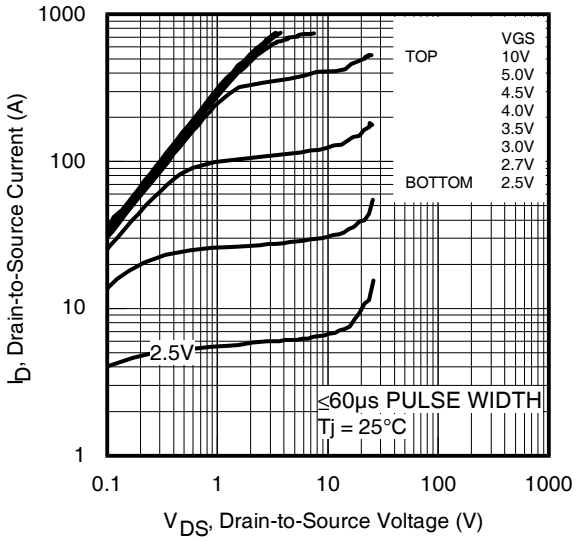



**Fig 1.** Typical Output Characteristics

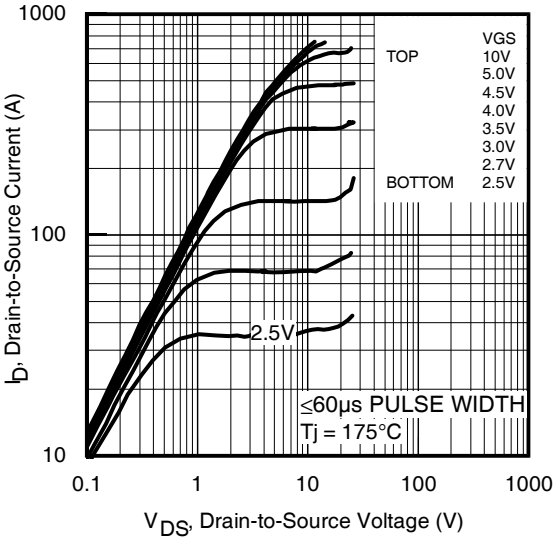



**Fig 2.** Typical Output Characteristics

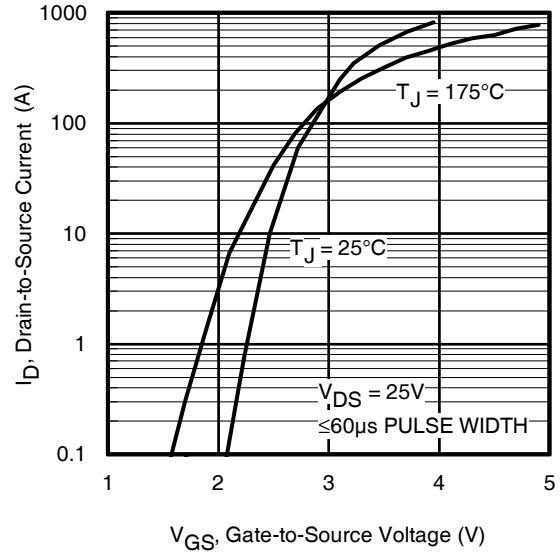



**Fig 3.** Typical Transfer Characteristics

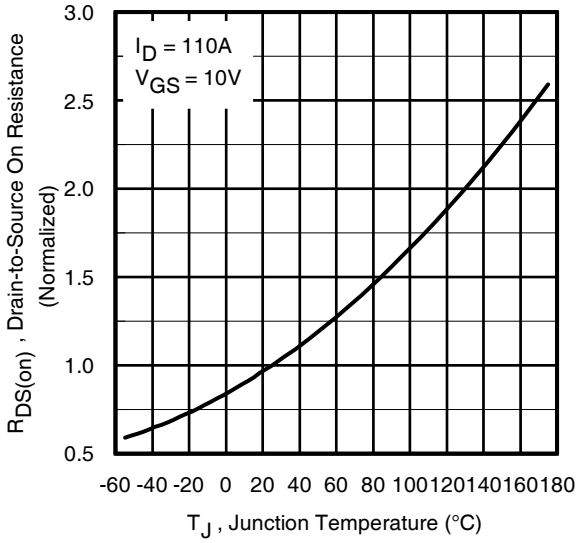



**Fig 4.** Normalized On-Resistance vs. Temperature

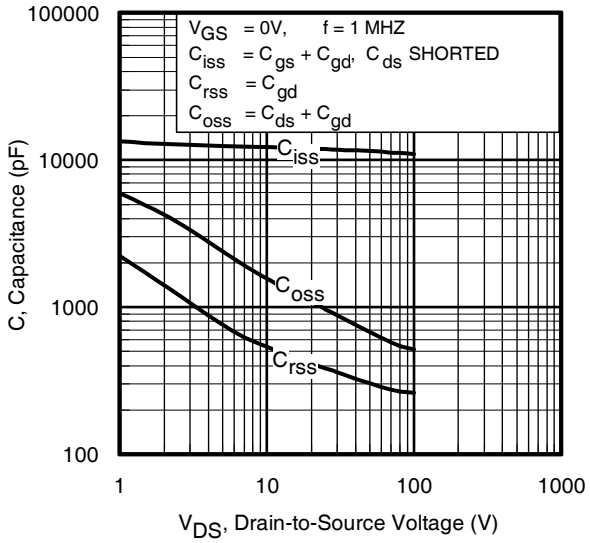



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

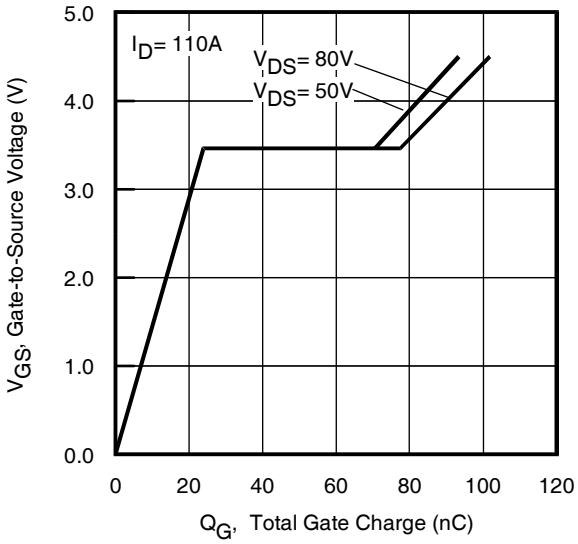



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

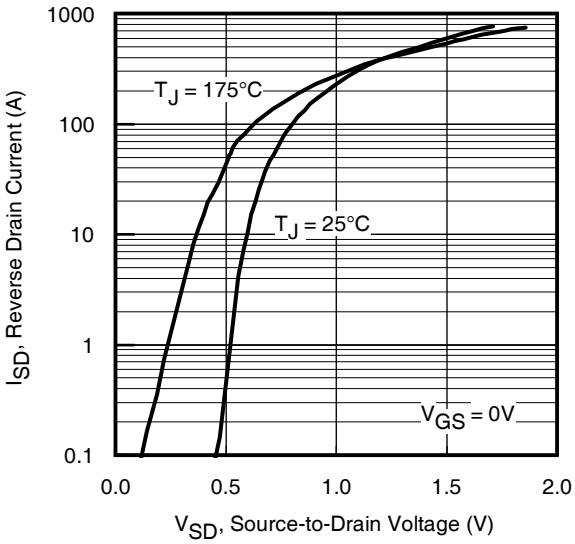



**Fig 7.** Typical Source-Drain Diode Forward Voltage

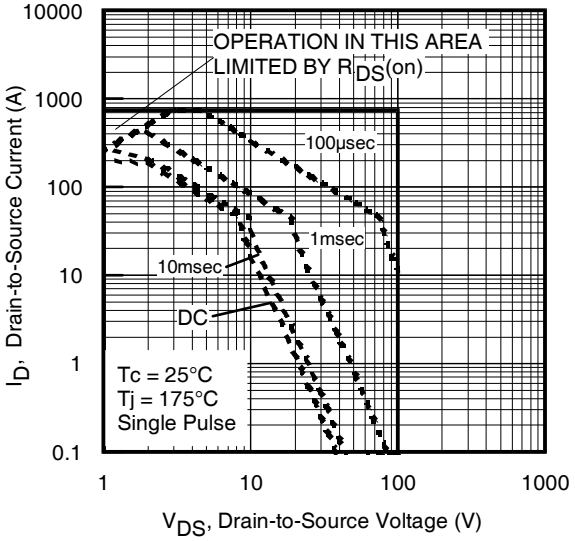



**Fig 8.** Maximum Safe Operating Area

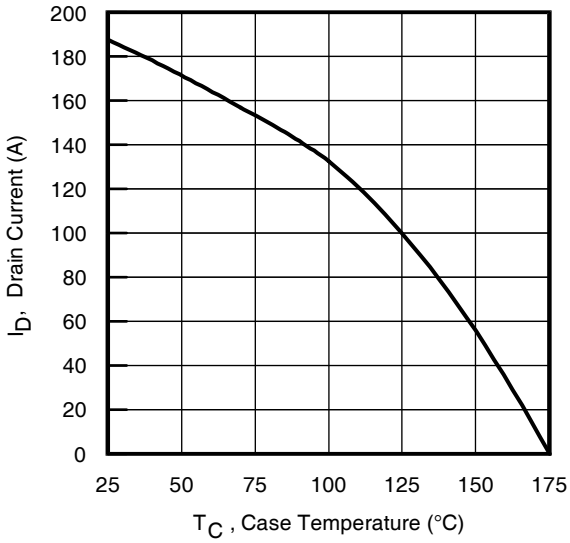



**Fig 9.** Maximum Drain Current vs. Case Temperature

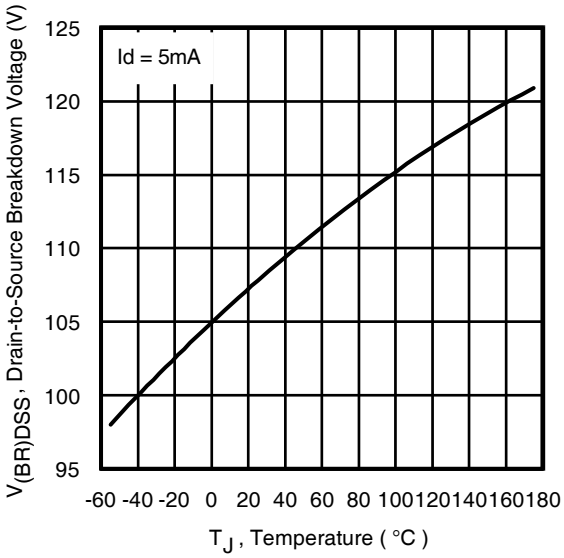



**Fig 10.** Drain-to-Source Breakdown Voltage

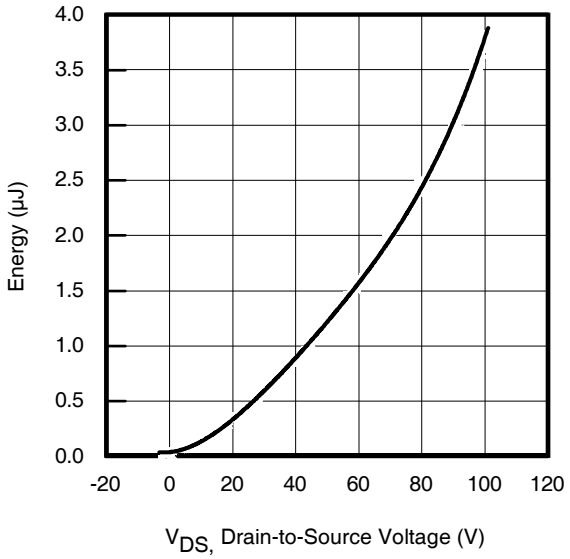



**Fig 11.** Typical $C_{OSS}$ Stored Energy

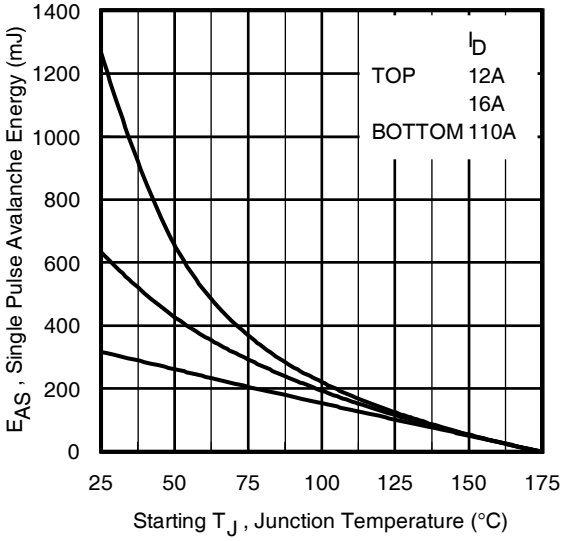



**Fig 12.** Maximum Avalanche Energy vs. DrainCurrent

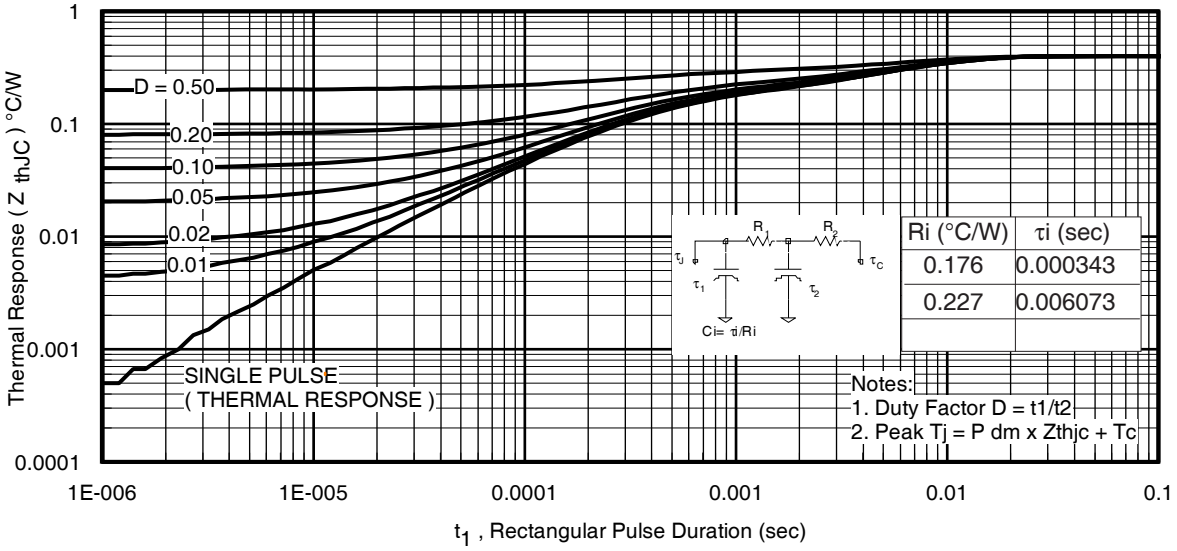



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

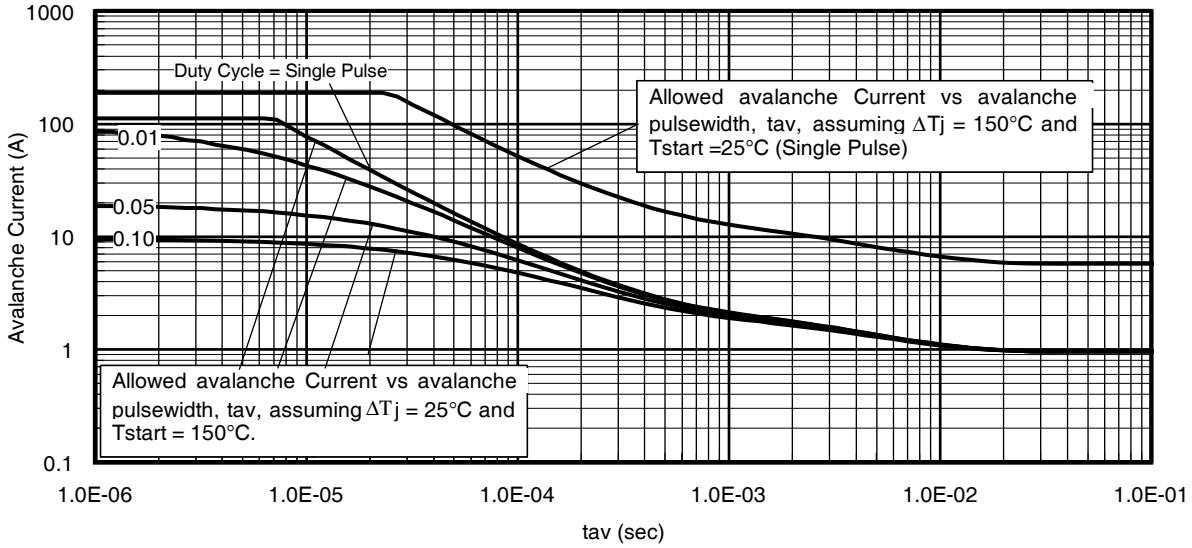



**Fig 14.** Typical Avalanche Current vs.Pulsewidth

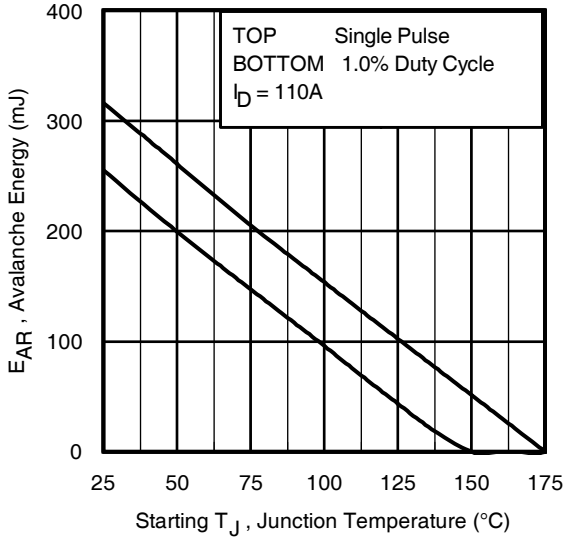



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as$T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 14, 15).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

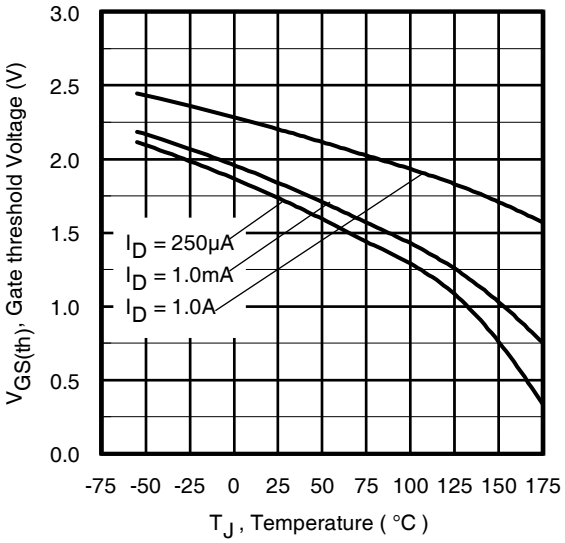



**Fig 16.** Threshold Voltage vs. Temperature

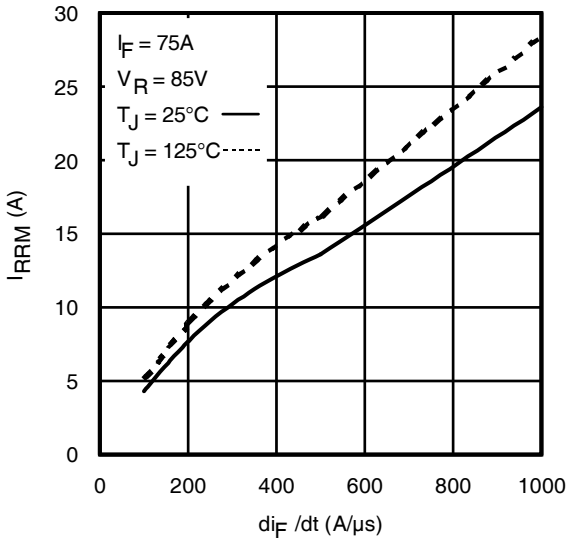



**Fig. 17** - Typical Recovery Current vs. $di_f/dt$

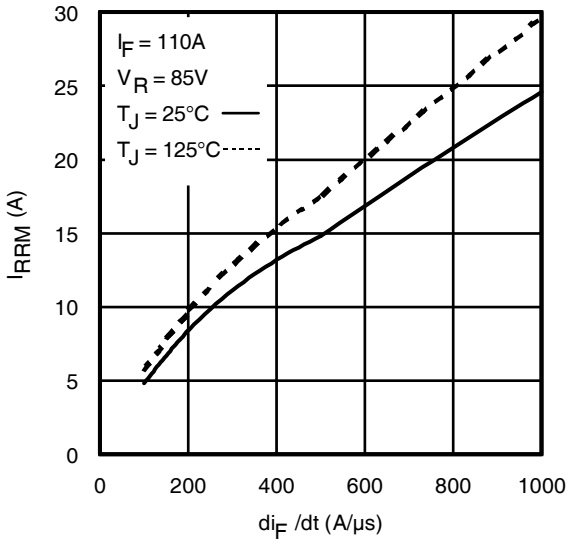



**Fig. 18** - Typical Recovery Current vs. $di_f/dt$

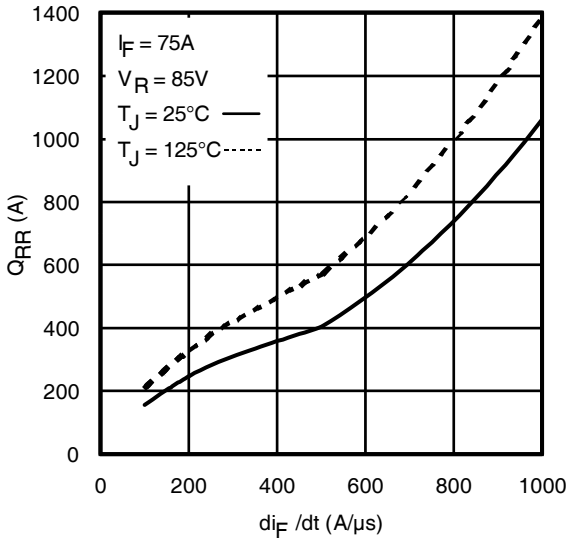



**Fig. 19** - Typical Stored Charge vs. $di_f/dt$

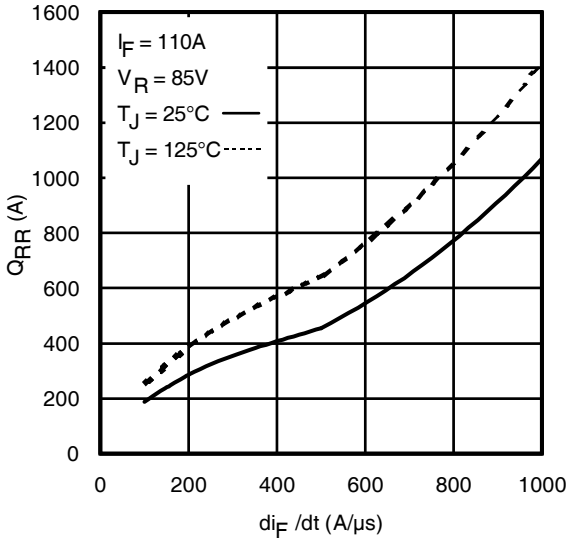



**Fig. 20** - Typical Stored Charge vs. $di_f/dt$

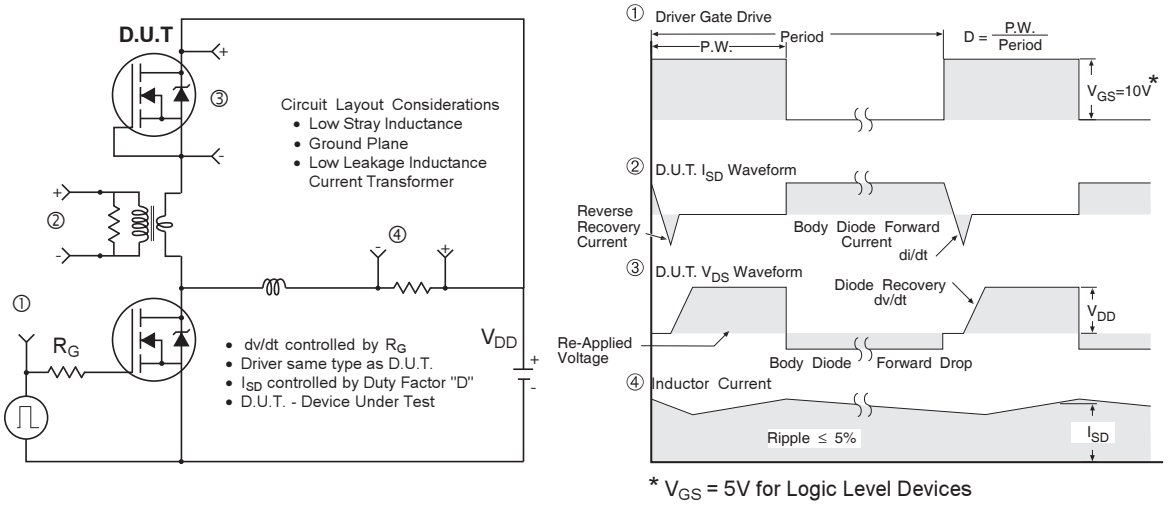



**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

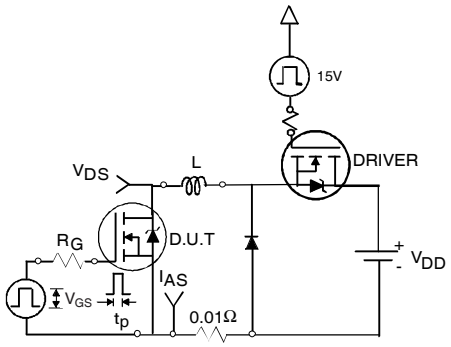



**Fig 22a.** Unclamped Inductive Test Circuit

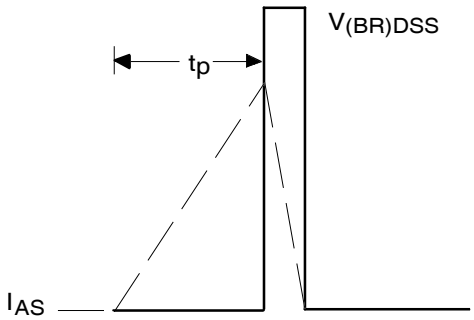



**Fig 22b.** Unclamped Inductive Waveforms

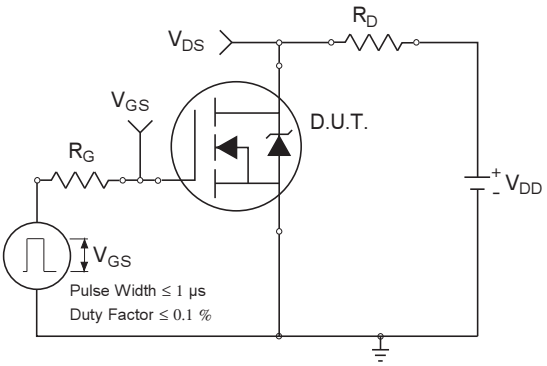



**Fig 23a.** Switching Time Test Circuit

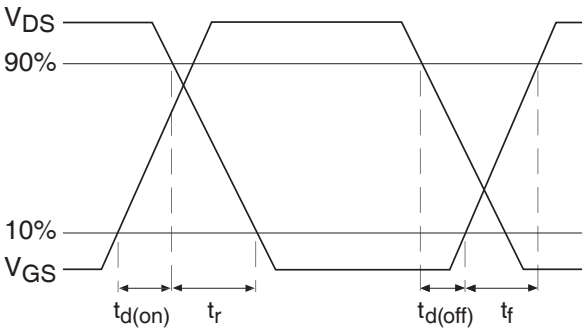



**Fig 23b.** Switching Time Waveforms

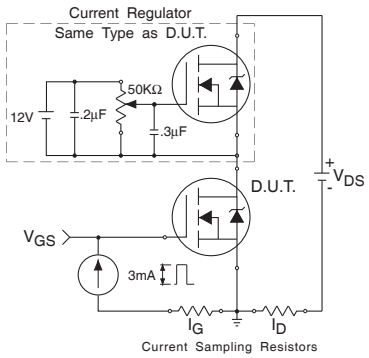



**Fig 24a.** Gate Charge Test Circuit

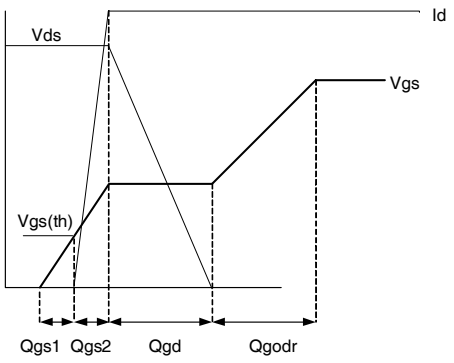
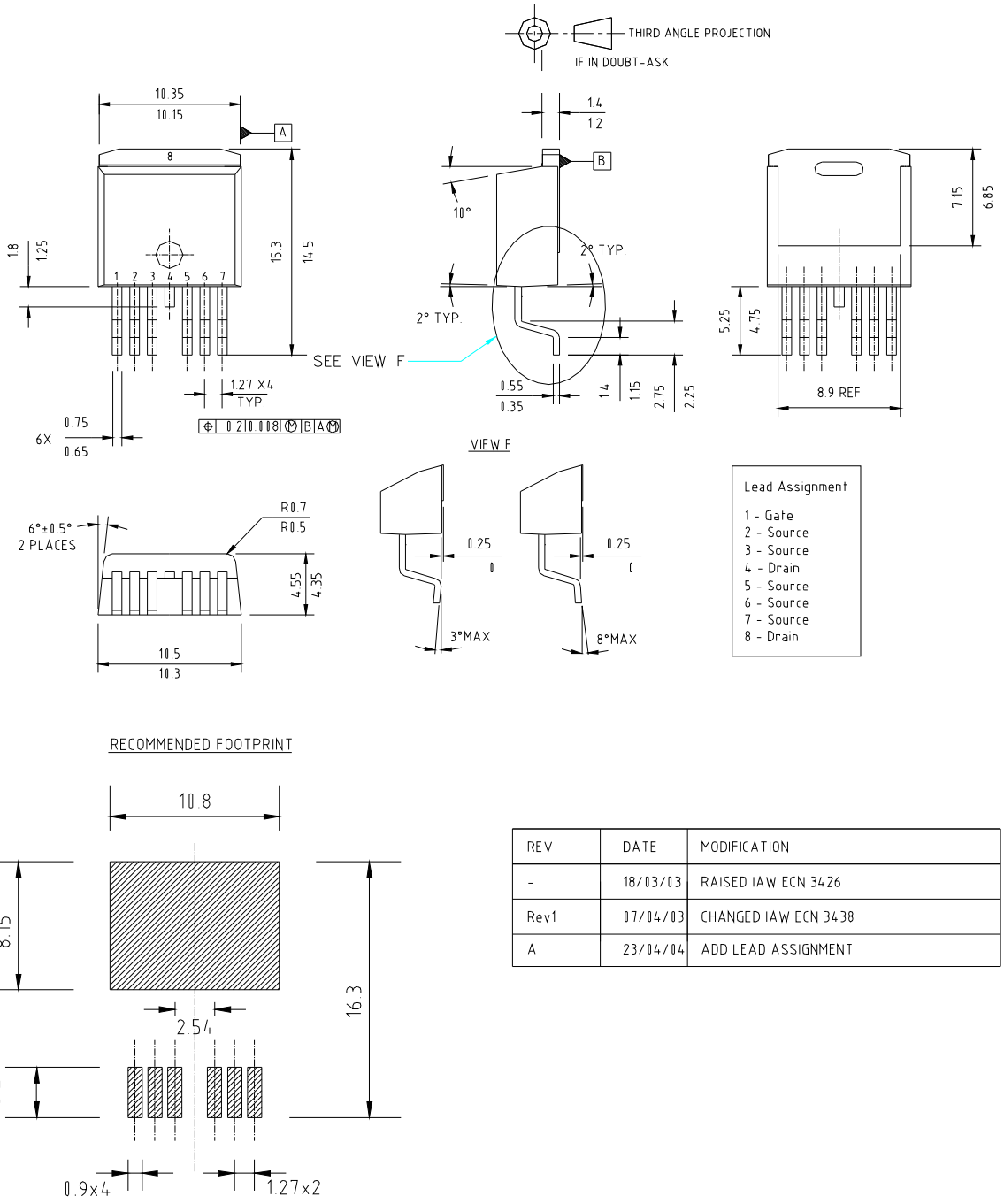



**Fig 24b.** Gate Charge Waveform

# D²Pak - 7 Pin Package Outline

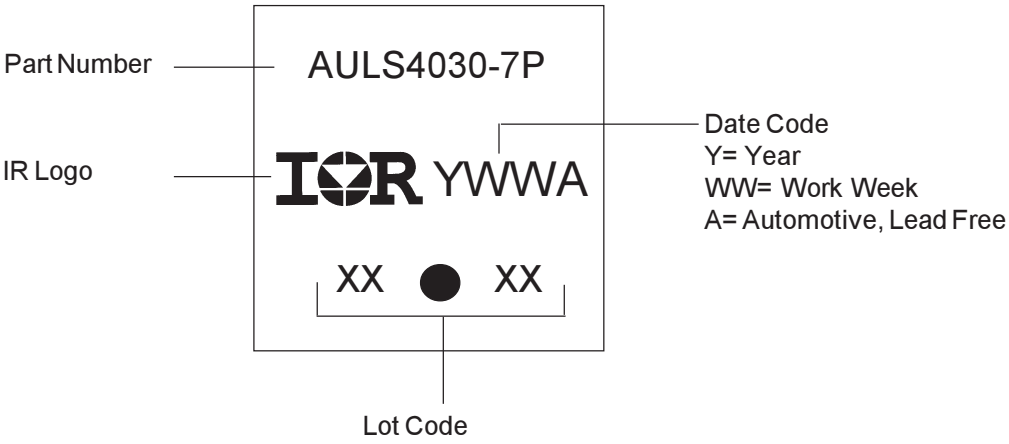
Dimensions are shown in millimeters (inches)




| REV | DATE | MODIFICATION |
|---|---|---|
| - | 18/03/03 | RAISED IAW ECN 3426 |
| Rev1 | 07/04/03 | CHANGED IAW ECN 3438 |
| A | 23/04/04 | ADD LEAD ASSIGNMENT |

**Note: For the most current drawing please refer to IR website at http://www.irf.com/package/**

## D²Pak - 7 Pin Part Marking Information

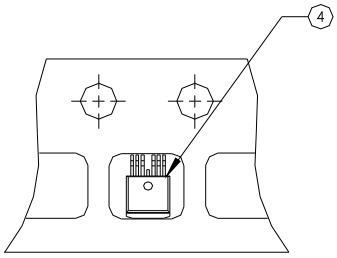


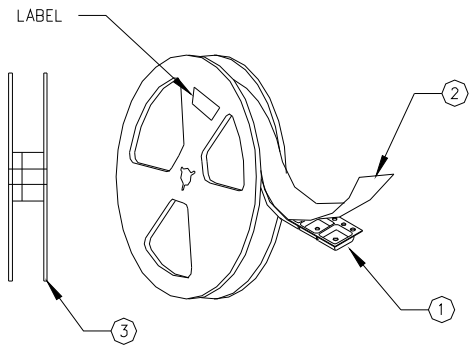

## D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 800 DEVICES.
   - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   - 2.4 QUANTITY:
   - 2.5 VENDOR CODE: IR
   - 2.6 LOT CODE:
   - 2.7 DATE CODE:




**Note: For the most current drawing please refer to IR website at http://www.irf.com/package/**

## Qualification Information†

| | | | |
|---|---|---|---|
| **Qualification Level** | | Automotive (per AEC-Q101) †† | |
| | | Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| **Moisture Sensitivity Level** | | 7L-D2 PAK | MSL1 |
| **ESD** | Machine Model | Class M4(+/- 800V )††† (per AEC-Q101-002) | |
| | Human Body Model | Class H3A(+/- 6000V )††† (per AEC-Q101-001) | |
| | Charged Device Model | Class C5(+/- 2000V )††† (per AEC-Q101-005) | |
| **RoHS Compliant** | | Yes | |

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Exceptions (if any) to AEC-Q101 requirements are noted in the qualification report.

††† Highest passing voltage

## IMPORTANT NOTICE

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For technical support, please contact IR’s Technical Assistance Center

http://www.irf.com/technical-info/

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## Revision History

| Date | Comments |
|---|---|
| 3/3/2014 | • Added "Logic Level Gate Drive" bullet in the features section on page 1<br>• Updated data sheet with new IR corporate template |

  