



# PQM11

NPN/NPN resistor-equipped transistors;  
R1 = 10 kΩ, R2 = 10 kΩ

26 October 2015

Product data sheet

## 1. General description

NPN/NPN Resistor-Equipped Transistors (RET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PQMB11.

NPN/PNP complement: PQMD3.

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Low package height of 0.37 mm
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	50	V
I <sub>O</sub>	output current			-	-	100	mA
<b>Per transistor</b>							
R1	bias resistor 1	T <sub>amb</sub> = 25 °C	[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

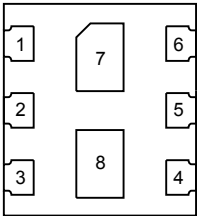
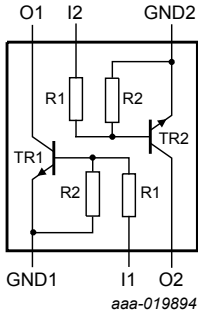
[1] See section "Test information" for resistor calculation and test conditions.



NPN/NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view <b>DFN1010B-6 (SOT1216)</b></p>	 <p>aaa-019894</p>
2	I1	input ( base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input ( base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

## 6. Ordering information

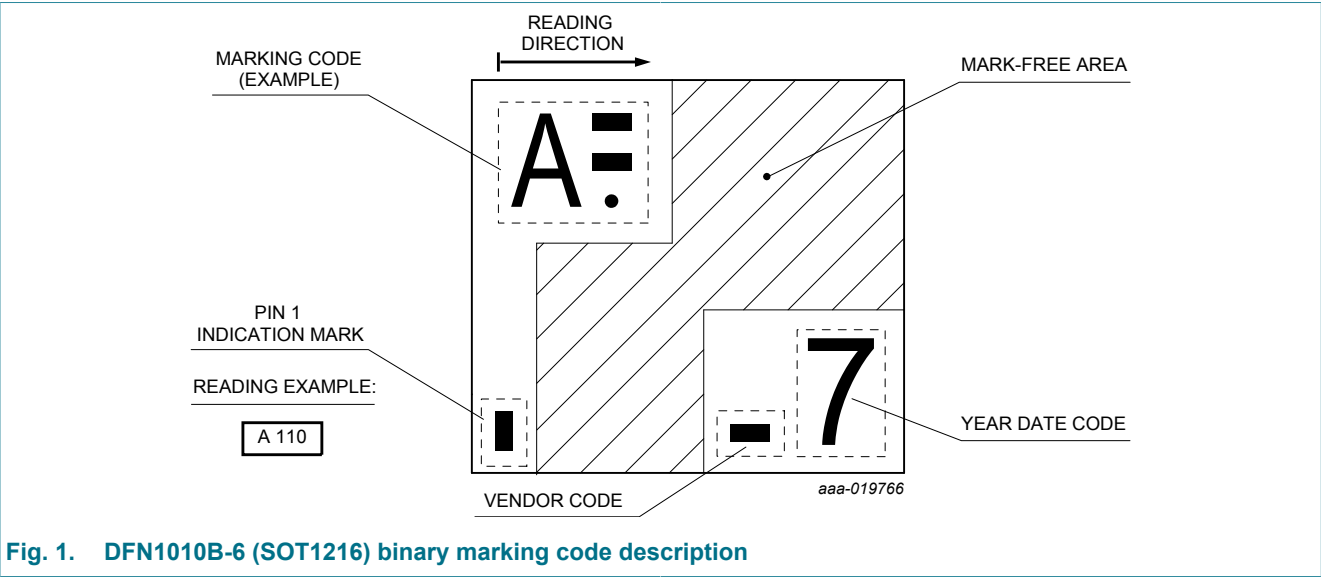
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PQMH11	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PQMH11	A 001



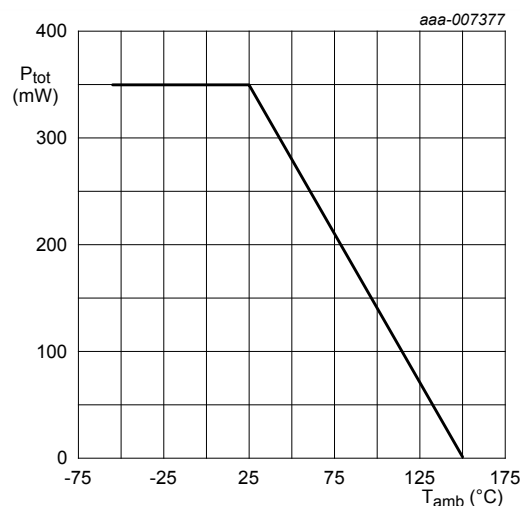
## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	10	V
V <sub>I</sub>	input voltage	positive		-	40	V
		negative		-	-10	V
I <sub>O</sub>	output current			-	100	mA
I <sub>CM</sub>	peak collector current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	230	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	350	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

**Fig. 2. Per device: Power derating curve**

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	543	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	357	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

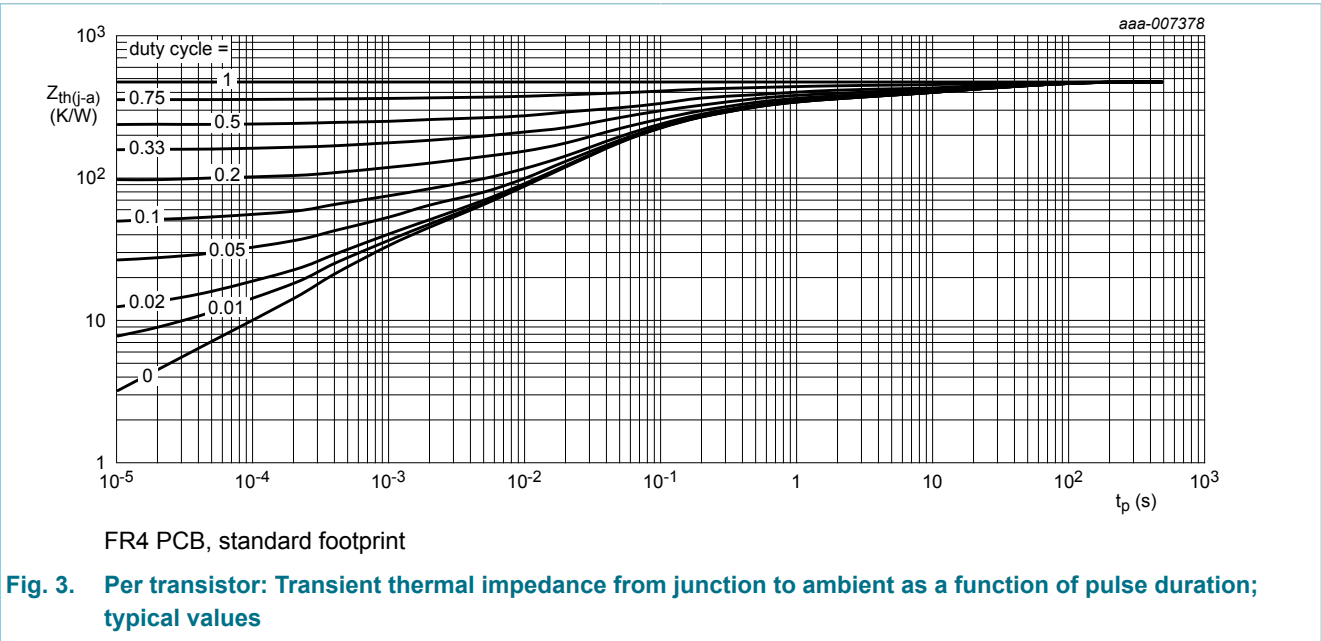


Fig. 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$I_{CBO}$	collector-base cut-off current (emitter open)	$V_{CB} = 50\text{ V}$ ; $I_E = 0\text{ A}$ ; $T_{amb} = 25\text{ °C}$		-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current (base open)	$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 25\text{ °C}$		-	-	1	μA
		$V_{CE} = 30\text{ V}$ ; $I_B = 0\text{ A}$ ; $T_{amb} = 150\text{ °C}$		-	-	5	μA
$I_{EBO}$	emitter-base cut-off current (collector open)	$V_{EB} = 5\text{ V}$ ; $I_C = 0\text{ A}$ ; $T_{amb} = 25\text{ °C}$		-	-	400	μA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}$ ; $I_C = 5\text{ mA}$ ; $T_{amb} = 25\text{ °C}$		30	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}$ ; $I_B = 0.5\text{ mA}$ ; $T_{amb} = 25\text{ °C}$		-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$ ; $I_C = 100\text{ μA}$ ; $T_{amb} = 25\text{ °C}$		-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$ ; $I_C = 10\text{ mA}$ ; $T_{amb} = 25\text{ °C}$		2.5	1.8	-	V
R1	bias resistor 1	$T_{amb} = 25\text{ °C}$	[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
$C_C$	collector capacitance	$V_{CB} = 10\text{ V}$ ; $I_E = 0\text{ A}$ ; $f = 1\text{ MHz}$ ; $T_{amb} = 25\text{ °C}$		-	-	2.5	pF
$f_T$	transition frequency	$V_{CE} = 5\text{ V}$ ; $I_C = 10\text{ mA}$ ; $f = 100\text{ MHz}$ ; $T_{amb} = 25\text{ °C}$	[2]	-	230	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor

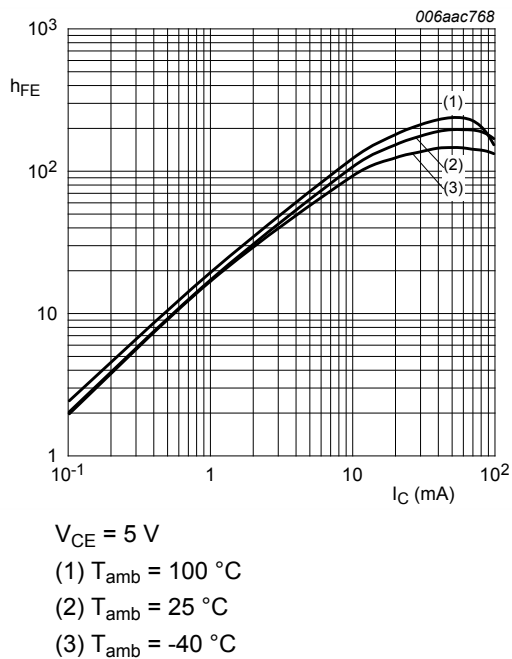


Fig. 4. DC current gain as a function of collector current; typical values

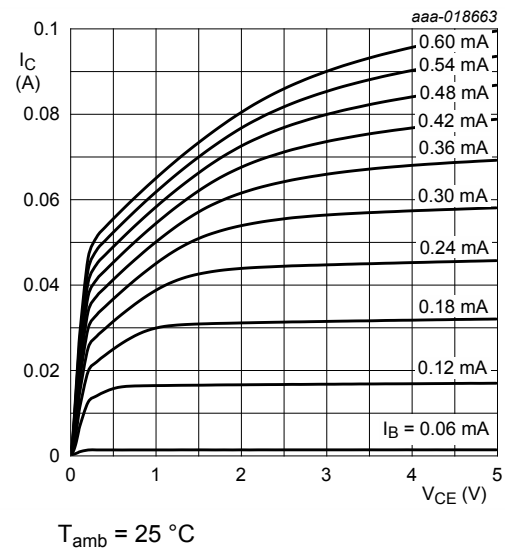


Fig. 5. Collector current as a function of collector-emitter voltage; typical values

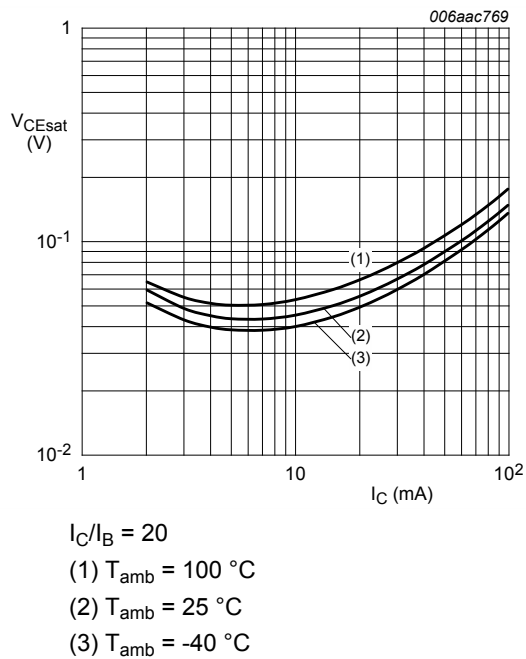


Fig. 6. Collector-emitter saturation voltage as a function of collector current; typical values

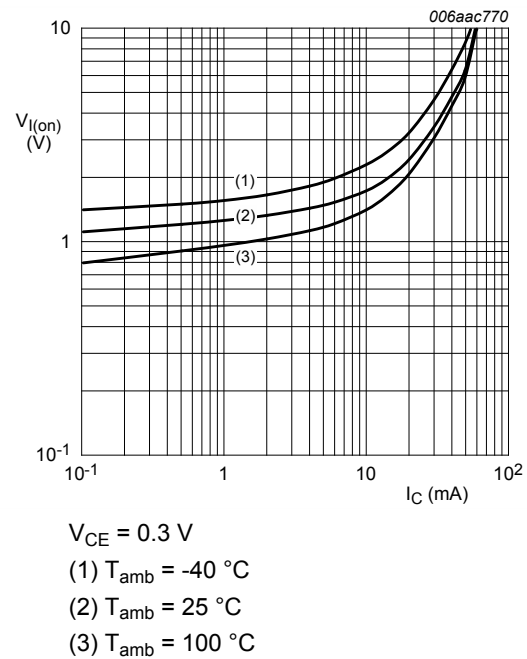


Fig. 7. On-state input voltage as a function of collector current; typical values

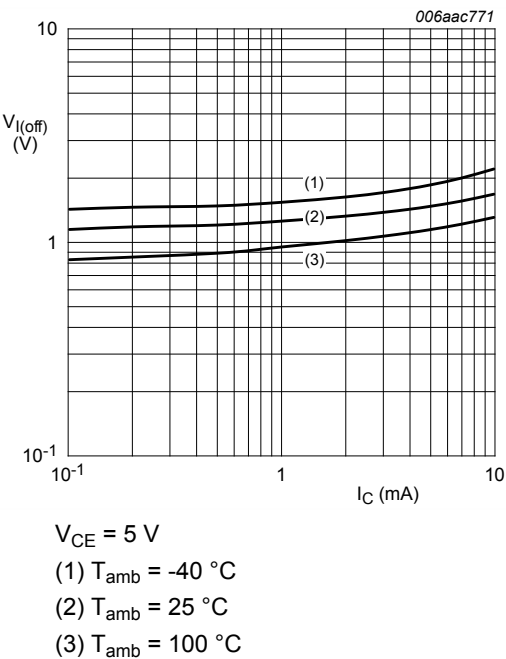


Fig. 8. Off-state input voltage as a function of collector current; typical values

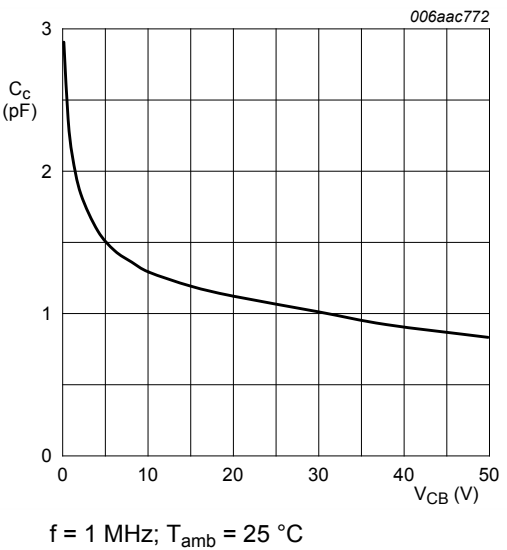


Fig. 9. Collector capacitance as a function of collector-base voltage; typical values

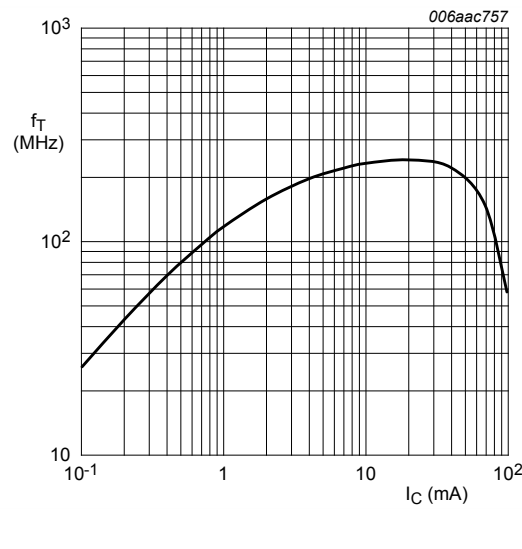


Fig. 10. Transition frequency as a function of collector current; typical values of built-in transistor

## 11. Test information

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.



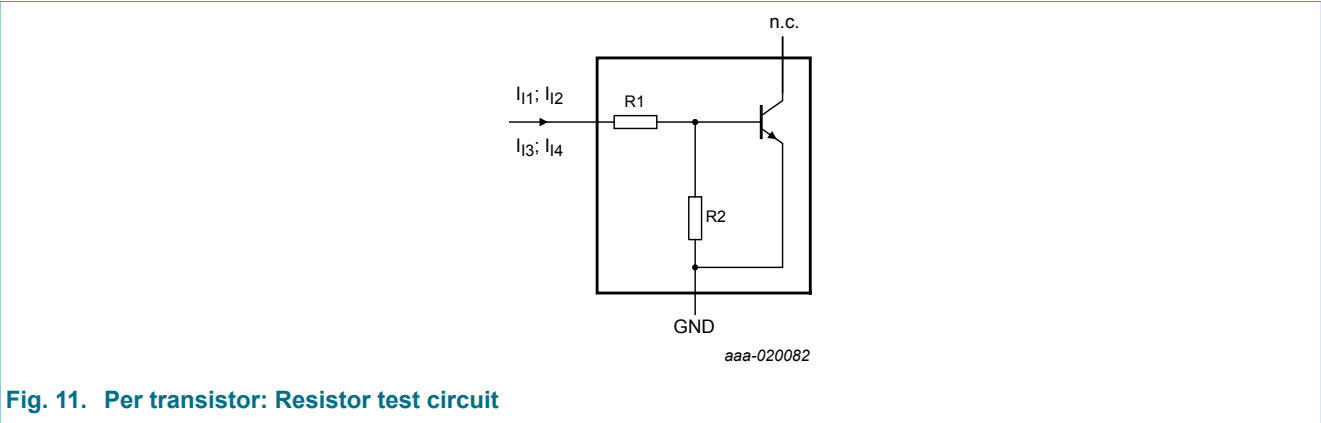
11.2 Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

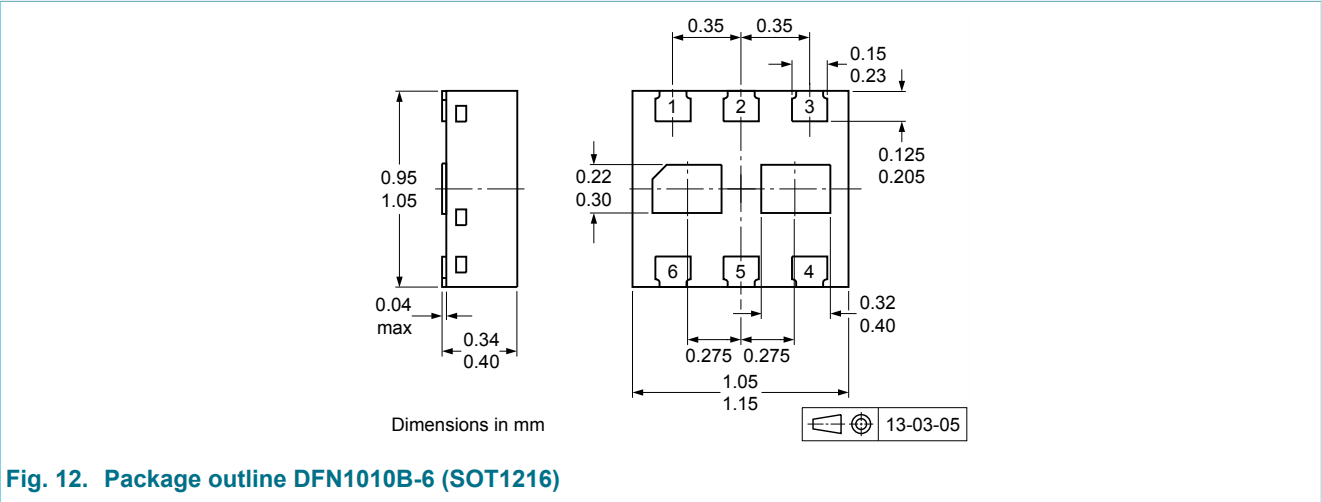


11.3 Resistor test conditions

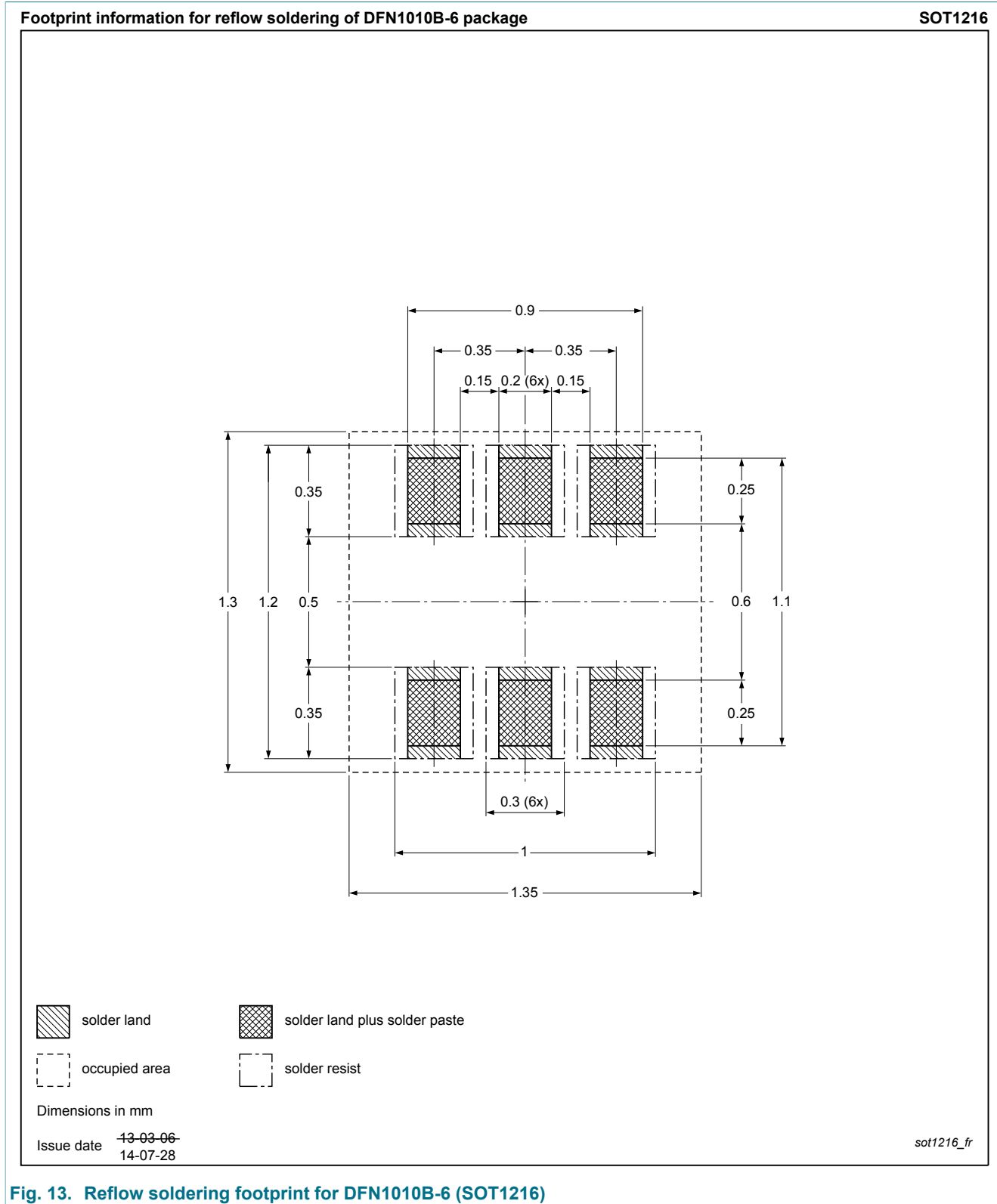
Table 8. Resistor test conditions

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I <sub>I1</sub>	I <sub>I2</sub>	I <sub>I3</sub>	I <sub>I4</sub>
10	10	350 μA	450 μA	-350 μA	-450 μA

12. Package outline



## 13. Soldering



**Fig. 13. Reflow soldering footprint for DFN1010B-6 (SOT1216)**

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PQMH11 v.1	20151026	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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NPN/NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$ 

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