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NTE74176
Integrated Circuit
TTL – 35Mhz Presettable Decade Counter/Latch

Description:

The NTE74176 is a high–speed monolithic counter in a 14–Lead plastic DIP type package consisting of four DC coupled master–slave flip–flops which are internally interconnected to provide a divide–by–two and a divide–by–five counter. This device is fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

The NTE74176 may also be used as a 4–bit latch bu using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are active.

This high–speed counter will accept count frequencies of 0 to 35Mhz at the clock–1 input and 0 to 17.5Mhz at the clock–2 input. During the count operation, transfer of information to the outputs occurs on the negative–going edge of the clock pulse. The counter features a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

All inputs are diode–clamped to minimize transmission–line effects and simplify system design. The circuit is compatible with most TTL logic families and typical power dissipation is 150mW.

Features:

- Reduced Power Version of the NTE74196 50Mhz Counter
- Performs BCD, Bi–Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 35Mhz
- Input Clamping Diodes Simplify System Design

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.
Note 2. This is the voltage between two emitters of a multiple–emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	−	−	−800	μA
Low−Level Input Voltage	V_{OL}	−	−	0.8	V
Count Frequency Clock−1 Input	f_{max}	0	−	35	MHz
Clock−2 Input		0	−	17.5	MHz
Pulse Width Clock−1 Input	t_w	14	−	_	ns
Clock−2 Input		28	−	−	ns
$\overline{\text{Clear}}$		20	−	−	ns
Load		25	−	−	ns
Input Hold Time High−Level Data	t_h	$t_{w(load)}$	−	−	ns
Low−Level Data		$t_{w(load)}$	−	−	ns
Input Setup Time High−Level Data	t_{su}	15	−	−	ns
Low−Level Data		20	−	−	ns
Count Enable Time (Note 3)	t_{enable}	25	−	−	ns
Operating Temperature Range	T_A	0	−	+70	°C

Note 3. Minimum count enable time is the interval immediately preceding the negative−going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

Electrical Characteristics: (Note 4, Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	−	−	V
Low−Level Input Voltage	V_{IL}		−	−	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	−	−	−1.5	V
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	−	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA, Note 6	−	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	−	−	1	mA
High−Level Input Current Data, Count/Load	I_{IH}	V_{CC} = MAX, V_I = 2.4V	−	−	40	μA
$\overline{\text{Clear}}$, Clock 1			−	−	80	μA
Clock 2			−	−	120	μA

Note 4. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 5. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 6. Q_A outputs are tested at I_{OL}n = 16mA plus the limit value of I_{IL} for the clock−2 input. This permits driving the clock−2 while fanning out to 10 Series 74 loads.

Electrical Characteristics (Cont'd): (Note 4, Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Level Input Current Data, Count/Load	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	–1.6	mA
$\overline{\text{Clear}}$			–	–	–3.2	mA
Clock 1			–	–	–4.8	mA
Clock 2			–	–	–4.8	mA
Short–Circuit Output Current	I_{CS}	V_{CC} = MAX, Note 7	–18	–	–57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 8	–	30	48	mA

Note 4. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 5. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 7. Not more than one output should be shorted at a time.

Note 8. I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Count Frequency (From Clock 1 Input to Q_A Output)	f_{max}	R_L = 400Ω, C_L = 15pF	35	50	–	MHz
Propagation Delay Time (From Clock 1 Input to Q_A Output)	t_{PLH}		–	8	13	ns
	t_{PHL}		–	11	17	ns
Propagation Delay Time (From Clock 2 Input to Q_B Output)	t_{PLH}		–	11	17	ns
	t_{PHL}		–	17	26	ns
Propagation Delay Time (From Clock 2 Input to Q_C Output)	t_{PLH}		–	27	41	ns
	t_{PHL}		–	34	51	ns
Propagation Delay Time (From Clock 2 Input to Q_D Output)	t_{PLH}		–	13	20	ns
	t_{PHL}		–	17	26	ns
Propagation Delay Time (From A, B, C, D Input to Q_A, Q_B, Q_C, Q_D, Output)	t_{PLH}		–	19	29	ns
	t_{PHL}		–	31	46	ns
Propagation Delay Time (From Load Input to Any Output)	t_{PLH}		–	29	43	ns
	t_{PHL}		–	32	48	ns
Propagation Delay Time (From $\overline{\text{Clear}}$ Input to Any Output)	t_{PHL}		–	32	48	ns

Typical Count Configurations:

The output of flip–flop A is not internally connected to the succeeding flip–flops; therefore, the count may be operated in three independent modes:

1. When used as a binary–coded–decimal decade counter, the clock–2 input must be externally connected to the Q_A output. The clock–1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table.
2. If a symmetrical divide–by–ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock–1 input. The input count is then applied at the clock–2 input and a divide–by–ten square wave is obtained at output Q_A in accordance with the bi–quinary function table.
3. For operation as a divide–by–two counter and a divide–by–five counter, no external interconnections are required. Flip–flop A is used as a binary element for the divide–by–two function. The clock–2 input is used to obtain binary divide–by–five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip–flops are loaded and cleared simultaneously.

Function Tables:

Decade (BCD)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = High Level, L = Low Level
NOTE: Output Q_A connected to clock−2 input.

Bi−Quinary (5−2)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = High Level, L = Low Level
NOTE: Output Q_D connected to clock−1 input.

Pin Connection Diagram