Low Voltage, 1.2 Ω, Dual SPDT Analog Switch

DESCRIPTION

The DG2725 is a CMOS Dual SPDT (Dual Single Pole Double Throw) analog switch. It features low on-resistance of 0.7 Ω at 3 V power supply, fast switching speed, and low power consumption.

The DG2725 conducts signals equally at both directions and protects COM1 and COM2 pins at Power Off condition. The COM1 and COM2 leakage is guaranteed to be less than 1 µA when V+ is at 0 V. The DG2725 operates in a wide voltage range of 1.65 V to 5 V, and can be controlled by low voltage logic signals.

The DG2725 also features supply current even with control signal is at low voltage below the V+ voltage. The well matched dual SPDT is designed for break before make switching operation.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2725 are offered in a miniQFN package. The miniQFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- Low Voltage Operation (1.65 V to 5 V)
- Low On-Resistance - 1.2 Ω at V+ = 3 V
- Power Off Protection on COM1 and COM2 pins
- Latch up current great than 300 mA per JESD78
- **Halogen-free according to IEC 61249-2-21 definition**
- **Compliant to RoHS Directive 2002/95/EC**

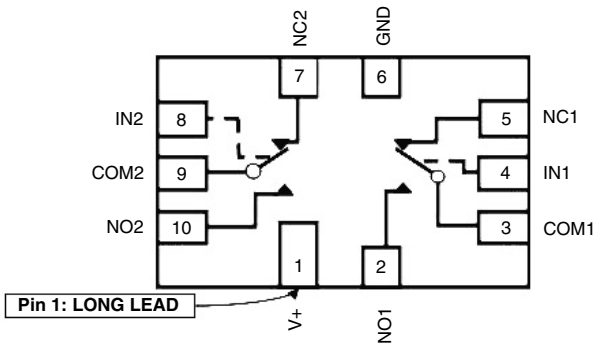
Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- PMPs and PDAs
- Modems and peripherals
- Computers and ebooks
- Tablet devices
- Displays and gaming
- STB

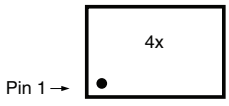
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2725
miniQFN-10L



Device Marking: 4x for DG2725
x = Date/Lot Traceability Code

(Top View)



Note: Pin 1 has long lead

TRUTH TABLE		
Logic	**NC1, 2**	**NO1, 2**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85°C	miniQFN10	DG2725DN-T1-GE4

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Reference to GND	V+		- 0.3 to 5.5	V
	IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Current (Any terminal except NO, NC or COM)			30	mA
Continuous Current (NO, NC, or COM)			± 350	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)			± 500	
Storage Temperature (D Suffix)			- 65 to 150	°C
Power Dissipation (Packages)[b]	miniQFN10[c]		208	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4.0 mW/C above 70 °C.

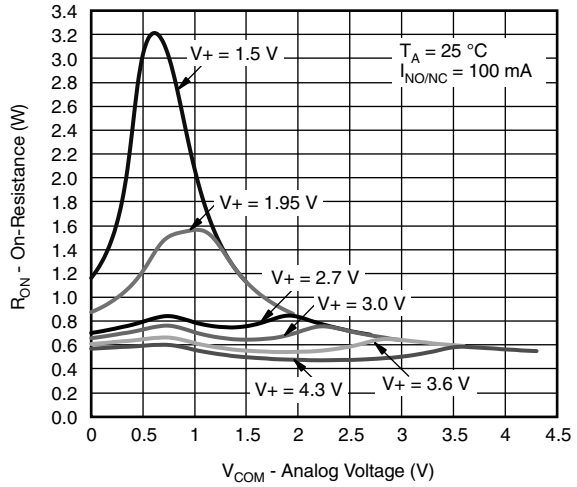
SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 1.65 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	$R_{DS(on)}$	Full	0		V+	V
On-Resistance	$R_{DS(on)}$	V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0.7 V			0.7	1.2	Ω
		V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 2.3 V			0.65		
		V+ = 4.3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0.9 V			0.55	1	
		V+ = 4.3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 2.5 V			0.42		
R_{ON} Match[d]	ΔR_{ON}	V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0.7 V			0.02	0.25	
		V+ = 4.3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0.9 V					
R_{ON} resistance flatness[d]	R_{ON} flatness	V+ = 3 V and 4.3 V, $I_{NO/NC}$ = 100 mA			0.13	0.4	
Switch Off Leakage Current	$I_{NO/NC(off)}$	V+ = 4.3 V, $V_{NO/NC}$ = 0.3 V/4.0 V, V_{COM} = 4.0 V/0.3 V	Room	- 10		10	nA
			Full	- 50		50	
	$I_{COM(off)}$		Room	- 10		10	
			Full	- 50		50	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 4.3 V, $V_{NO/NC}$ = V_{COM} = 4.0 V/0.3 V	Room	- 10		10	
			Full	- 50		50	
Digital Control							
Input High Voltage	V_{INH}	V+ = 1.65 V to 4.3 V	Full	1.7			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{IN}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Break-Before-Make Time[e]	t_{BBM}	V+ = 3.6 V, V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	2			ns
Turn-On Time[e]	t_{ON}		Room			95	
			Full			100	
Turn-Off Time[e]	t_{OFF}		Room			50	
			Full			55	
Off-Isolation[d]	O_{IRR}	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		- 85		dB
Crosstalk[d]	X_{TALK}				- 95		
3dB bandwith[d]		R_L = 50 Ω, C_L = 5 pF	Room		62		MHz

SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 1.65 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Dynamic Characteristics							
NO, NC Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 V, or V+, f = 1 MHz	Room		24		pF
	$C_{NC(off)}$				30		
Channel On Capacitance[d]	$C_{NO(on)}$				100		
	$C_{NC(on)}$				100		
Power Supply							
Power Supply Range	V+			1.65		4.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full	- 1	0.01	1.0	µA
Supply Current per Logic Input	I+T	V+ = 4.3 V, V_{INx} = 2.6 V	Room		7		
		V+ = 4.3 V, V_{INx} = 1.8 V	Room		15		
Power OFF COM pin Leakage	I_{OFF}	V = 0 V, V_{IN} = 4.3 V, NCx, NOx floating	Full	- 1		+ 1	

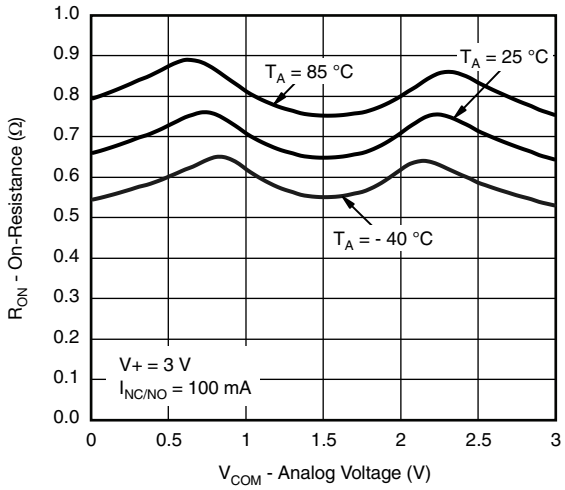
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

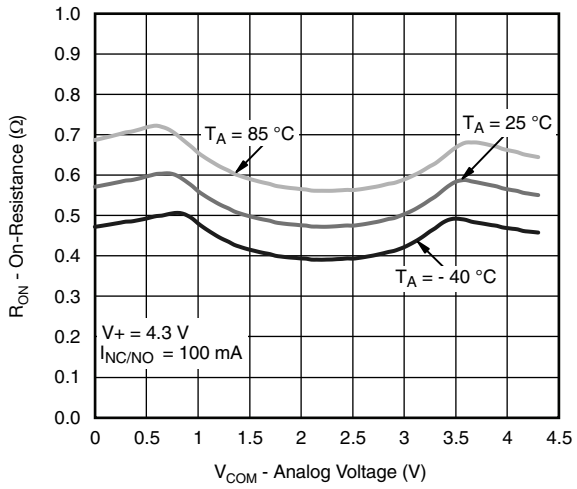


R_{ON} vs. V_{COM} and Single Supply Voltage

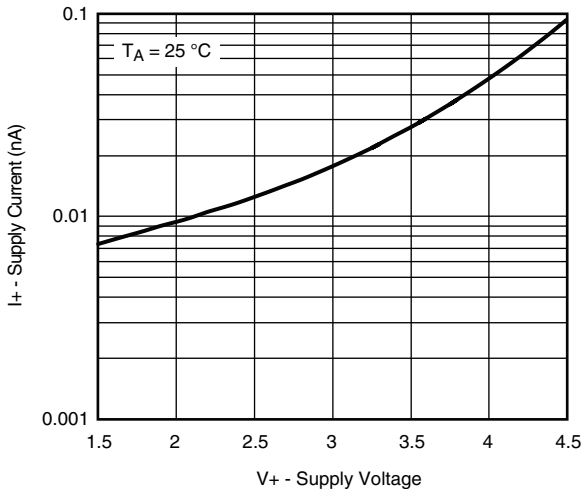


R_{ON} vs. Analog Voltage and Temperature

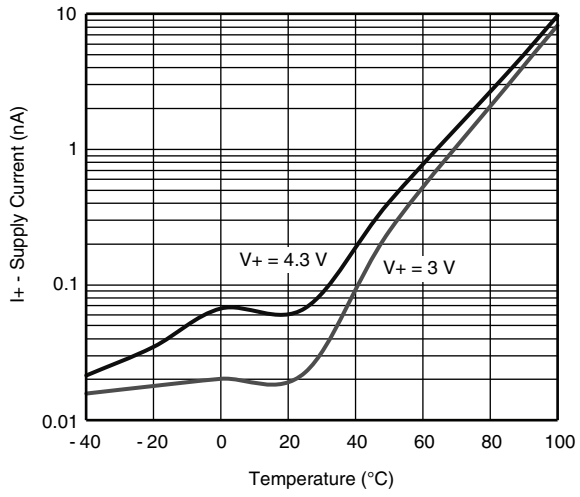
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



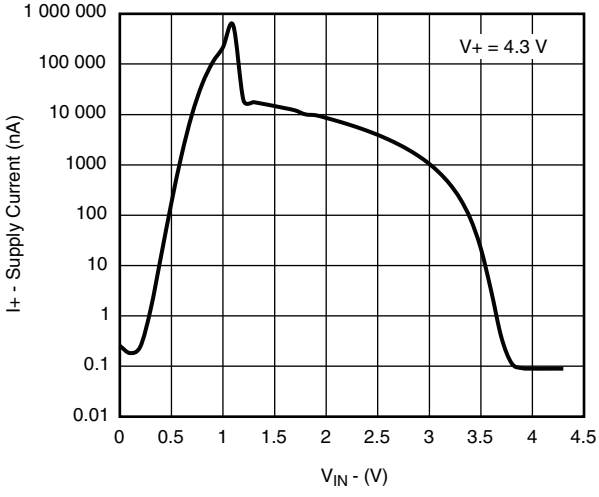
R_{ON} vs. Analog Voltage and Temperature



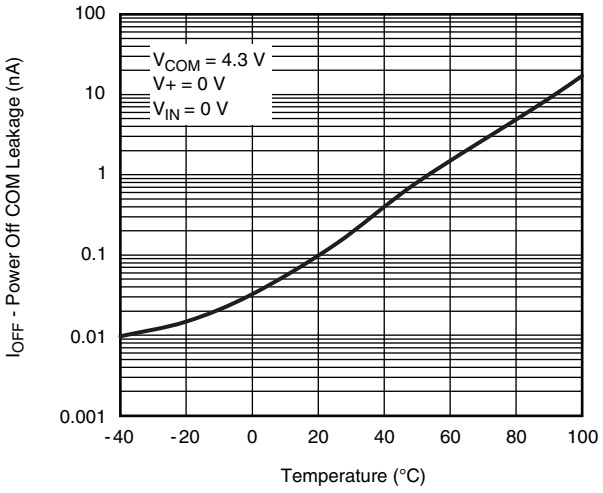
I+ vs. V+



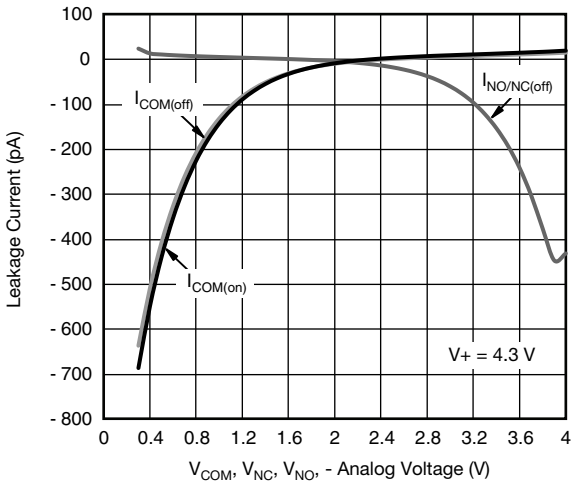
I+ Supply Current vs. Temperature



I+ vs. V_{IN}

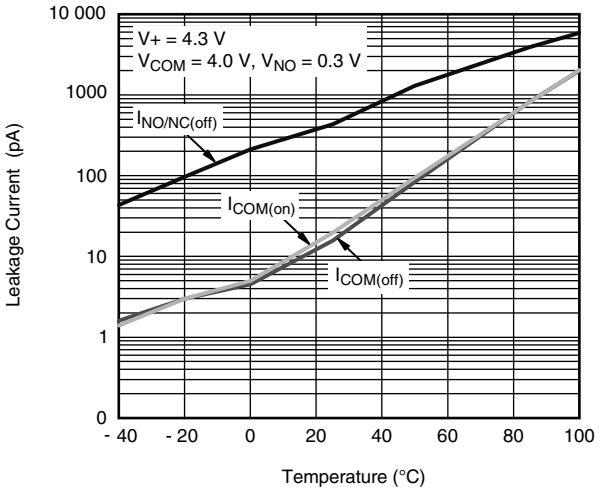


Power Off Leakage I_{OFF} (I_{COM}) vs. Temperature

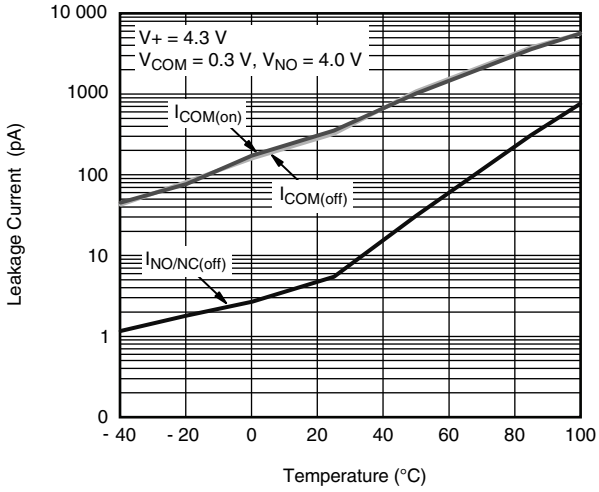


Leakage vs. Analog Voltage, V+ = 4.3 V

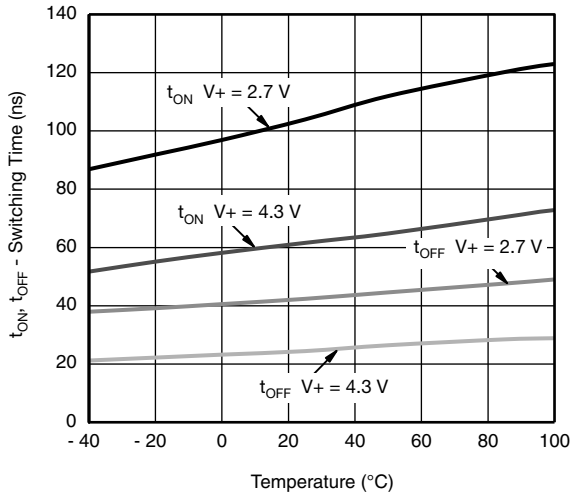
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



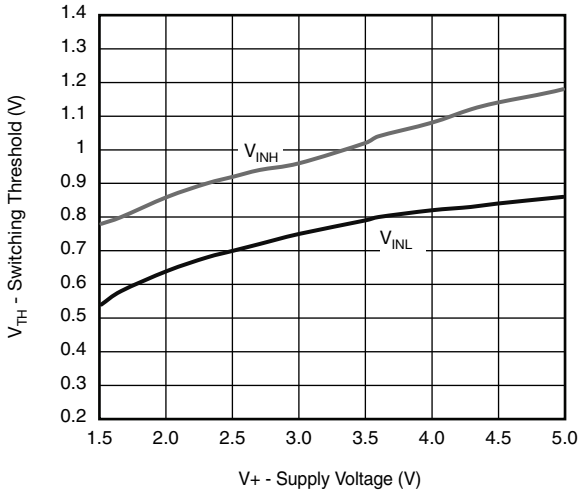
Leakage Current vs. Temperature



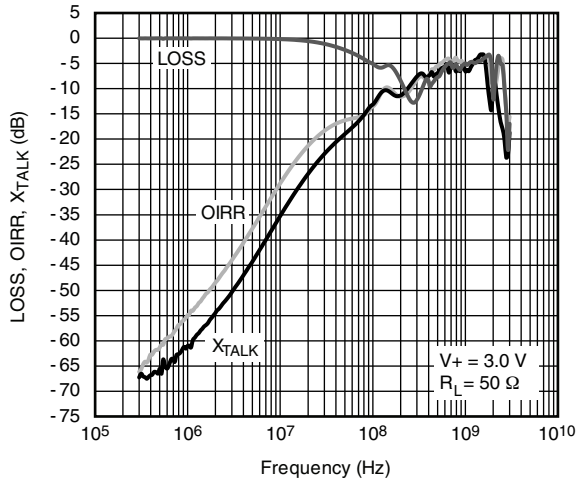
Leakage Current vs. Temperature



t_{ON}, t_{OFF} Switching Time vs. Temperature

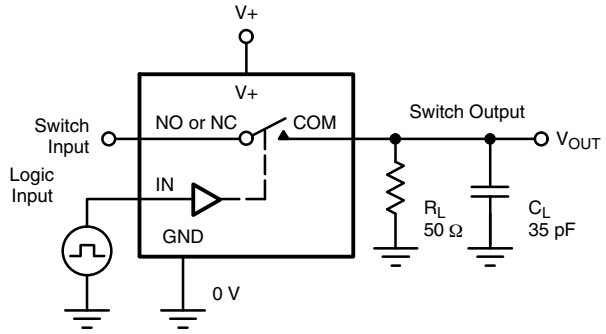


Switching Threshold vs. Supply Voltage



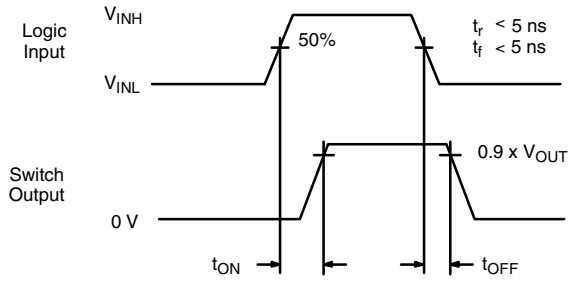
PABK-A Insertion Loss, Off Isolation and Crosstalk

TEST CIRCUITS



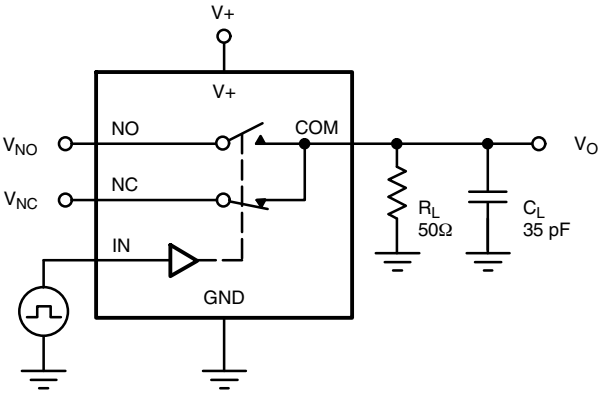
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

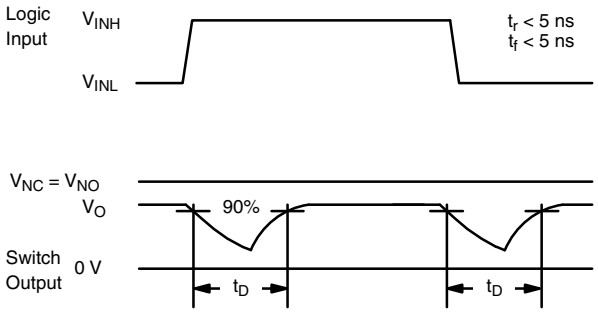
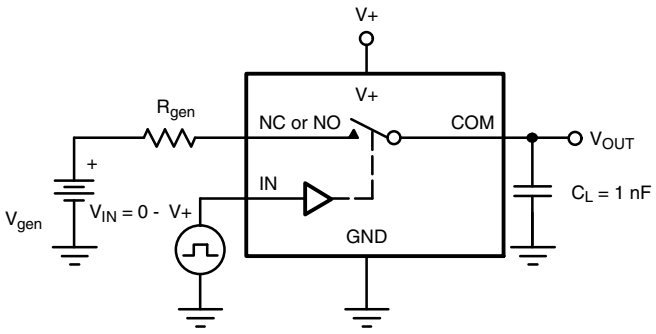
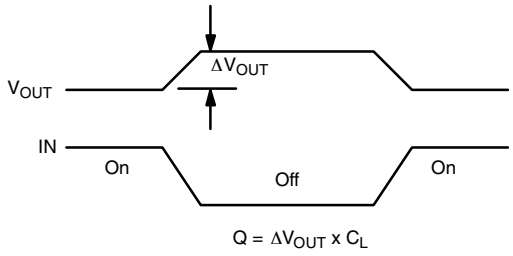


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

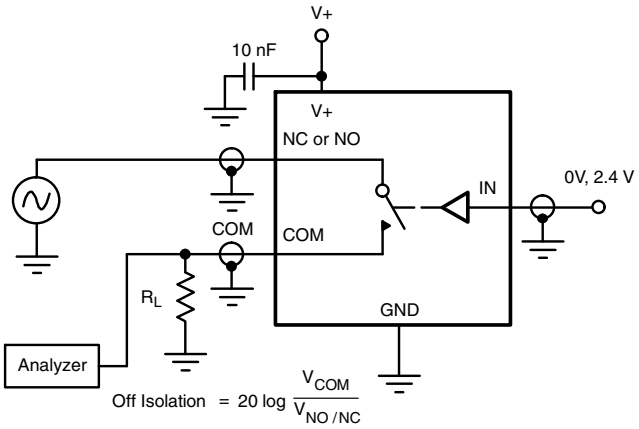


Figure 4. Off-Isolation

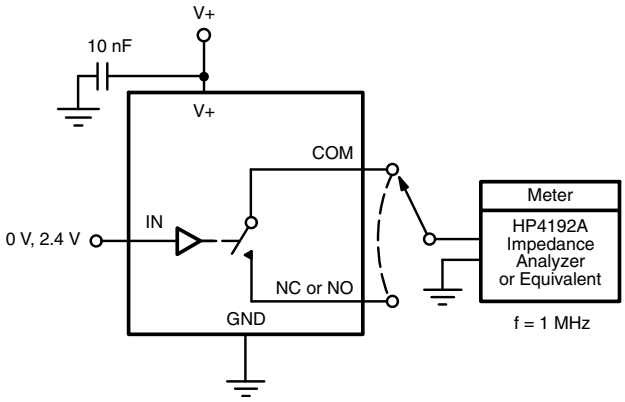
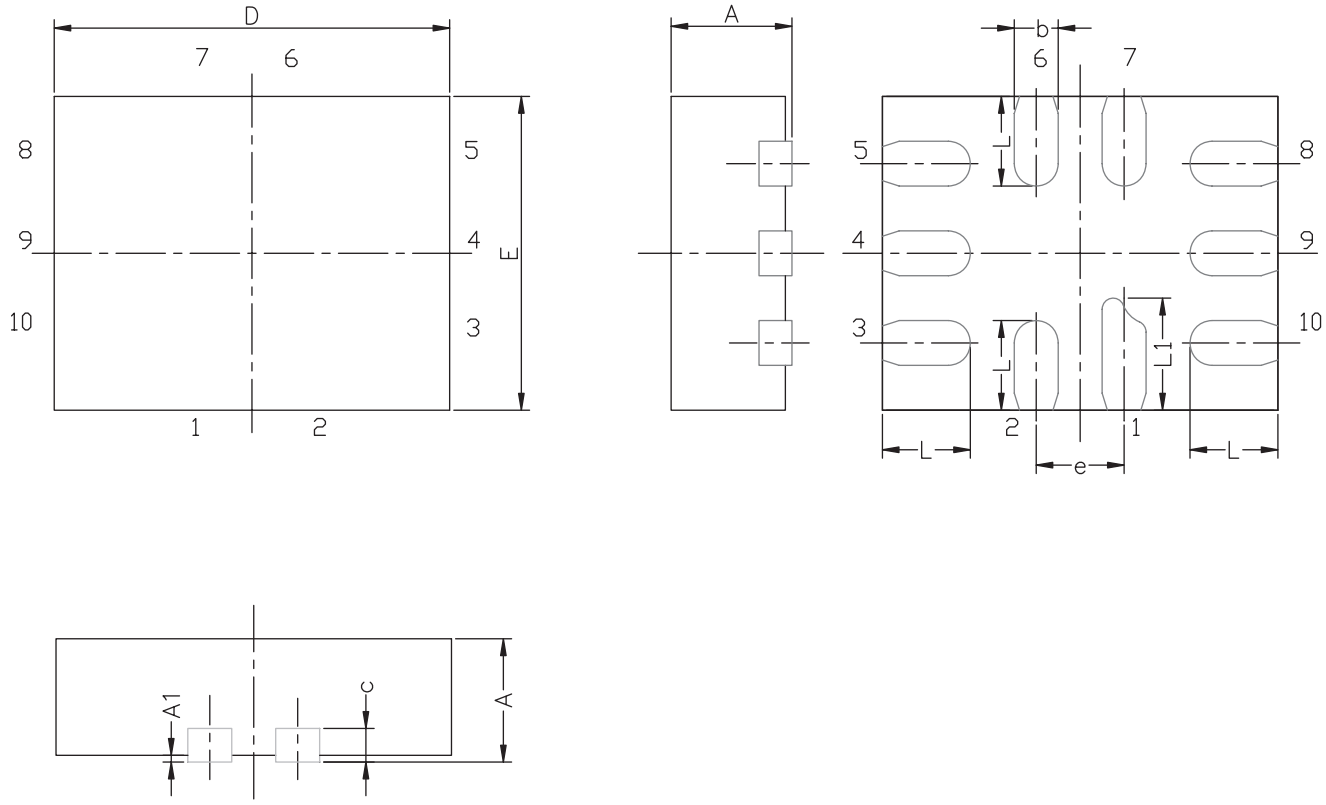


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67647.

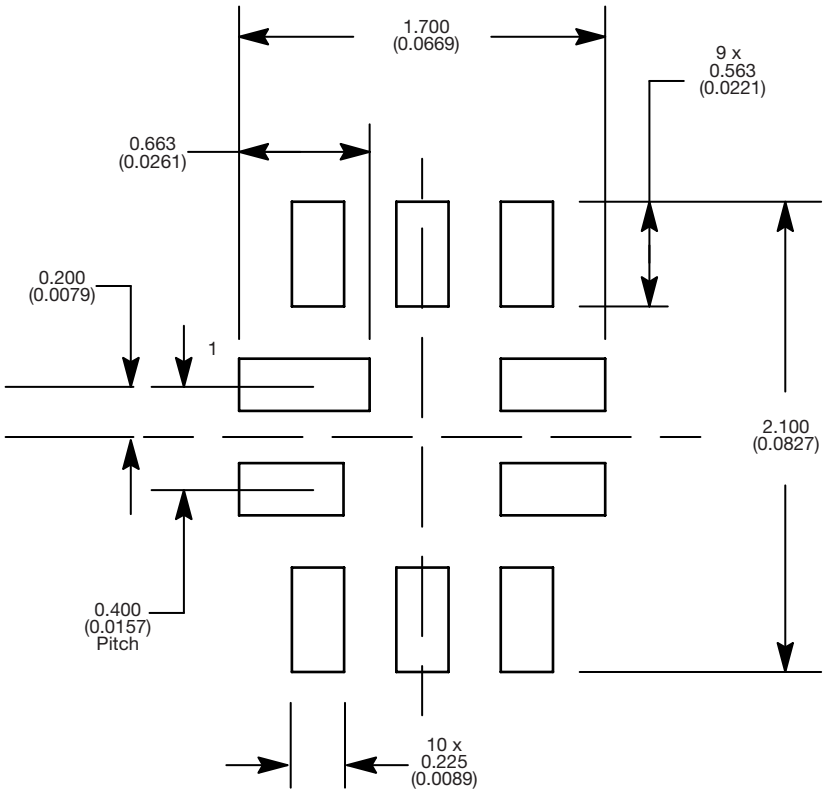
MINI QFN-10L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.15 REF			0.006 REF		
D	1.75	1.80	1.85	0.069	0.071	0.073
E	1.35	1.40	1.45	0.053	0.055	0.057
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

ECN T-07039-Rev. A, 12-Feb-07
DWG: 5957

RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint
Dimensions in mm (inch)

Disclaimer

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.