

Vishay Siliconix

RoHS

COMPLIANT

HALOGEN FREE Avaijabje

P-Channel 8-V (D-S) MOSFET

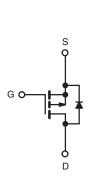
PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)	
	0.040 at V _{GS} = - 4.5 V	- 4.1		
- 8	0.060 at V _{GS} = - 2.5 V	- 3.4	7.8 nC	
	0.088 at V _{GS} = - 1.8 V	- 2.0		

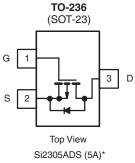
FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested

APPLICATIONS

- Load Switch
- DC/DC Converter





* Marking Code

Ordering Information: Si2305ADS-T1-E3 (Lead (Pb)-free) Si2305ADS-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel	MOSEET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 8	v	
Gate-Source Voltage		V _{GS}	± 8		
	T _C = 25 °C		- 5.4		
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C		- 4.3		
Continuous Drain Current $(T_j = 150 \text{ C})$	T _A = 25 °C		- 4.1 ^{a, b}		
	T _A = 70 °C		- 3.3 ^{a, b}	A	
Pulsed Drain Current		I _{DM}	- 10		
Continuous Courses Drain Diada Current	T _C = 25 °C		- 1.4		
Continuous Source-Drain Diode Current	T _A = 25 °C	Is	- 0.8 ^{a, b}		
	T _C = 25 °C		1.7		
Maximum Davier Dissignation	T _C = 70 °C		1.1	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	0.96 ^{a, b}	VV	
	T _A = 70 °C		0.62 ^{a, b}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 50 to 150	<u></u>	
Soldering Recommendations (Peak Temperature)		1	260	-0	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

New Product

Si2305ADS

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THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	100	130	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	60	75	0/11

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 175 °C/W.

SPECIFICATIONS $T_J = 25 \text{ °C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•		•	•	•		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 55		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η _D = - 250 μΑ		2.1			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 0.45		- 0.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$			± 100	nA	
Zara Cata Valtaga Durin Ourrant	lago	$V_{DS} = -8 V, V_{GS} = 0 V$			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -8 V, V_{GS} = 0 V, T_{J} = 55 °C$			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 5 V, V_{GS} = - 4.5 V	- 5			A	
		V _{GS} = - 4.5 V, I _D = - 4.1 A		0.032	0.040	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 3.4 A		0.048	0.060		
		V _{GS} = - 1.8 V, I _D = - 2.0 A		0.070	0.088		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 5 V, I _D = - 4.1 A		8		S	
Dynamic ^b		•	•	•	•	•	
Input Capacitance	C _{iss}			740			
Output Capacitance	C _{oss}	V _{DS} = - 4 V, V _{GS} = 0 V, f = 1 MHz		290		pF	
Reverse Transfer Capacitance	C _{rss}			190			
T + 1 0 + 0	Qg	$V_{DS} = -4 V$, $V_{GS} = -4.5 V$, $I_{D} = -4.1 A$		7.8	15	nC	
Total Gate Charge				4.5	9		
Gate-Source Charge	Q _{gs}	$V_{DS} = -4 V, V_{GS} = -2.5 V, I_{D} = -4.1 A$		1.2			
Gate-Drain Charge	Q _{qd}			1.6		1	
Gate Resistance	R _g	f = 1 MHz	1.4	7	14	Ω	
Turn-On Delay Time	t _{d(on)}			13	20		
Rise Time	t _r	$V_{DD} = -4 V, R_{L} = 1.2 \Omega$		35	53	1	
Turn-Off DelayTime	t _{d(off)}	$\text{I}_\text{D}\cong$ - 3.3 A, V_GEN = - 4.5 V, R_g = 1 Ω		32	48		
Fall Time	t _f			10	20		
Turn-On Delay Time	t _{d(on)}			5	10	ns	
Rise Time	t _r	V_{DD} = - 4 V, R_L = 1.2 Ω		11	17		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 3.3 A, V_{GEN} = - 8 V, R_g = 1 Ω		22	33	1	
Fall Time	t _f	, , , , , , , , , , , , , , , , , , ,		16	24		
Drain-Source Body Diode Characterist	ics	·		•			
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 1.4		
Pulse Diode Forward Current ^a	I _{SM}				- 10	A	
Body Diode Voltage	V _{SD}	I _F = - 3.3 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			33	50	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			14	21	nC	
Reverse Recovery Fall Time	t _a	$I_F = -3.3 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^{\circ}\text{C}$		14			
Reverse Recovery Rise Time	t _b			19		ns	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

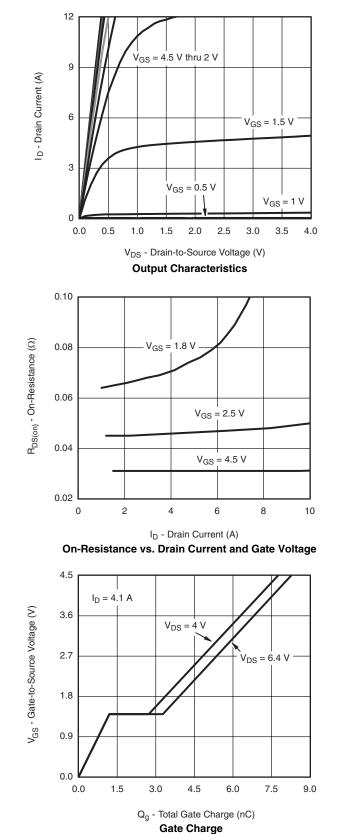
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

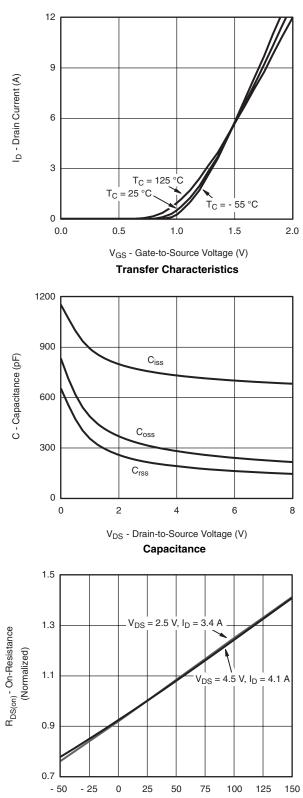




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





T_J - Junction Temperature (°C)

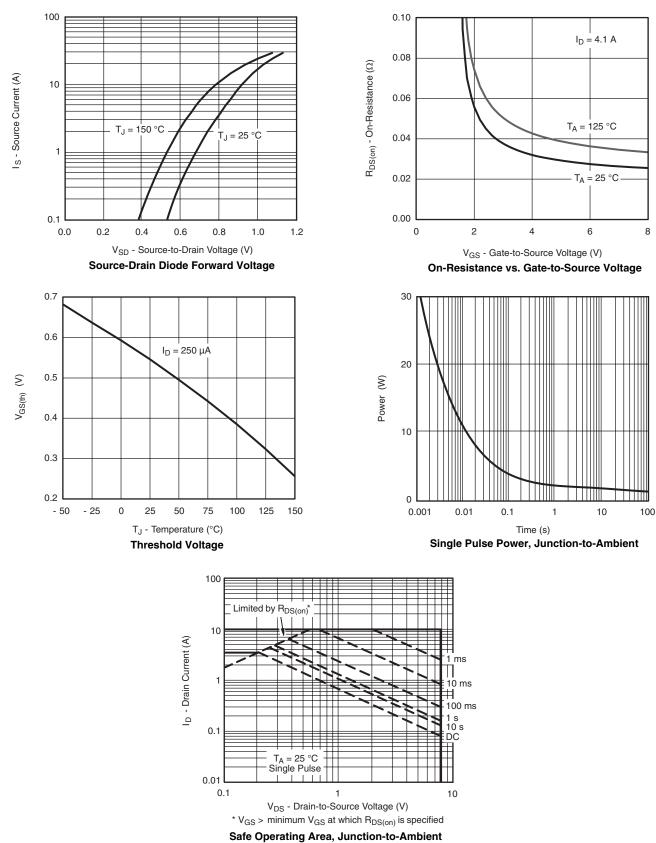
On-Resistance vs. Junction Temperature

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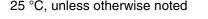


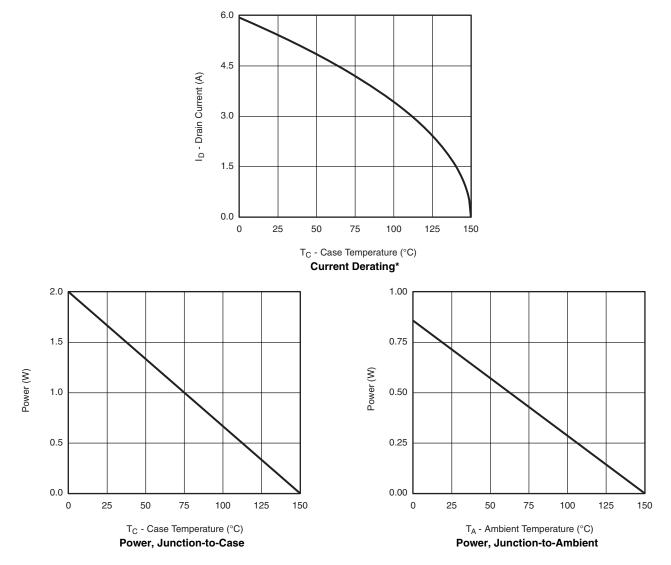




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



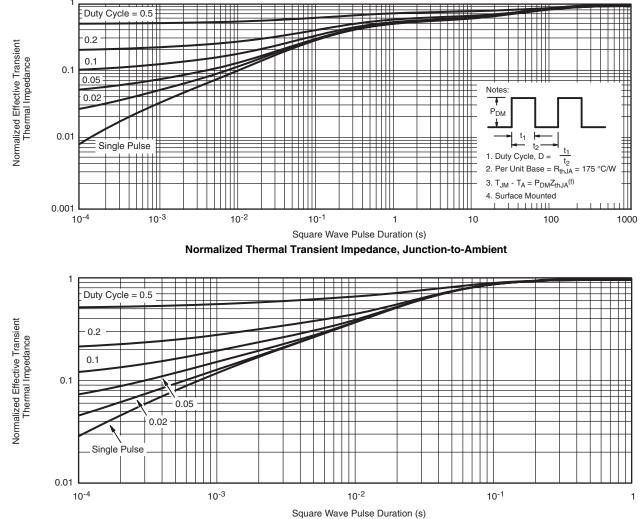


* The power dissipation PD is based on TJ(max) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg269940</u>.



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