APPLICATION NOTE

Atmel AT04389: Connecting SAMD20E to the AT86RF233 Transceiver

Atmel SAMD20

Description

This application note describes a method to connect an Atmel® ATSAMD20E microcontroller to an Atmel AT86RF233 IEEE® 802.15.4 Wireless Transceiver. The 32-pin SAM D20E is gaining popularity as a baseband processor for wireless applications. The current development platform uses the 64-pin SAM D20J on the ATSAMD20-XPRO and RF233-XPRO extender board. This combination is supported in Atmel Studio 6. To translate firmware written for the 64-pin platform to a 32-pin target product several layers of signal mapping; such as the 64-pin to 32-pin conversion and header I/O constraints, have to be reconciled. This paper offers a solution that matches the target product topology to the legacy development platform as closely as possible.

Features

- Essential Hardware Connections
- Development Platform Compatibility
- 64-Pin to 32-Pin Mapping
- Signal Map Spreadsheet
- Example Schematic

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1. Description

This application note describes a method to connect an Atmel ATSAMD20E to an AT86RF233 IEEE 802.15.4 Wireless Transceiver. The 32-pin SAM D20E is gaining popularity as a baseband processor for wireless applications. The current development platform uses the 64-pin SAM D20J on the ATSAMD20-XPRO and RF233-XPRO extender board. This combination is supported in Atmel Studio 6. To translate firmware written for the 64-pin platform to a 32-pin target product several layers of signal mapping; such as the 64-pin to 32-pin conversion and header I/O constraints, have to be reconciled. This paper offers a solution that matches the target product topology to the legacy development platform as closely as possible.

2. Signal_map.xlsx Spreadsheet

The spreadsheet and schematics included with the application note show the basic connections that should be made between the SAMD20E and the RF233. This is a starting point for new work. Designers can use the remaining I/O and features on the D20E as needed for their derivative projects.

The following section describes the column grouping of the signal_map.xlsx spreadsheet. The column group on the left *SAM D20J XPRO (64 Pin*) is the starting point. This column is the 64-pin SAMD20J signal definitions. Each level of interconnect is shown in a column group. Each signal is shown in a single row. The signals cascade from left-to-right starting with the 64-pin SAMD20J to the final connections on the 32-pin SAMD20E target product. As the signals cascade across the spreadsheet some drop off because of various interface constraints and the matrix becomes sparsely populated.

The SAMD20 processor uses SERCOM ports and MUX modes to on-board sub-systems to the “PA” ports and I/O pins. Table “PORT Function Multiplexing” of the SAMD20 datasheet [1] explains the different permutations and connections possible for various SAMD20-package options. This paper is focused on the 64-pin D20J and the 32-pin D20E. Some of the SECOM ports, such as SERCOM4, are not available on the smaller 32-pin package. This forces the UART migration from SERCOM4 to SERCOM3 on the target product. Additionally the PIN locations are re-organized for the smaller package.

The next column group in the mapping, *XPRO-EX2*, is the Xplained PRO EXT2 header. The designers of the Xplained PRO EK family have chosen a limited set of I/O that provides a uniform interface across a broad line of products. These choices limit the signals available and mandate certain combinations. For example signals like RESETN and SWD programming interface are not included in this interface. These need to be defined ad-hoc on the target product.

Firmware developers using Studio 6 will want to use the REB-233 XPRO Extender card to add the radio transceiver to the SAMD20 CPU. There is a column group for this card too, *REB-233 XPRO*. This card has some interesting features like ID_PROM and UART that are not on the basic target product. These signals are abandoned at this level.

For reference the next column group, *AT86RF233*, shows the low-level connections to the AT86RF233. All the connections on the RF233, including the segregated analog and digital power domains, are shown to give a complete picture of the transceiver implementation.

Toward the right edge of the spreadsheet is the 32-pin SAMD20 column group, *SAM D20E (32 Pin)*. This shows the SAMD20 connections and signal names. The SPI interface and several of the control I/O signals have passing straight through the mapping matrix and are connected to the legacy PA Ports. Some new signals, such as TRX_RESET are established using the remaining GPIO on the 32-pin SAMD20E.

The final column group, *LOCAL_BUS*, identifies the net names used on the example schematic. Additionally the signals are labeled by functional group and their change status. LEGACY status indicates no change; the D20E signals match the legacy D20J signals. CHANGED status indicates the function has been moved and must be accounted for in the HAL layer of software. REMOVED status means the signal did not complete the translation through the matrix or was removed to simplify the basic design.

3. Example Schematic

The two-page schematic shows the circuitry commonly used for RF233 wireless systems. RF signal chain components such as antenna, pi matching network, balun and local oscillator are shown. The essentials for the SAMD20 baseband CPU are also shown: CPU, programming header, UART test interface and power filtering. Developers can connect additional circuitry to the unused GPIO as needed. Additional suggestions include AT24MAC602 ID-PROM for network credential storage, pushbutton and LED for wireless network binding stimulus and indication.

Note: The SAMD20 on the target product can be programmed using a jumper cable from the Xplained PRO USB interface.

The AT86RF233 datasheet [2] suggests segregating analog and digital power domains to prevent common inductance coupling of EMI. The component R4 is a virtual mnemonic device used to separate the two signals in the CAD tool. In layout this short would be implemented by connection AGND and DGND together at transceiver (Pin U3.33 the 'thermal-pad'.)

4. Conclusion

The spreadsheet and schematic give a detailed example of the SAMD20E to RF233 interface. This will give Atmel developers a head start. Projects using this connection set should readily adapt to firmware developed in Atmel Studio 6 using the ATSAMD20-XPRO. Following this application note, and using the recommended basic features, will give Atmel developers a smooth path to production.

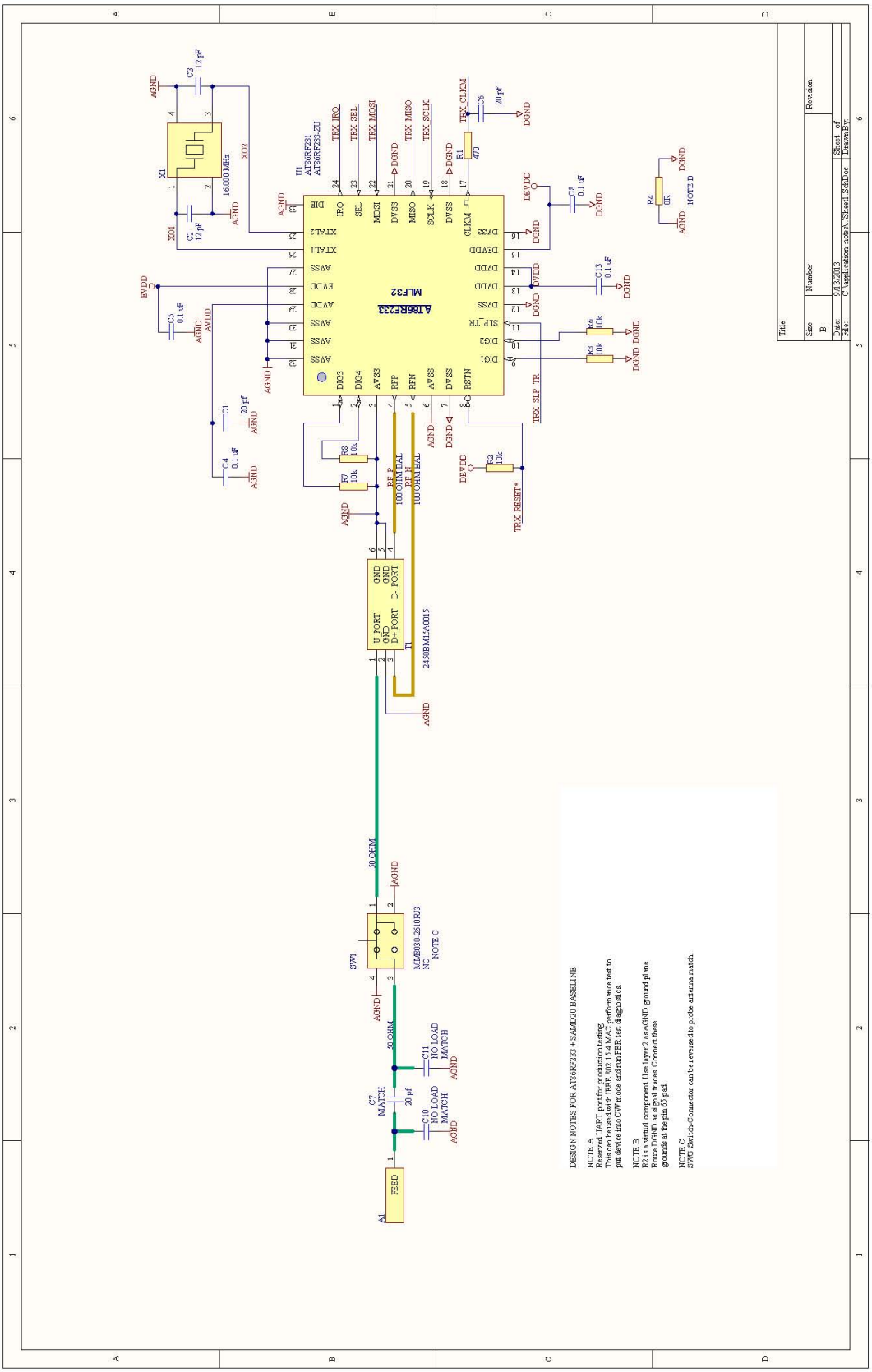
5. References

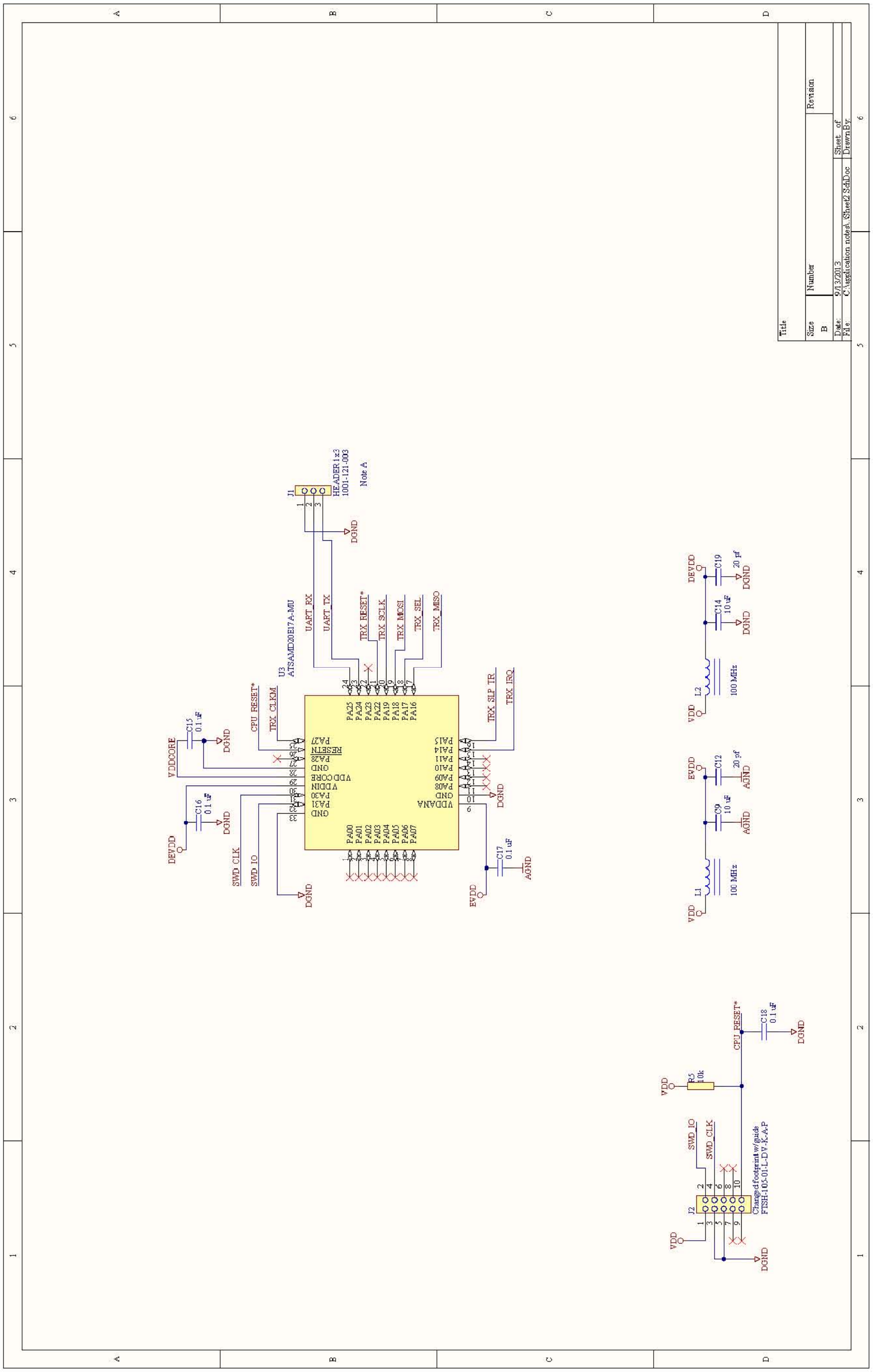
[1]. Atmel 42129 SAMD20 Datasheet
[2]. Atmel 8351 AT86RF233 Datasheet
[3]. Atmel 42102 SAM D20 Xplained Pro User Guide
[4]. A09-1873 SAMD20 XPRO Schematic (internal doc)
[5]. A08-1669 RFA233=XPRO Schematic (internal doc)

Appendix A. Signal Map Spreadsheet

ITEM	SAM D20J XPRO (64 Pin)					XPRO-EX2	REB-233 XPRO		AT86RF233		SAM D20E (32 Pin)		LOCAL_BUS		
	D20_XPRO_SIG	D20J_PIN	D20J_SIG	SERCOM	MUX	EXT2	REB_XPRO_SIG	REB_XPRO_PIN	RF233_SIG	RF233_PIN	D20E_PIN	D20E_SIG	NET_NAME	GROUP	STATUS
1	PA19_S1_SPI_SCLK	38	PA19	S1-P3	C	PIN18_SPI_CLK	SPI_CLK	J100.18	SCLK	U1.19	U3.20	PA19	TRX_SCLK	TRX	LEGACY
2	PA18_S1_SPI_MOSI	37	PA18	S1-P2	C	PIN16_SPI_MOSI	SPI_MOSI	J100.16	MOSI	U1.22	U3.19	PA18	TRX_MOSI	TRX	LEGACY
3	PA16_S1_SPI_MISO	35	PA16	S1-P0	C	PIN17_SPI_MISO	SPI_MISO	J100.17	MISO	U1.20	U3.17	PA16	TRX_MISO	TRX	LEGACY
4	PA17_S1_SPI_SS	36	PA17	S1-P1	C	PIN15_SPI_SS_A	SPI_SS_A	J100.15	SEL	U1.23	U3.18	PA17	TRX_SEL	TRX	LEGACY
5	PB12_S4_UART_TX	25	PB12	S4-P0	C	PIN14_UART_TX	UART_RX	J100.14							CHANGED
6	PB13_S4_UART_RX	26	PB13	S4-P1	C	PIN13_UART_RX	UART_TX	J100.13							CHANGED
7	PA08_S2_I2C_SDA		PA08	S2-P0	D	PIN11_TWI_SDA	TWI_SDA	J100.11						ID_PROM	REMOVED
8	PA09_S2_I2C_SCL		PA09	S2-P1	D	PIN12_TWI_SCL	TWI_SCL	J100.12						ID_PROM	REMOVED
9		52	RESETN								U3.26	RESETN	CPU_RESET*	SWD	LEGACY
10	PA30_SWDCLK	57	PA30								U3.31	PA30	SWD_CLK	SWD	LEGACY
11	PA31_SWDIO	58	PA31								U3.32	PA31	SWD_IO	SWD	LEGACY
12	PA15_GPIO_SS	32	PA15			PIN10_SPI_SS_B/GPIO	SPI_SS_B/GPIO	J100.10	SLP_TR	U1.11	U3.16	PA15	TRX_SLP_TR	TRX	LEGACY
13	PA14_GPIO_IRQ4	31	PA14			PIN9_IRQ/GPIO	IRQ/GPIO	J100.09	IRQ	U1.24	U3.15	PA14	TRX_IRQ	TRX	LEGACY
14	PA22_PWM_TC4_0	43	PA22			PIN7_PWM(+)	PWM(+)	J100.07	RSTN	U1.08	U3.21	PA22	TRX_RESET*	TRX	LEGACY
15	PA23_PWM_TC4_1	44	PA23			PIN8_PWM(-)	PWM(-)	J100.08							LEGACY
16	PA10_ADC18	13	PA10			PIN3_ADC(+)	ADC(+)	J100.03	DIG1	U1.09			PULL_DOWN	TRX	REMOVED
17	PA11_ADC19	14	PA11			PIN4_ADC(-)	ADC(-)	J100.04	DIG3	U1.01			PULL_DOWN	TRX	REMOVED
18	PA20_GPIO	41				PIN5_GPIO	GPIO	J100.05	DIG2	U1.10			PULL_DOWN	TRX	REMOVED
19	PA21_GPIO	42				PIN6_GPIO	GPIO	J100.06	CLKM	U1.17	U3.25	PA27	TRX_CLKM	TRX	LEGACY
20	PA24_S3_UART_TX	45	PA24	S3-P2	C						U3.23	PA24	TX	UART	CHANGED
21	PA52_S3_UART_RX	46	PA25	S3-P3	C						U3.24	PA25	RX	UART	CHANGED
22											U3.09	VDDANA	EVDD	POWER	
23											U3.10	GND	DGND	POWER	
24											U3.28	GND	DGND	POWER	
25											U3.29	VDDCORE	VDDCORE	POWER	
26											U3.30	VDDIN	DEVDD	POWER	
27											U3.33	PAD	DGND	POWER	
28									DIG4	U1.02			PULL_DOWN	TRX	
29									AVSS	U1.03			AGND	POWER	
30									RFP	U1.04			RF_P	TRX	
31									RFN	U1.05			RF_N	TRX	
32									AVSS	U1.06			AGND	POWER	
33									DVSS	U1.07			DGND	POWER	
34									DVSS	U1.12			DGND	POWER	
35									DVDD	U1.13			DVDD	POWER	
36									DVDD	U1.14			DVDD	POWER	
37									DEVDD	U1.15			DEVDD	POWER	
38									DVSS	U1.16			DGND	POWER	
39									DVSS	U1.18			DGND	POWER	
40									DVSS	U1.21			DGND	POWER	
41									XTAL2	U1,25			XO2	XO	
42									XTAL1	U1.26			XO1	XO	
43									AVSS	U1.27			AGND	POWER	
44									EVDD	U1.28			EVDD	POWER	
45									AVDD	U1.29			AVDD	POWER	
46									AVDD	U1.30			AVDD	POWER	
47									AVDD	U1.30			AVDD	POWER	
48									AVDD	U1.32			AVDD	POWER	
49									PAD	U1.33			AVDD	POWER	

Appendix B. Example Schematic





ATSAMD20E17A-MU
U3
UART_RX
UART_TX
TRX_RESET*
TRX_SCLK
TRX_MOSI
TRX_SEL
TRX_MISO
TRX_SLP_TR
TRX_IRQ
CPU_RESET*
TRX_CLKM
VDDCORE
DEVDD
EVDD
SWD_CLK
SWD_IO
DGND
AGND
J1
HEADER 1x3
1001-121-003
Note A
J2
FTSH-105-01-L-DV-K-A-P
R5
10k
100 MHz
Title
Size
B
Number
Revision
Date:
9/13/2013
Sheet of
Drawn By:

Appendix C. Revision History

Doc. Rev.	Date	Comments
42189B	10/2013	The document title has changed from “SAMD20E to Wireless Connections” to “Connecting SAMD20E to the AT86RF233 Transceiver”
42189A	09/2013	Initial document release

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