



# Automotive P-Channel 40 V (D-S) 175 °C MOSFET



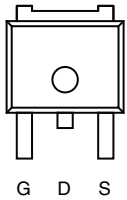
RoHS COMPLIANT HALOGEN FREE

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	- 40
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = - 10 V	0.0094
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = - 4.5 V	0.0160
I <sub>D</sub> (A)	- 90
Configuration	Single

## FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R<sub>g</sub> and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

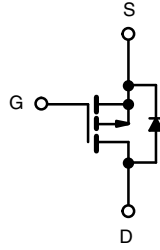
TO-252



G D S

Top View

Drain Connected to Tab



P-Channel MOSFET

ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD90P04-9m4L-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	- 40	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 90
		T <sub>C</sub> = 125 °C	- 52
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	- 100	A
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	- 160	
Single Pulse Avalanche Current	I <sub>AS</sub>	- 50	
Single Pulse Avalanche Energy	E <sub>AS</sub>	125	
Maximum Power Dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	136
		T <sub>C</sub> = 125 °C	45
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R <sub>thJA</sub>	50	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	1.1	

### Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA		- 40	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA		- 1.5	-	- 2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V	-	-	- 1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V, T <sub>J</sub> = 125 °C	-	-	- 50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V, T <sub>J</sub> = 175 °C	-	-	- 150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> ≤ - 5 V	- 50	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 17 A	-	0.0075	0.0094	Ω
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 50 A, T <sub>J</sub> = 125 °C	-	-	0.0147	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 50 A, T <sub>J</sub> = 175 °C	-	-	0.0178	
		V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 14 A	-	0.0130	0.0160	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 17 A		-	46	-	S
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 20 V, f = 1 MHz	-	5339	6675	pF
Output Capacitance	C <sub>oss</sub>			-	852	1065	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	681	855	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 20 V, I <sub>D</sub> = - 50 A	-	103	155	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	15	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	21	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.4	2.8	4.2	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 0.4 Ω I <sub>D</sub> ≅ - 50 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		-	13	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	15	23	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	61	92	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	19	29	
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 160	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = - 50 A, V <sub>GS</sub> = 0 V		-	- 0.95	- 1.5	V

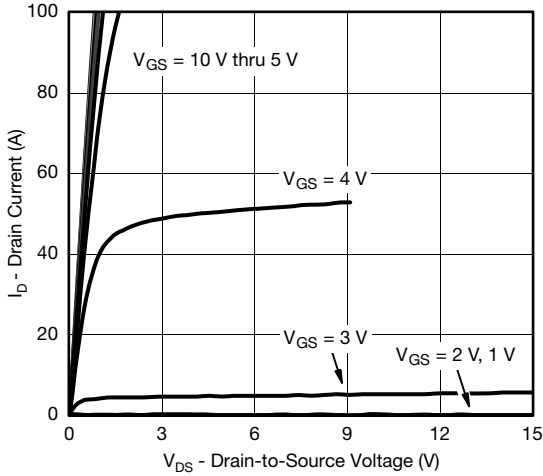
**Notes**

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

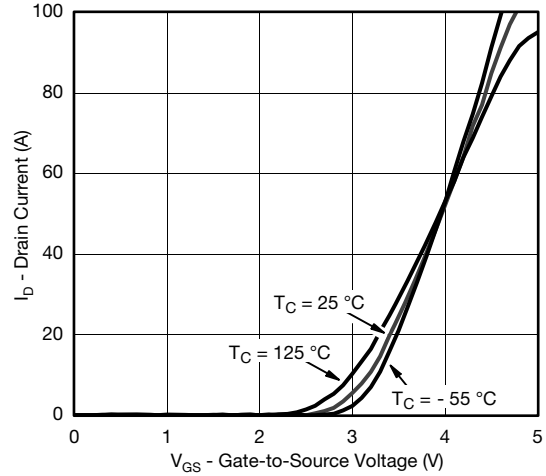
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



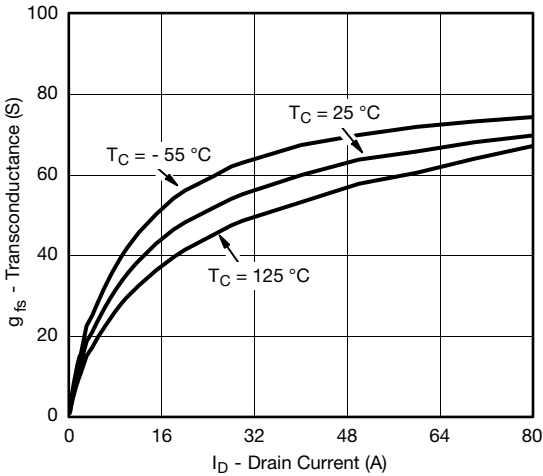
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



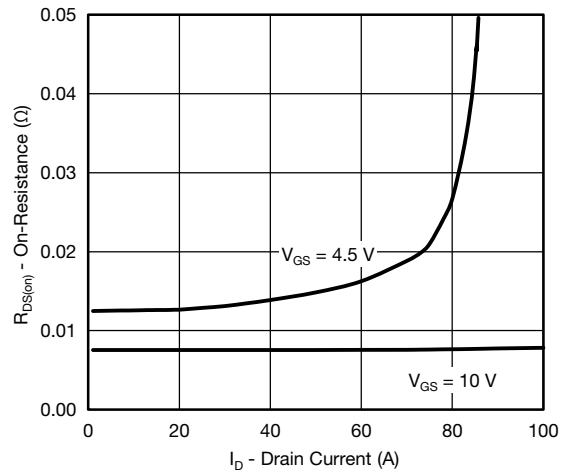
Output Characteristics



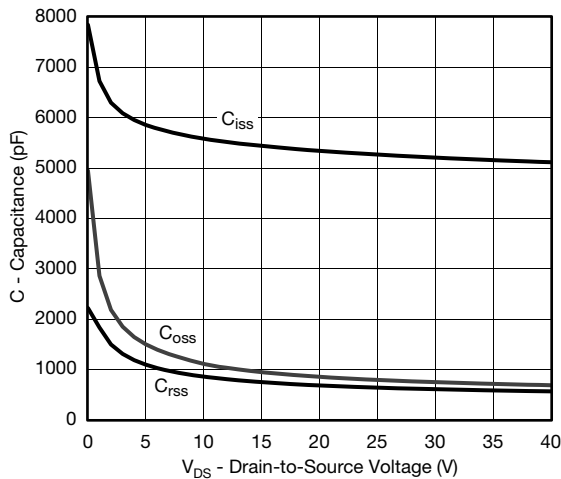
Transfer Characteristics



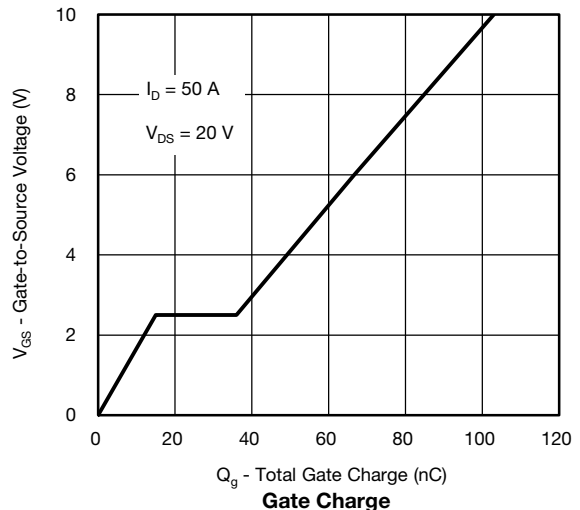
Transconductance



On-Resistance vs. Drain Current



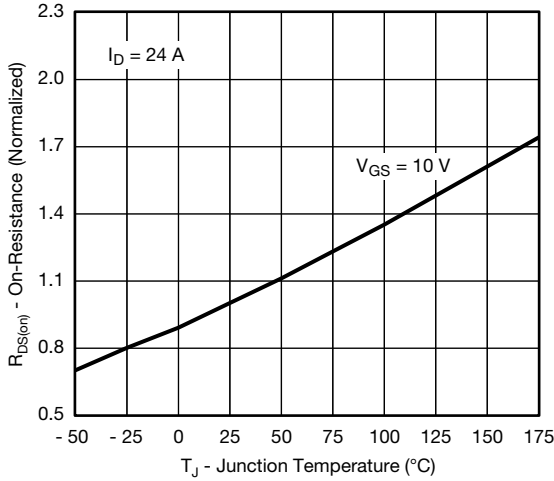
Capacitance



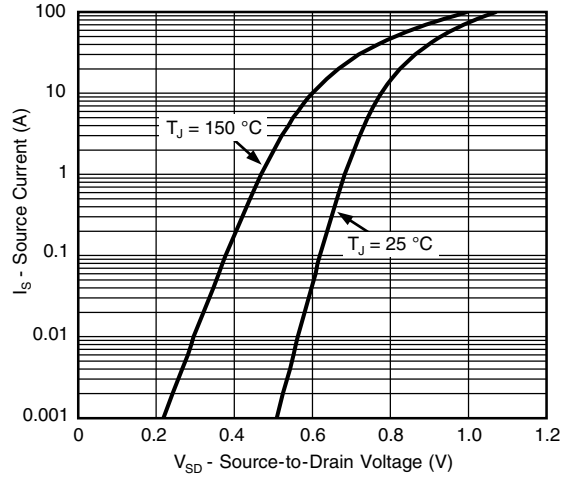
Gate Charge



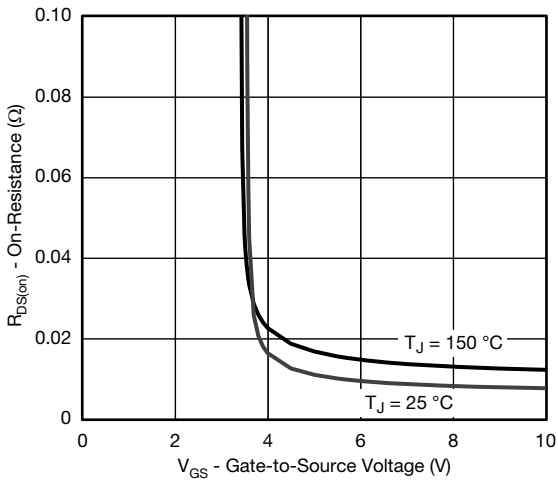
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



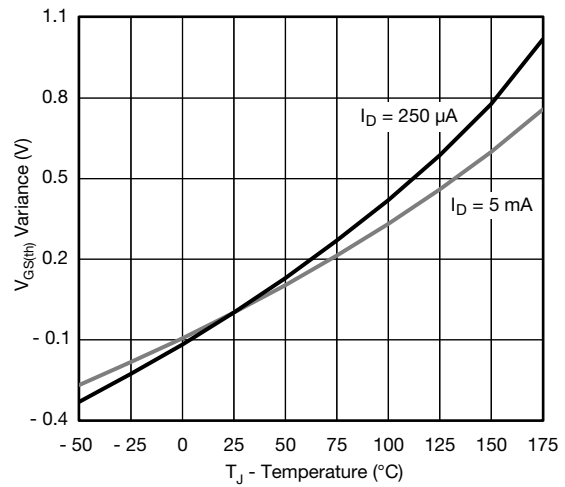
On-Resistance vs. Junction Temperature



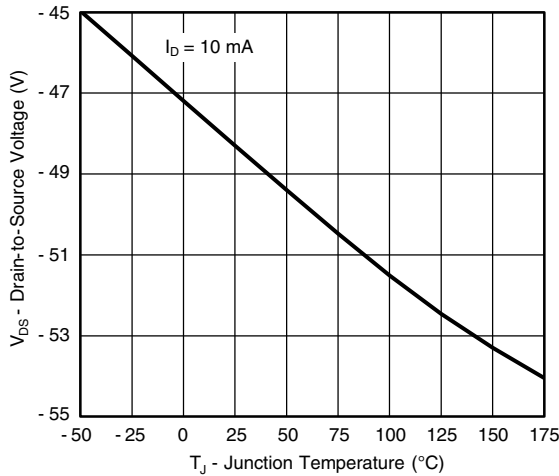
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



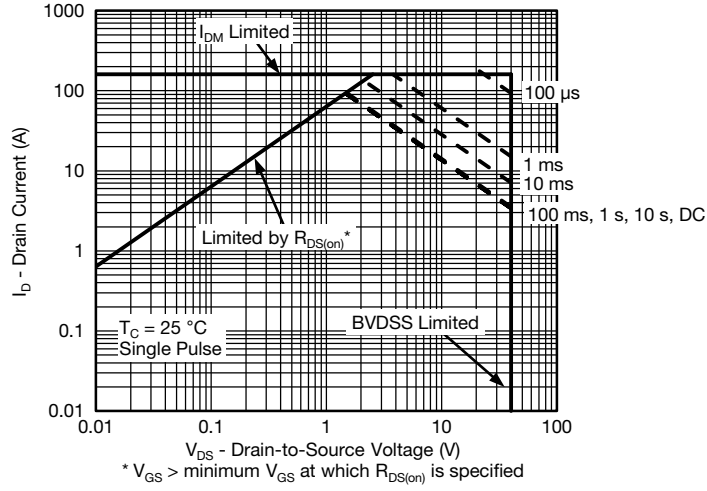
Threshold Voltage



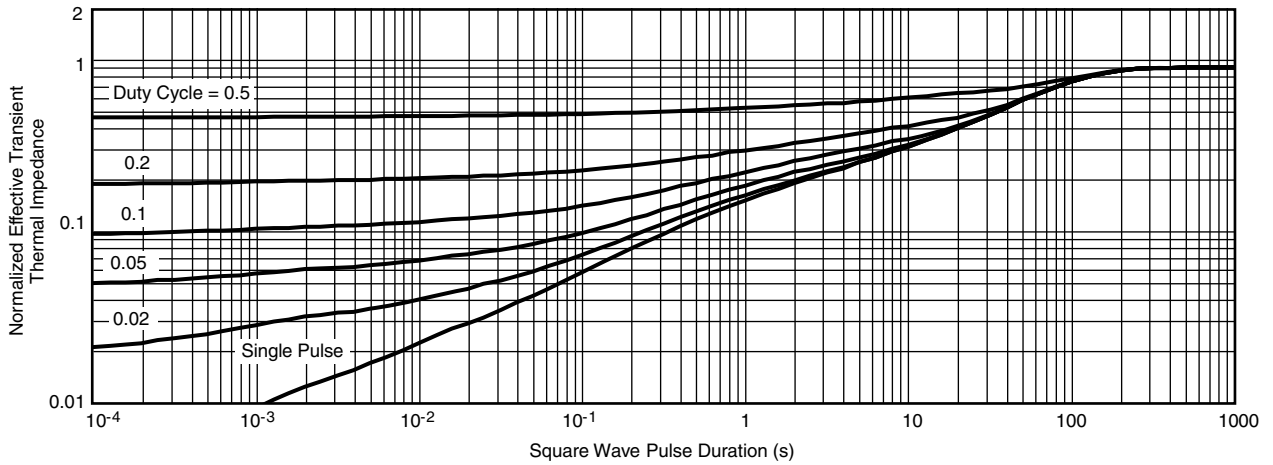
Drain Source Breakdown vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



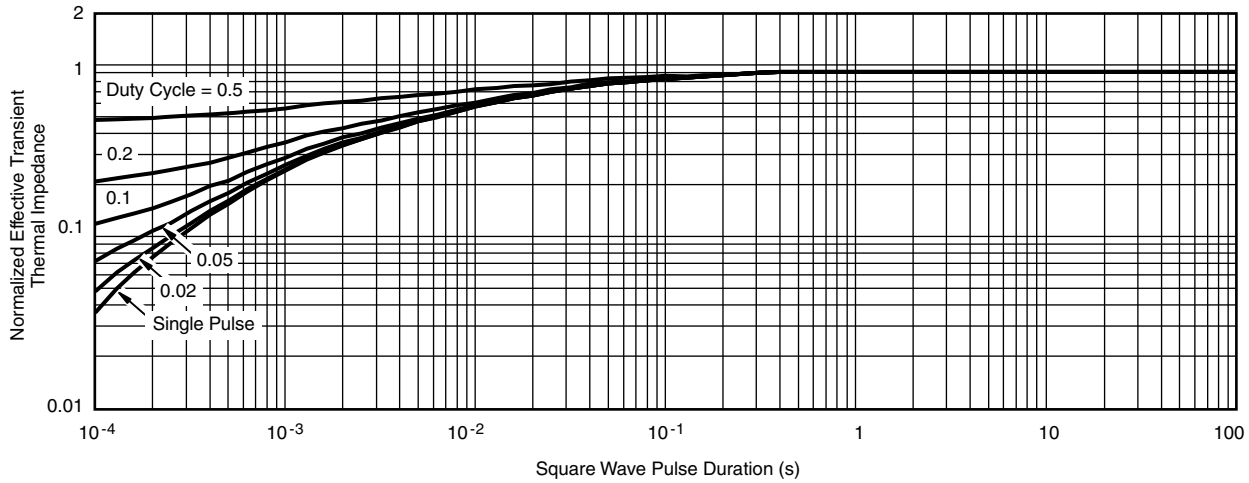
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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DPAK / TO-252 and Reverse DPAK

Ordering codes for the SQ rugged series power MOSFETs in the DPAK / TO-252 and Reverse DPAK packages:

Table with 3 columns: DATASHEET PART NUMBER, OLD ORDERING CODE a, NEW ORDERING CODE. Lists various MOSFET part numbers and their corresponding ordering codes.

Note

a. Old ordering code is obsolete and no longer valid for new orders



### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13				
DWG: 6019				

**Note**

- Dimension L3 is for reference only.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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