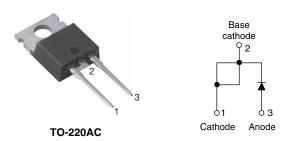
VS-10ETS...PbF Series, VS-10ETS...M3 Series

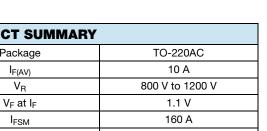
Vishay Semiconductors

High Voltage, Input Rectifier Diode, 10 A



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PRODUCT SUMMARY					
Package	TO-220AC				
I _{F(AV)}	10 A				
V_{R}	800 V to 1200 V				
V _F at I _F	1.1 V				
I _{FSM}	160 A				
T _J max.	150 °C				
Diode variation	Single die				



FEATURES

- Very low forward voltage drop
- 150 °C max. operating junction temperature
- · Designed and qualified according to JEDEC-JESD47
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912







APPLICATIONS

- Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

DESCRIPTION

High voltage rectifiers optimized for very low forward voltage drop with moderate leakage.

These devices are intended for use in main rectification (single or three phase bridge).

OUTPUT CURRENT IN TYPICAL APPLICATIONS						
APPLICATIONS SINGLE-PHASE BRIDGE THREE-PHASE BRIDGE UNITS						
Capacitive input filter T _A = 55 °C, T _J = 125 °C common heatsink of 1 °C/W	12.0	16.0	A			

MAJOR RATINGS AND CHARACTERISTICS							
SYMBOL	CHARACTERISTICS	VALUES	UNITS				
I _{F(AV)}	Sinusoidal waveform	10	A				
V _{RRM}		800/1200	V				
I _{FSM}		160	A				
V _F	10 A, T _J = 25 °C	1.1	V				
TJ		- 40 to 150	°C				

VOLTAGE RATINGS						
PART NUMBER	V _{RRM} , MAXIMUM PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I _{RRM} AT 150 °C mA			
VS-10ETS08PbF, VS-10ETS08-M3	800	900	0.5			
VS-10ETS12PbF, VS-10ETS12-M3	1200	1300	0.5			

ABSOLUTE MAXIMUM RATINGS							
PARAMETER SYMBOL		TEST CONDITIONS	VALUES	UNITS			
Maximum average forward current	I _{F(AV)}	T _C = 105 °C, 180° conduction half sine wave	10				
Maximum peak one cycle	I	10 ms sine pulse, rated V _{RRM} applied	135	Α			
non-repetitive surge current	I _{FSM}	10 ms sine pulse, no voltage reapplied	160				
Maximum I ² t for fusing	I ² t	10 ms sine pulse, rated V _{RRM} applied	91	A ² s			
Maximum 1-t for fusing		10 ms sine pulse, no voltage reapplied	130	A-5			
Maximum I ² √t for fusing	l²√t	t = 0.1 ms to 10 ms, no voltage reapplied	1300	A²√s			

VS-10ETS...PbF Series, VS-10ETS...M3 Series

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ELECTRICAL SPECIFICATIONS							
PARAMETER SYMBOL TEST CONDITIONS					UNITS		
Maximum forward voltage drop	V_{FM}	10 A, T _J = 25 °C		1.1	V		
Forward slope resistance	r _t	T _{.1} = 150 °C	20	mΩ			
Threshold voltage	V _{F(TO)}	1j = 150 C	0.82	V			
Mariana		T _J = 25 °C		0.05	Л		
Maximum reverse leakage current	I _{RM}	T _J = 150 °C	V _R = Rated V _{RRM}	0.50	mA		

THERMAL - MECHANICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum junction and storage temperature range	T _J , T _{Stg}		- 40 to 150	°C			
Maximum thermal resistance, junction to case	R _{thJC}	DC operation	2.5				
Maximum thermal resistance, junction to ambient (PCB mount)	R _{thJA}		62	°C/W			
Soldering temperature	T _S		240	°C			
Approximate weight			2	g			
Approximate weight			0.07	OZ.			
Marking davise		Case style TO-220AC	10ETS08				
Marking device		Case style 10-220AC	10ETS12				

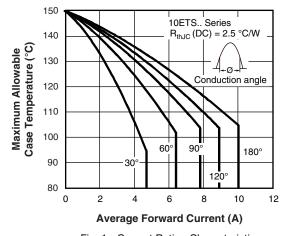


Fig. 1 - Current Rating Characteristics

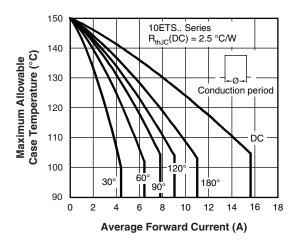


Fig. 2 - Current Rating Characteristics



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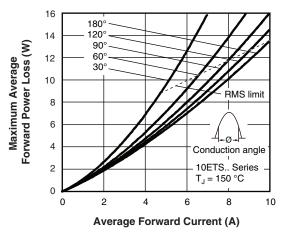


Fig. 3 - Forward Power Loss Characteristics

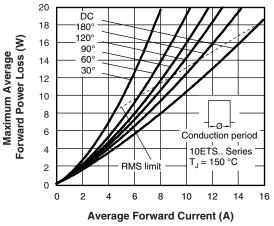


Fig. 4 - Forward Power Loss Characteristics

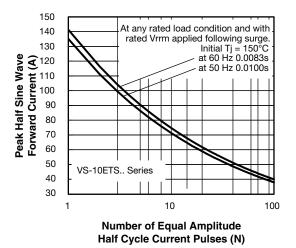


Fig. 5 - Maximum Non-Repetitive Surge Current

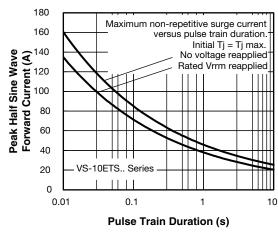


Fig. 6 - Maximum Non-Repetitve Surge Current

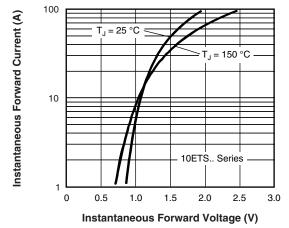


Fig. 7 - Forward Voltage Drop Characteristics

VS-10ETS...PbF Series, VS-10ETS...M3 Series

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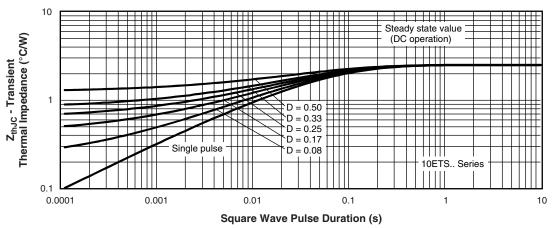


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	10	E	т	s	12	PbF
	1	2	3	4	5	6	7
	1 2 3	- Cu - Cir	hay Sem rrent ration cuit confi	ng (10 = iguration	10 A)	oduct	
	4		ckage: TO-220	۸۰			
	5	-	oe of silic				
		S =	Standar	d recove	ery recti	ifier	

6 - Voltage code x 100 = V_{RRM} - 12 = 1200 V

7 - Environmental digit:

PbF = Lead (Pb)-free and RoHS compliant

-M3 = Halogen-free, RoHS compliant and terminations lead (Pb)-free

ORDERING INFORMATION (Example)							
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION				
VS-10ETS08PbF	50	1000	Antistatic plastic tubes				
VS-10ETS08-M3	50	1000	Antistatic plastic tubes				
VS-10ETS12PbF	50	1000	Antistatic plastic tubes				
VS-10ETS12-M3	50	1000	Antistatic plastic tubes				

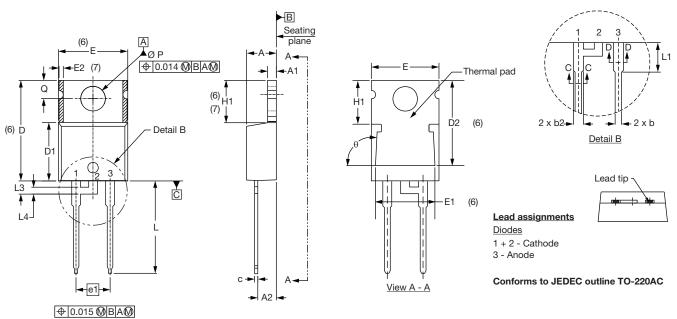
LINKS TO RELATED DOCUMENTS				
Dimensions www.vishay.com/doc?95221				
Part marking information	TO-220AC PbF	www.vishay.com/doc?95224		
Fart marking information	TO-220AC -M3	www.vishay.com/doc?95068		



Vishay Semiconductors

TO-220AC

DIMENSIONS in millimeters and inches



SYMBOL	MILLIM	IETERS	INC	HES	NOTES
STIVIBUL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
Е	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIM	IETERS	INCHES		NOTES	
STIVIBUL	MIN.	MAX.	MIN.	MAX.	NOTES	
E1	6.86	8.89	0.270	0.350	6	
E2	-	0.76	-	0.030	7	
е	2.41	2.67	0.095	0.105		
e1	4.88	5.28	0.192	0.208		
H1	6.09	6.48	0.240	0.255	6, 7	
L	13.52	14.02	0.532	0.552		
L1	3.32	3.82	0.131	0.150	2	
L3	1.78	2.13	0.070	0.084		
L4	0.76	1.27	0.030	0.050	2	
ØΡ	3.54	3.73	0.139	0.147		
Q	2.60	3.00	0.102	0.118		
θ	90° t	o 93°	90° t	o 93°		

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline



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