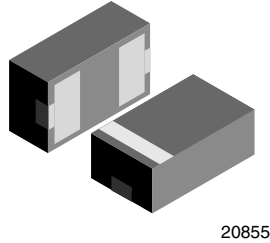
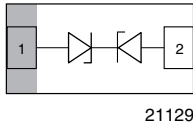


# Bidirectional Symmetrical (BiSy) Single Line ESD-Protection Diode in LLP1006-2M


**MARKING** (example only)


Bar = pin 1 marking  
 X = date code  
 Y = type code (see table below)

**FEATURES**

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD-protection
- Working range  $\pm 5.5$  V
- Low leakage current < 0.1  $\mu$ A
- Low load capacitance  $C_D = 10$  pF
- ESD-protection acc. IEC 61000-4-2  
 $\pm 30$  kV contact discharge  
 $\pm 30$  kV air discharge
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VCUT05B1-DD1	VCUT05B1-DD1-G-08	8000	8000

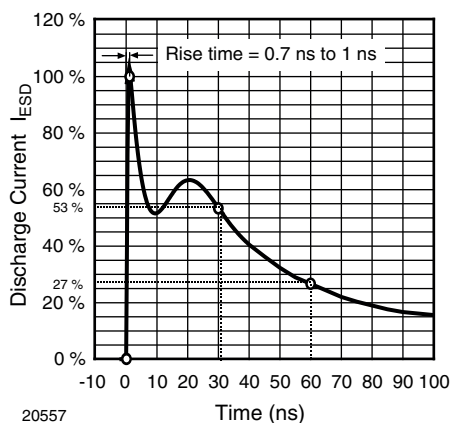
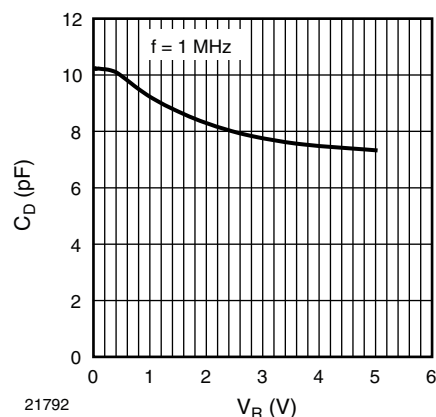
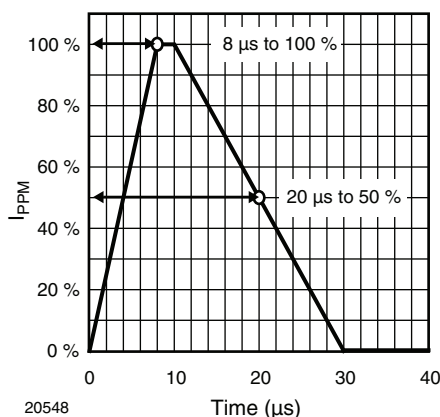
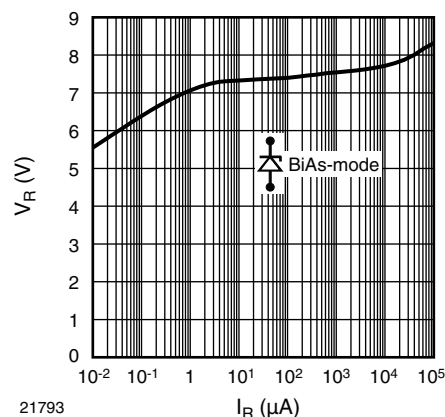
PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VCUT05B1-DD1	LLP1006-2M	P	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VCUT05B1-DD1				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot	$I_{PPM}$	3	A
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot	$P_{PP}$	38	W
ESD immunity	Contact discharge acc. IEC61000-4-2; 10 pulses	$V_{ESD}$	$\pm 30$	kV
	Air discharge acc. IEC61000-4-2; 10 pulses	$V_{ESD}$	$\pm 30$	
Operating temperature	Junction temperature	$T_J$	-55 to +145	°C
Storage temperature		$T_{stg}$	-55 to +150	°C

**CUT THE SPIKES WITH VCUT05B1-DD1**

The VCUT05B1-DD1 is a Bidirectional and Symmetrical (BiSy) ESD-protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT05B1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like and ESD-strike can be clamped with minimal over- or undershoots.

<b>ELECTRICAL CHARACTERISTICS VCUT05B1-DD1</b>						
$(T_{amb} = 25\text{ }^{\circ}\text{C}, \text{ unless otherwise specified})$						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at $I = 0.1\text{ }\mu\text{A}$	$V_R$	5.5	-	-	V
Reverse current	at $V = 5.5\text{ V}$	$I_R$	-	-	0.1	$\mu\text{A}$
Reverse breakdown voltage	at $I = 1\text{ mA}$	$V_{BR}$	6	7.5	8.5	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$	$V_C$	-	8.3	10.5	V
	at $I_{PP} = I_{PPM} = 3\text{ A}$	$V_C$	-	10.3	12.5	V
Capacitance	at $V = 0\text{ V}; f = 1\text{ MHz}$	$C_D$	-	10	13	pF
	at $V = 2.5\text{ V}; f = 1\text{ MHz}$	$C_D$	-	8	-	pF

**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}, \text{ unless otherwise specified}$ )

 Fig. 1 - ESD Discharge Current Wave Form  
 acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

 Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$ 

 Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
 acc. IEC 61000-4-5

 Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

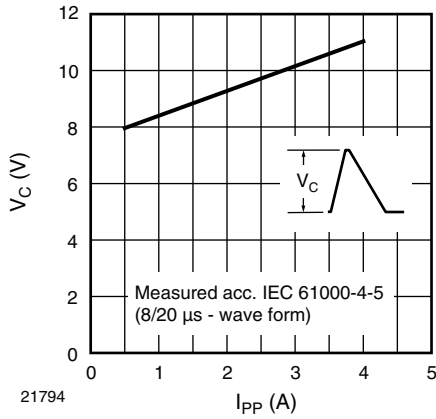


Fig. 5 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$

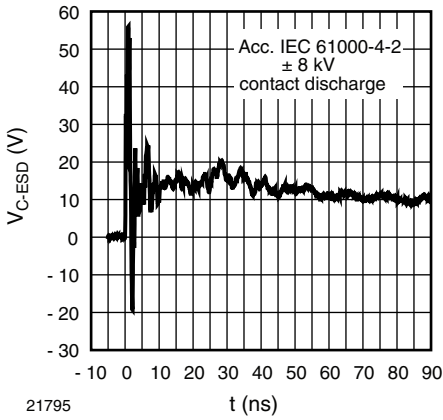


Fig. 6 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

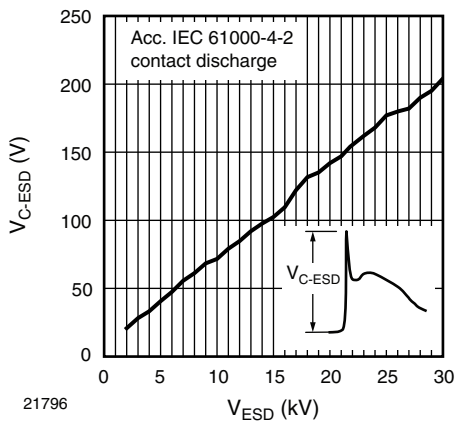
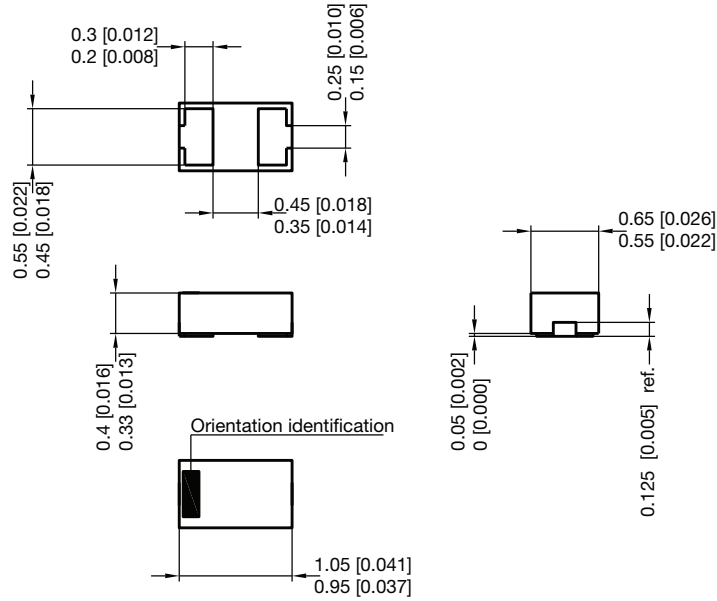


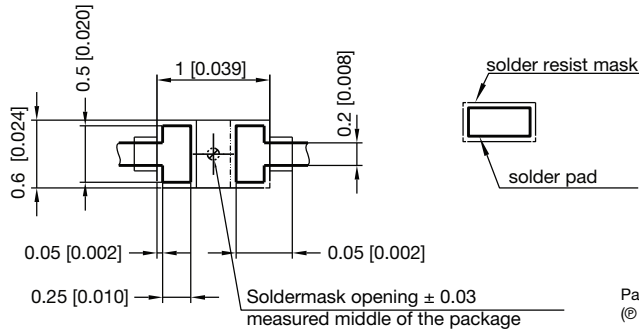
Fig. 7 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)



PACKAGE DIMENSIONS in millimeters (inches): **LLP1006-2M**

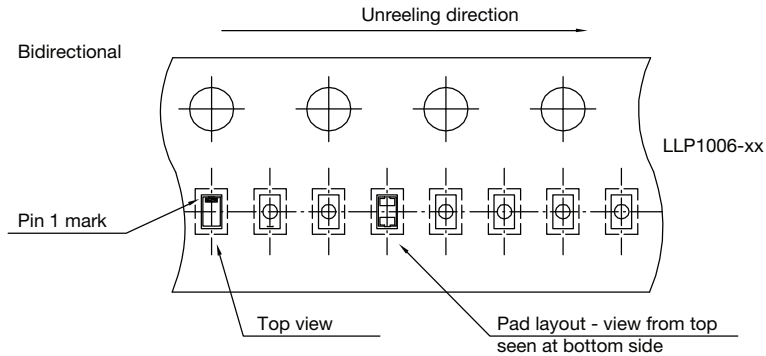


Foot print recommendation:



Document no.: S8-V-3906.04-019 (4)  
Rev. 1 - Date: 15.July 2015  
21798

Pad design patented:  
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